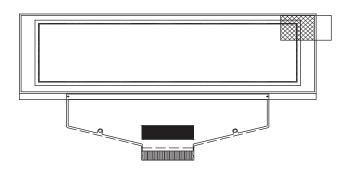


www.vishay.com Vishay

256 x 64 Graphic OLED



MECHANICAL DATA						
ITEM	STANDARD VALUE	UNIT				
Module dimension	88.0 x 27.8 x 2.05					
Viewing area	78.78 x 21.18					
Active area	76.778 x 19.178	mm				
Dot size	0.278 x 0.278	mm				
Dot pitch	0.3 x 0.3					
Mounting hole	n/a					

FEATURES

• Type: graphic

Display format: 256 x 64 dotsBuilt-in controller: SSD1322

Duty cycle: 1/64+3 V power supply

• Interface: 6800, 8000, and SPI

With polarizer

 Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

	Pb
ı	Pb-free

COMPLIANT

ABSOLUTE MAXIMUM RATINGS						
ITEM	SYMBOL	STANDAR	STANDARD VALUE			
I I CIVI	STIVIBUL	MIN.	MAX.	UNIT		
Supply voltage for operation ⁽¹⁾⁽²⁾	V _{CI}	-0.3	4			
Supply voltage for logic ⁽¹⁾⁽²⁾	V_{DD}	-0.5	2.75	V		
Supply voltage for I/O pins (1)(2)	V _{DDI/O}	-0.5	V _{CI}	V		
Supply voltage for display (1)(2)	V _{CC}	-0.5	20			
Operating temperature	T _{OP}	-40	+80	°C		
Storage temperature	T _{STG}	-40	+80			

Notes

- (1) All the above voltages are on the basis of " $V_{SS} = 0 \text{ V}$ ".
- (2) When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to section 6 "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

ELECTRICAL CHARACTERISTICS							
ITEM	CVMPOL	CONDITION	STA	STANDARD VALUE			
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply voltage for logic	V _{CI}	(1)	2.8	3.0	3.3		
Supply voltage for display	V _{CC}	-	14	14.5	15		
Input high voltage	V _{IH}	-	0.8 V _{DDI/O}	-	V _{DDI/O}		
Input low voltage	V _{IL}	=	0	-	0.2 V _{DDI/O}	V	
Output high voltage	V _{OH}	=	0.9 V _{DDI/O}	-	V _{DDI/O}		
Output low voltage	V _{OL}	-	0	-	0.1 V _{DDI/O}		
50 % check board operating current	I _{DD}	V _{CC} = 14.5 V	23	25	32	mA	

Note

⁽¹⁾ Supply voltage for logic = V_{DD} core power supply can be regulated from V_{CI}.

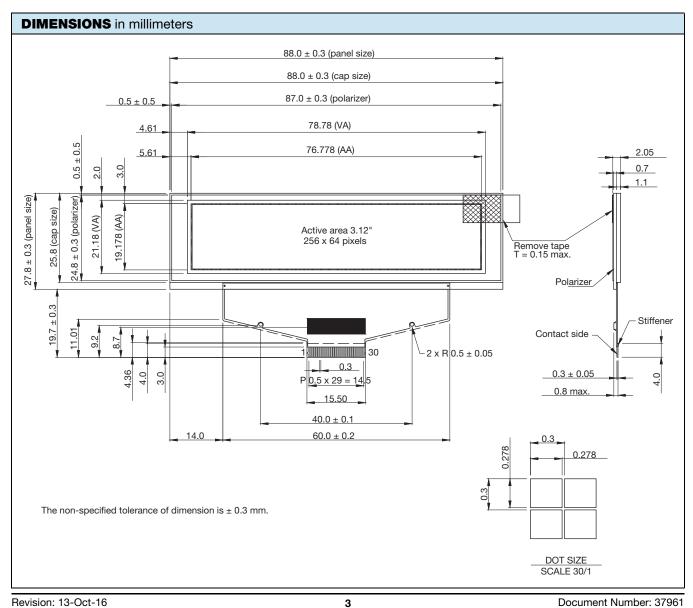
OPTIONS	OPTIONS								
	EMITTING COLOR						MOQ		
YELLOW	GREEN	RED	BLUE	WHITE	YELLOW	GREEN	RED	BLUE	WHITE
-	Yes	ı	-	-	-	Yes	ı	-	ı

Revision: 13-Oct-16 **1** Document Number: 37961 For technical questions, contact: displays@vishay.com



INTERFACE PIN FUNCTION								
PIN NO.	SYMBOL	I/O			FUNCTION			
POWER S	SUPPLY							
26	V _{CI}	Р	Power supply for op This is a voltage sup than V _{DD} and V _{DDI/O} .	ply pin. It must be co	onnected to externa	l source and always	be equal to or higher	
25	V_{DD}	Р	This is a voltage sup	Power supply for core logic circuit This is a voltage supply pin. It can be supplied externally (within the range of 2.4 V to 2.6 V) or regulated nternally from V _{CI} . A capacitor should be connected between this pin and V _{SS} under all circumstances.				
24	V _{DDI/O}	Р	Power supply for I/O pin This pin is a power supply pin of I/O buffer. It should be connected to V_{DD} or external source. All I/O signal should have V_{IH} reference to $V_{DDI/O}$. When I/O signal pins (BS0 to BS1, D0 to D7, control signals) pull high, they should be connected to $V_{DDI/O}$.					
2	V _{SS}	Р		Ground of logic circuit This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.				
3, 29	V _{CC}	Р	Power supply for OL These are the most p	•	y pin of the chip. Th	ey must be connecte	ed to external source.	
5, 28	V _{LSS}	Р	Ground of analog cir These are the analog		should be connected	d to V_{SS} externally.		
DRIVER								
22	I _{REF}	I	This pin is segment	Current reference for brightness adjustment This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS} . Set the current lower than 10 μ A.				
4	V _{сомн}	Р	This pin is the input	Voltage output high level for COM signal This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and V _{SS} .				
27	V _{SL}	Р	This is segment volta	Voltage output low level for SEG signal This is segment voltage reference pin. When external V _{SL} is not used, this pin should be left open. When external V _{SL} is used, this pin should connect with resistor and diode to ground.				
TESTING	PADS							
21	FR	0	Frame frequency triggering signal This pin will send out a signal that could be used to identify the driver status. Nothing should be connected to this pin. It should be left open individually.				. Nothing should be	
16	BS0		Communicating prot These pins are MCU		nput. See the follow	ing table:		
		I		3-wire SPI	4-wire SPI	8-bit 68XX parallel	8-bit 80XX parallel	
	D 0.		BS0	1	0	1	0	
17	BS1		BS1	0	0	1	1	
20	RES#	I	Power reset for cont This pin is reset sign		n is low, initialization	n of the chip is execu	uted.	
19	CS#	I	Chip select This pin is the chip s low.	elect input. The chip	is enabled for MCU	communication only	y when CS# is pulled	
18	D/C#	I	This pin is data / cor display data. When	Data / command control This pin is data / command control pin. When the pin is pulled high, the input at D7 to D0 is treated as display data. When the pin is pulled low, the input at D7 to D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the timing characteristics				
14	E/RD#	I	as the enable (E) sig pulled low. When co	face input. When into nal. Read / write ope nnecting to an 80XX itiated when this pin	eration is initiated wh microprocessor, thi is pulled low and	hen this pin is pulled s pin receives the rea	r, this pin will be used high and the CS# is ad (RD#) signal. Data When serial mode is	

INTERI	INTERFACE PIN FUNCTION							
PIN NO.	SYMBOL	I/O	FUNCTION					
15	R/W#	I	Read / write select or write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as read / write (R / W#) selection input. Pull this pin to "high" for read mode and pull it to "low" for write mode. When 80XX interface mode is selected, this pin will be the write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to V _{SS} .					
6 to 13	D7 to D0	I/O	Host data input / output bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to V _{SS} except for D2 in serial mode.					
RESERVE								
23	NC	-	Reserved pin The NC pin between function pins are reserved for compatible and flexible design.					
1, 30	NC (GND)	-	Reserved pin (supporting pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.					





Vishay

1.Module Classification Information

 OLED
 -256
 Y
 064
 B
 G
 P
 P
 3
 N
 0
 0
 000

 1
 2
 3
 4
 5
 6
 7
 8
 9
 10
 11
 12
 13

1	Brand: Vishay Intertechnology, Inc.						
2	Horizontal Forma	t: 256 columns					
3	Display Type : N→Character Type, H→Graphic Type, Y→TAB Type ,O→COG Type						
4	Vertical Format:	64 rows or lines					
5	Series code: B						
		A : Amber	R: RED				
	F '''' O I	B: Blue	C : Full color				
6	Emitting Color	G: Green	W: White				
		Y: Yellow Green	L: Yellow				
7	Polarizer P: With Polarizer; N: Without Polarizer						
8	Display Mode P : Passive Matrix ; A: Active Matrix						
9	Driver Voltage	3: 3.0 V; 5: 5.0V					
10	Touch Panel	N : Without touch panel; T: With touch panel					
		0 : Standard type					
		Sunlight Readable type					
11	Products type	2. Transparent OLED (TOLED)					
		3. Flexible OLED					
		4. OLED for Lighting					
		0 : Standard(A-level)					
		2 : B-level					
12	Product grades	3 : C-level					
		4 : high class(AA-level)					
		5 : Customer offerings					
13	Serial No.	Application serial number(000~ZZZ)					



Vishay

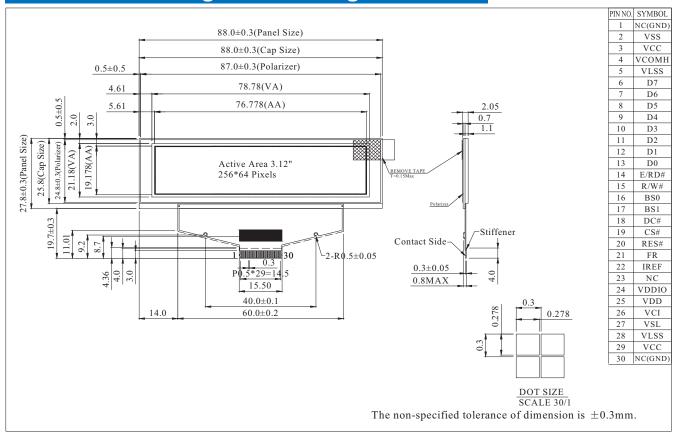
2.General Specification

Item	Dimension	Unit
Dot Matrix	256 x 64 Dots	_
Module dimension	88.0 × 27.8 × 2.05 (mm)	mm
Active Area	76.778×19.178 (mm)	mm
Pixel Size	0.278×0.278 (mm)	mm
Pixel Pitch	0.3×0.3 (mm)	mm
Display Mode	Passive Matrix	
Display Color	Green	
Drive Duty	1/64 Duty	
IC	SSD1322	



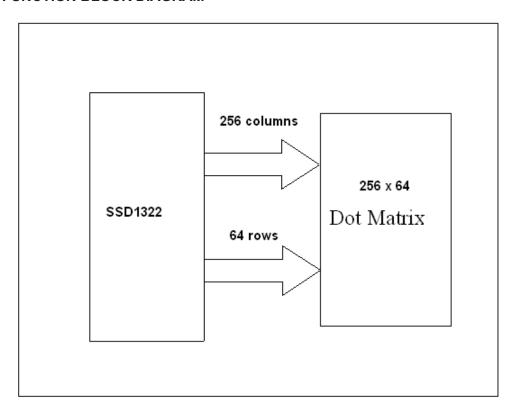
Vishay

3. Contour Drawing & Block Diagram



Vishay

FUNCTION BLOCK DIAGRAM



^{*}For more information, please refer to the SSD1322 datasheet.

Vishay

4. Interface Pin Function

Pin Number	Symbol	I/O	Function
Number			
Power Supp	oly	l	
26	VCI	Р	Power Supply for Operation
			This is a voltage supply pin. It must be connected to
			external source & always be equal to or higher than VDD
25	VDD	Р	& VDDIO. Power Supply for Core Logic Circuit
23	V D D	-	This is a voltage supply pin. It can be supplied externally (within
			the range of 2.4~2.6V) or regulated internally from VCI. A
			capacitor should be connected between this pin & VSS under
	1/2-212		all circumstances.
24	VDDIO	Р	Power Supply for I/O Pin This pip is a power supply pip of I/O buffer. It about he
			This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signal should have
			VIH reference to VDDIO. When I/O signal pins (BS0~BS1,
			D0~D7, control signals) pull high, they should be connected
			to VDDIO.
2	VSS	Р	Ground of Logic Circuit
			This is a ground pin. It also acts as a reference for the logic
3,29	VCC	Р	pins. It must be connected to external ground. Power Supply for OLED Panel
3,29	VCC	F	These are the most positive voltage supply pin of the chip. They
			must be connected to external source.
5,28	VLSS	Р	Ground of Analog Circuit
			These are the analog ground pins. They should be connected
			to VSS externally.
Driver	IDEE	l ,	Ourse of Defense of the Drinkford Adjustment
22	IREF		Current Reference for Brightness Adjustment This pin is segment current reference pin. A resister should be
			This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower
			than 10uA.
4	VCOMH	Р	Voltage Output High Level for COM Signal
			This pin is the input pin for the voltage output high level for
			COM signals. A tantalum capacitor should be connected
			between this pin and VSS.
27	VSL	Р	Voltage Output Low Level for SEG Signal
			This is segment voltage reference pin.
			When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with
			resistor and diode to ground.
	1	L	. co.co. a a.co to ground



Testing Pad	ls					
21	FR	0	Frame Frequency Triggering Sign This pin will send out a signal that c driver status. Nothing should be con be left open individually.	ould be us		
16	BS0	1	Communicating Protocol Select			
17	BS1	•	These pins are MCU interface selectable:			ollowing
				BS0	BS1	
			3-wire SPI	1	0	
			4-wire SPI	0	0	
			8-bit 68XX Parallel	1	1	
			8-bit 80XX Parallel	0	1	J
20	RES#	I	Power Reset for Controller and D This pin is reset signal input. When of the chip is executed.		low, initial	ization
19	CS#	I	Chip Select This pin is the chip select input. The communication only when CS# is p		nabled for	MCU
18	D/C#	I	Data/Command Control This pin is Data/Command control p high, the input at D7~D0 is treated a When the pin is pulled low, the input transferred to the command registe MCU interface signals, please refer Timing Characteristics Diagrams.	as display t at D7~D r. For deta	data. 0 will be	
14	E/RD#	1	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.			
15	R/W#	I	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.			
6~13	D7~D0	I/O	Host Data Input/Output Bus These pins are 8-bit bi-directional d the microprocessor's data bus. Whe			



OLED-256Y064B-GPP3N00000

www.vishay.com

			D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.
Reserve			
23	N.C.	-	Reserved Pin
			The N.C. pin between function pins are reserved for compatible and flexible design.
1,30	N.C.	-	Reserved Pin (Supporting Pin)
	(GND)		The supporting pins can reduce the influences from stresses
			on the function pins. These pins must be connected to external ground.



Vishay

5.Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	VCI	-0.3	4	V	1, 2
Supply Voltage for Logic	VDD	-0.5	2.75	V	1, 2
Supply Voltage for I/O Pins	VDDIO	-0.5	VCI	V	1, 2
Supply Voltage for Display	VCC	-0.5	20	V	1, 2
Operating Temperature	TOP	-40	80	°C	-
Storage Temperature	TSTG	-40	80	°C	-

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 6 "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate



Vishay

6.Electrical Characteristics

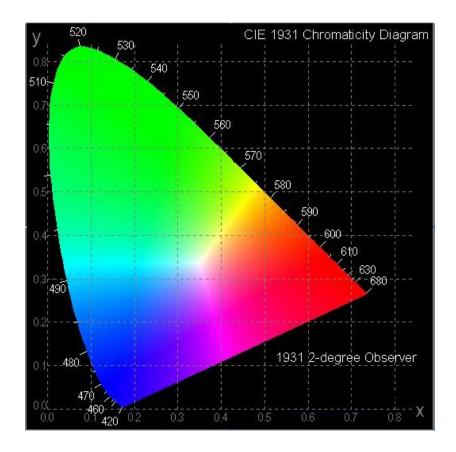
Item	Symbol	Condition	Min	Тур	Max	Unit
Supply Voltage for Operation	VCI	Note	2.8	3.0	3.3	V
Supply Voltage for Display	VCC	_	14	14.5	15	V
High Level Input	VIH	_	0.8×V _{DDIO}	_	V _{DDIO}	V
Low Level Input	VIL	_	0	_	0.2×V _{DDIO}	V
High Level Output	VOH	_	0.9×V _{DDIO}	_	V _{DDIO}	V
Low Level Output	VOL	_	0	_	0.1×V _{DDIO}	V
50% Check Board operating	Current	VCC =14.5V	23	25	32	mA

Note: Supply Voltage for Logic = VDD core power supply can be regulated from VCI.

Vishay

7. Optical Characteristics

Item	Symbol	Condition	Min	Тур	Max	Unit
View Angle	(V)θ		160			deg
View Arigie	(Η)φ		160			deg
Contrast Ratio	CR	Dark	2000:1		_	_
Response Time	T rise	_		10		μs
Response fille	T fall	_		10		μs
Display with 50% check Board Brig		ghtness	100	120		cd/m2
CIEx(Green)		(CIE1931)	0.24	0.28	0.32	
CIEy(Green)		(CIE1931)	0.59	0.63	0.67	



Vishay

www.vishay.com

8.OLED Lifetime

ITEM	Conditions	Min	Тур	Remark
Operating Life Time	Ta=25°C / Initial 50% check board brightness Typical Value	40,000 Hrs	-	Note

Notes:

- 1. Life time is defined the amount of time when the luminance has decayed to <50% of the initial value
- 2. This analysis method uses life data obtained under accelerated conditions to extrapolate an estimated probability density function (*pdf*) for the product under normal use conditions.
- 3. Screen saving mode will extend OLED lifetime.



Vishay

9. Reliability

Content of Reliability Test

Environmenta	l Test		1
Test Item	Content of Test	Test Condition	Applicable Standard
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80□ 240hrs	
_ow Temperature storage	Endurance test applying the low storage temperature for a long time.	-40□ 240hrs	
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	80□ 240hrs	
ow Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40□ 240hrs	
High Femperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60□,90%RH 240hrs	
Temperature Cycle	Endurance test applying the low and high temperature cycle. -40 25 80 30min 5min 30min 1 cycle	-40□/80□ 100 cycles	
Mechanical Tes	st		
/ibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hr	
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sin wave 11 ms 3 times of each direction	
Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	
Others			
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	

OLED-256Y064B-GPP3N00000



www.vishay.com

Vishay

Test and measurement conditions

- 1. All measurements shall not be started until the specimens attain to temperature stability. After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.
- 2. All-pixels-on is used as operation test pattern.
- 3. The degradation of Polarizer are ignored for High Temperature storage, High Temperature/ Humidity Storage, Temperature Cycle

Evaluation criteria

- 1. The function test is OK.
- 2. No observable defects.
- 3. Luminance: > 50% of initial value.
- 4. Current consumption: within ± 50% of initial value.

APPENDIX:

RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

Vishay

10.Inspection Specification

NO	Item	Criterion			AQL
01	Electrical Testing	 1.1 Missing vertical, horizontal segment, segment contrast defect. 1.2 Missing character, dot or icon. 1.3 Display malfunction. 1.4 No function or no display. 1.5 Current consumption exceeds product specifications. 1.6 OLED viewing angle defect. 1.7 Mixed product types. 1.8 Contrast defect. 			0.65
02	Black or white spots on OLED (display only)	 2.1 White and black spots on display ≤0.25mm, no more than three white or black spots present. 2.2 Densely spaced: No more than two spots or lines within 3mm. 		2.5	
03	OLED black spots, white spots, contamina tion (non-displ ay)	3.1 Round type : As following drawing Φ=(x+y)/2 X Y Y	SIZE $\Phi \le 0.10$ $0.10 < \\ \Phi \le 0.20$ $0.20 < \\ \Phi \le 0.25$ $0.25 < \Phi$	Acceptable Q TY Accept no dense 2	2.5
		3.2 Line type : (As following Length $$ $L \le 3.0$ $L \le 2.5$ $$	g drawing) Width W≤0.02 0.02 <w≤0.03 0.03<w≤0.05="" 0.05<w<="" td="" =""><td>Acceptable Q TY Accept no dense 2 As round type</td><td>2.5</td></w≤0.03>	Acceptable Q TY Accept no dense 2 As round type	2.5
04	Polarizer bubbles	If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.	Size Φ $\Phi \le 0.20$ $0.20 < \Phi \le 0.50$ $0.50 < \Phi \le 1.00$ $1.00 < \Phi$ Total Q TY	Acceptable Q TY Accept no dense 3 2 0 3	2.5



05 \$	Scratches	Symbols Define: x: Chip length	t: Glass thickness a:	Chip thickness	
		x: Chip length k: Seal width L: Electrode pad leng	t: Glass thickness a:		
		6.1 Conoral glass ch			
			ip : surface and crack bety	ween panels:	
		- Chin thickness	Chinidth	v. Chin langth	
		z: Chip thickness Z≦1/2t	y: Chip width Not over viewing	x: Chip length x≦1/8a	
	Chipped	2 ≧ 1/21	area	X <u>=</u> 170d	2.5
00 0	glass	1/2t <z≦2t< td=""><td>Not exceed 1/3k</td><td>x≦1/8a</td><td>2.3</td></z≦2t<>	Not exceed 1/3k	x≦1/8a	2.3
		6.1.2 Corner crack: z : Chip thickness $Z \le 1/2t$ $1/2t < z \le 2t$	y: Chip width Not over viewing area Not exceed 1/3k ore chips, x is the total	x: Chip length x≤1/8a x≤1/8a	



NO	Item	Criterion	AQL
		Symbols: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: OLED side length L: Electrode pad length 6.2 Protrusion over terminal: 6.2.1 Chip on electrode pad:	
		$\begin{array}{ c c c c c c }\hline y: Chip \ width & x: Chip \ length & z: Chip \ thickness \\\hline y \le 0.5 mm & x \le 1/8a & 0 < z \le t \\\hline \end{array}$	
		6.2.2 Non-conductive portion:	
06	Glass	y 12 X X	2.5
		y: Chip width x: Chip length z: Chip thickness	
		$y \le L$ $x \le 1/8a$ $0 < z \le t$	
		 If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications. If the product will be heat sealed by the customer, the alignment mark not be damaged. Substrate protuberance and internal crack. 	
		y: width x: length	
		$y \le 1/3L$ $x \le a$	
		у	





NO	Item	Criterion	AQL
07	Cracked glass	The OLED with extensive crack is not acceptable.	2.5
08	Backlight elements	 8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using OLED spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong. 	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination.9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	 10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, OLED pad, zebra pad or screw hold pad, make sure it is smoothed down. 	2.5 2.5 0.65 2.5 2.5 0.65 2.5
11	Soldering	 11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB. 	2.5 2.5 2.5 0.65





NO	Item	Criterion	AQL
12	General appearance	 12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. 12.2 No cracks on interface pin (OLB) of TCP. 12.3 No contamination, solder residue or solder balls on product. 12.4 The IC on the TCP may not be damaged, circuits. 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever. 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 12.7 Sealant on top of the ITO circuit has not hardened. 12.8 Pin type must match type in specification sheet. 12.9 OLED pin loose or missing pins. 12.10 Product packaging must the same as specified on packaging specification sheet. 12.11 Product dimension and structure must conform to product specification sheet. 	2.5 0.65 2.5 2.5 2.5 2.5 0.65 0.65 0.65 0.65

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Short	Major	
Wrong Display	Major	
Un-uniform B/A x 100% < 70% A/C x 100% < 70%	Major	A Normal B Dark Fixed C We Light Fixed

Vishay

11.Precautions in Use of OLED Modules

Modules

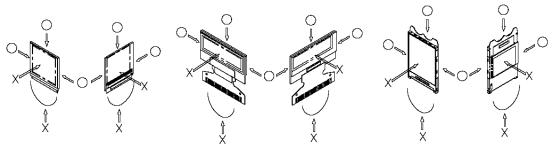
- (1)Avoid applying excessive shocks to module or making any alterations or modifications to it.
- (2)Don't make extra holes on the printed circuit board, modify its shape or change the components of OLED display module.
- (3)Don't disassemble the OLED display module.
- (4)Don't operate it above the absolute maximum rating.
- (5)Don't drop, bend or twist OLED display module.
- (6) Soldering: only to the I/O terminals.
- (7)Storage: please store in anti-static electricity container and clean environment.
- (8)Use a "Screen Saver" to extend the lifetime. Do not show fixed information for a long time in the application.
- (9)Don't use fixed information in OLED panel for long time that will cause "screen burn" effect.
- (10)The manufacturer has the right to change the passive components, including R2and R3 adjust resistors. (Resistors, capacitors and other passive components will have different appearance and color caused by the different supplier.)
- (11)The manufacturer has the right to change the PCB Rev. (In order to satisfy supply stability, management optimization, and the best product performance..., under the premise of not affecting the electrical characteristics and external dimensions. The manufacturer has the right to modify the version.)
- 11.1. Handling Precautions
- (1) Since the display panel is made of glass, do not apply mechanical impacts such us dropping from a high position.
- (2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale or ingest the organic substance.
- (3) If pressure is applied to the display surface or its neighborhood of the OLED display module, the cell structure may be damaged, be careful not to apply pressure to these sections.
- (4) The polarizer covering the surface of the OLED display module is soft and easily scratched. Please be careful when handling the OLED display module.
- (5) When the surface of the polarizer of the OLED display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
 - * Scotch Mending Tape No. 810 or an equivalent
 - Never try to breathe upon the soiled surface or wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

Also, pay attention that the following liquid and solvents can damage the polarizer:

- * Water
- * Ketone
- * Aromatic Solvents
- (6) Hold OLED display module very carefully when placing OLED display module into the system housing. Do not apply excessive stress or pressure to OLED display module. And, do not over bend the film with electrode pattern layouts.
 - These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



Vishay



- (7) Do not apply stress to the LSI chips and the surrounding molded sections.
- (8) Do not disassemble or modify the OLED display module.
- (9) Do not apply input signals while the logic power is off.
- (10) Pay sufficient attention to the working environments when handing OLED display modules to prevent occurrence of element breakage accidents by static electricity.
- * Be sure to make human body grounding when handling OLED display modules.
- * Be sure to ground tools to use or assembly such as soldering irons.
- * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
- * Protective film is being applied to the surface of the display panel of the OLED display module. Be careful since static electricity may be generated when removing the protective film.
- (11) Protective film is applied to the surface of the display panel. Remove the protective film before assembly. If the OLED display module has been stored for a long period of time, residue adhesive material from the protective film may remain on the surface of the display panel after the film is removed. In such case, remove the residue material by the method introduced in the above Section 5.
- (12) If electric current is applied when the OLED display module has moisture condensation or when it is placed under high humidity environments, the electrodes may corrode.

11.2. Storage Precautions

(1) When storing OLED display modules, put them in static electricity preventive bags avoiding exposure to direct sun light and fluorescent lamps. Avoid high temperature and high humidity environment or low temperature (less than 0°C) environments.

(We recommend storing these modules in the packaged state as they were shipped.) At that time, be careful not to let water drops adhere to the packages or bags or let condensation occur with them.

(2) If electric current is applied when condensation is present or when it is placed under high humidity environments, the electrodes may corrode.

11.3. Designing Precautions

- (1) The absolute maximum ratings are the ratings which cannot be exceeded for OLED display module, and if these values are exceeded, panel damage may be happen.
- (2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
- (3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
- (4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
- (5) For EMI, take necessary measures in the application equipment.
- (6) When fastening the OLED display module, fasten the external plastic housing section.
- (7) If power supply to the OLED display module is forcibly shut down by such errors as taking out the main battery while the OLED display panel is in operation, we cannot guarantee the quality of this OLED display module.

OLED-256Y064B-GPP3N00000



www.vishay.com

Vishay

* Connection (contact) to any other potential than the above may lead to rupture of the IC.11.4.

Precautions when disposing of the OLED display modules

 Request the qualified companies to handle industrial wastes when disposing of the OLED display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

11.5. Other Precautions

- (1) When an OLED display module is operated for a long time with a fixed pattern, the pattern may remain as an after image with slight contrast or brightness variation.
- Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
- (2) To protect OLED display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OLED display modules.
- * Pins and electrodes
- * Pattern layouts such as the TCP & FPC
- (3) With this OLED display module, the OLED driver is exposed. Generally, semiconductor elements change their characteristics when exposed to light, similar to the principle of the solar battery. Consequently, if this OLED driver is exposed to light, malfunctioning may occur.
- * Design the product and installation method so that the OLED driver may be shielded from light in actual usage.
- * Design the product and installation method so that the OLED driver may be shielded from light during the inspection processes.
- (4) Although this OLED display module stores the operational state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal states may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
- (5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.
- (6)Resistors, capacitors and other passive components will have different appearance and color caused by the different supplier.
- (7) The manufacturer has the right to upgrade and modify the product function.



Legal Disclaimer Notice

Vishay

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.