Understanding Dual Terminator Resistor Networks

By Mike Casey

One of the least understood resistor network schematics in the industry today is the dual-resistor terminator schematic shown below in the 8-pin SIP and in the 16-pin DIP configuration.

This schematic shows up in both commercial / industrial parts and in military parts. Commercial parts are sometimes identified as TTL dual-line terminators or as pulse-squaring terminators. The military parts are identified in MIL-PRF-83401 as “H” (SIP) and “J” (DIP) schematics.

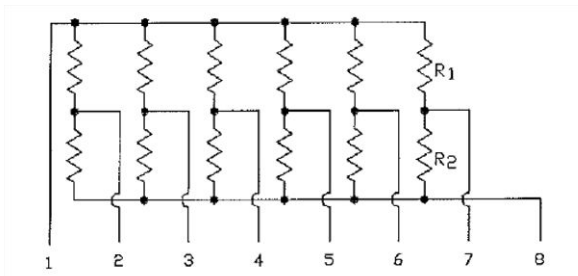

Fig. 1 - MSPxx05 - 8-Pin SIP

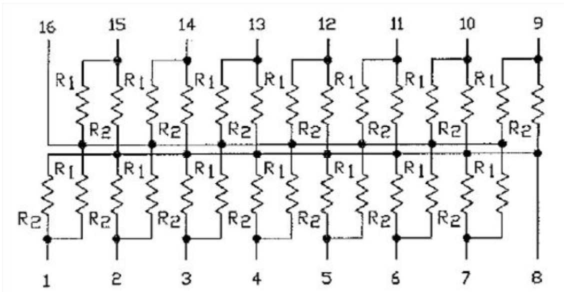

Fig. 2 - MDPxx05 - 16-Pin DIP

The SIP and the DIP schematics are both basically the same, in that each has two common busses with “N” leads and “N-2” series sets of R_1 and R_2 in parallel between the two busses. This ‘unique’ electrical schematic makes it impossible to measure the individual R_1 and R_2 values using a simple ohmmeter, a two-wire / four-wire (Kelvin) digital ohmmeter, or a resistance-scanning system without active-guarding capabilities.

However, two methods are available for determination of the accuracy of the resistor within each network if an active-guard test system is not available. Method I described below may be used to calculate the ‘equivalent’ resistances measureable at the various terminals of the network. Method II describes how to measure the ‘voltage-ratio’ of each resistor in the network.

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METHOD I

All schematics regardless of the number of pin-outs can be analyzed in the same way, but the 16-pin DIP will be examined here since it is the most complex.

STEP 1: Redraw the 16-pin DIP schematic as shown below. It will them resemble the SIP schematic except for the number of $R_1 + R_2$ parallel branches in the circuit.

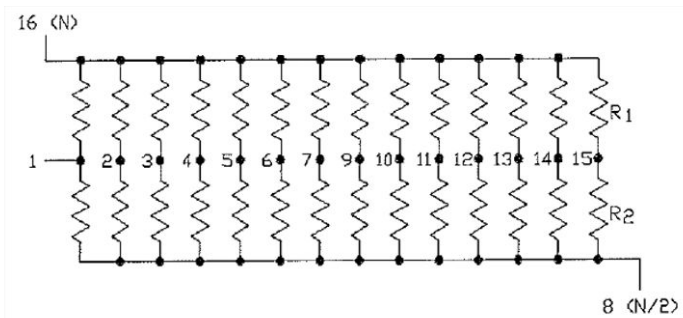


Fig. 3

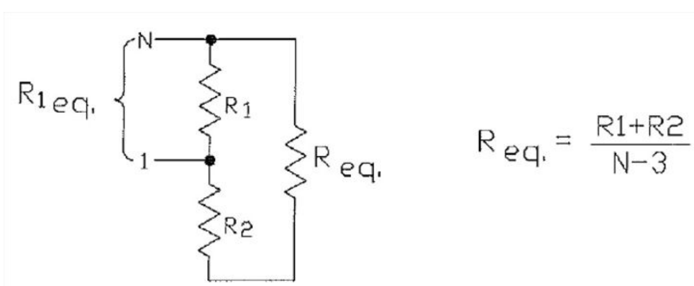
STEP 2: Calculate the first of “3” equivalent resistance measurements, the measurement between two common busses, as follows. On the SIP schematic, this measurement will be made between pin 1 and pin “N”. On the DIP schematic, this measurement will be made between pin “N” and pin “N/2”.

For the schematic shown in Figure 3, the equivalent resistance between the two busses is calculated using the following formula:

$$R_{eq.} \text{ (between pin N and N/2)} = \frac{R_1 + R_2}{N-2}$$

STEP 3: Calculate the second, “R_1”, equivalent resistance measurement, which can be made between pins 1, 2, 3,..., N-1 (excluding pin N/2), and the common pin “N”.

To illustrate this, the schematic shown in Fig. 3 is simplified as follows:



Step 3A

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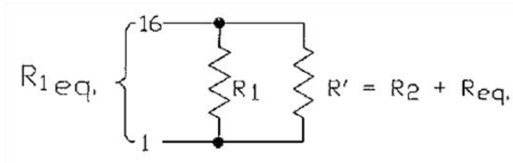
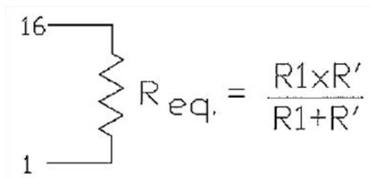
Add $R_2 + R_{eq.}$ in series to get R'.



Step 3B

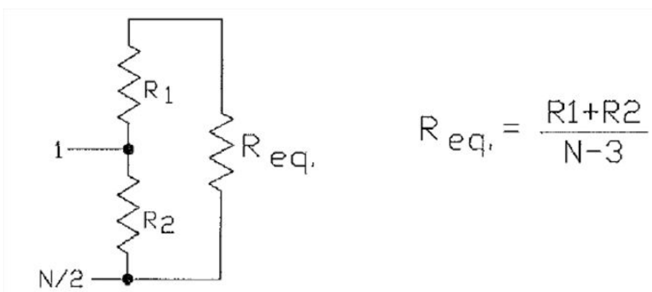
Compute the parallel equivalent of R_1 and R'.



Step 3C

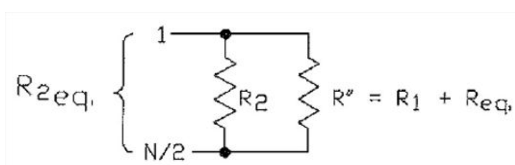
This is the $R_{1\ eq.}$ resistance value that can be measured between pins 1, 2, 3,…, N-1 (excluding pin N/2).

STEP 4: Calculate the third and last, "R_2" equivalent resistance measurement, which can be made between pins 1, 2, 3,…, N-1 (excluding pin N) and the common pin N/2. To illustrate this, the schematic shown in Fig. 3 is simplified as follows:



Step 4A

Add $R_1 + R_{eq.}$ in series to get R".



Step 4B

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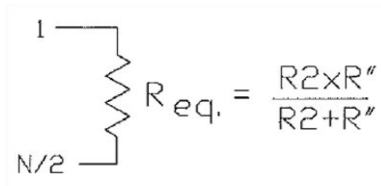
Compute the parallel equivalent of R_2 and R".



Step 4C

This is the $R_{2\ eq.}$ resistance value that can be measured between pins 1, 2, 3,…, N-1 (excluding pin N), and the common pin N. This concludes the calculations for $R_{eq.}$, $R_{1\ eq.}$ and $R_{2\ eq.}$, the resistance values that can be measured on the network using a simple ohmmeter or an unguarded resistance test system.

METHOD II

All schematics regardless of the number of pin-outs can be analyzed in this manner. The object is to compute the theoretical voltage drop at pins 1, 2, 3,…, N-1 with voltage “V” applied to pin N and with pin N/2 at ground potential.

<u>STEP 1</u>: Referring to Fig. 3, compute the current flow through on $R_1 + R_2$ series branch as follows:

$$I = \frac{V}{R_1 + R_2}$$

<u>STEP 2</u>: Calculate the voltage at pins 1, 2, 3,…, N-1 as follows:

$$V_{pin} = I \times R_2 = \frac{V \times R_2}{R_1 + R_2}$$

With a precision power supply supplying the voltage V (typically 5 V_{DC}), the voltage at each pin, V_{pin}, can be measured and should not vary more than ± the individual resistor tolerance at each pin. If all voltages measure the calculated V_{pin} ± the individual resistor tolerance, then all resistors within the circuit can be assumed to be within tolerance.