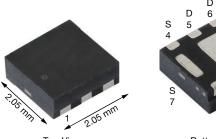
www.vishay.com

Vishay Siliconix

Automotive N-Channel 80 V (D-S) 175 °C MOSFET

PowerPAK® SC-70W-6L Single



Marking Code: QOXXXX

Bottom View

PRODUCT SUMMARY				
V _{DS} (V)	80			
$R_{DS(on)}$ (Ω) at $V_{GS} = 10 \text{ V}$	0.0546			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0700			
I _D (A)	9			
Configuration	Single			

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- · Wettable flank terminals
- 100 % R_a and UIS tested
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





HALOGEN FREE

	D	
G o —		
	o s	

N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SC-70W-6L
Lead (Pb)-free and halogen-free	SQA600CEJW (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATING	GS (T _C = 25 °C, unless	s otherwise noted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V_{DS}	80		
Gate-source voltage		V_{GS}	± 20		
Continuous drain surrent	T _C = 25 °C ^a	ı	9		
Continuous drain current	T _C = 125 °C	l _D	6.4		
Continuous source current (diode conduction) a		I _S	9	А	
Pulsed drain current ^a		I _{DM}	29		
Single pulse avalanche current		I _{AS}	13		
Single pulse avalanche energy L = 0.1 mH		E _{AS}	8.45	mJ	
Maximum power dissipation	T _C = 25 °C	Р	13.6	W	
	T _C = 125 °C	P_{D}	4.5		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) d, e			260		

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount c	R_{thJA}	90	°C/W
Junction-to-case (drain)		R_{thJC}	11	C/VV

Notes

- a. Package limited
- b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %
- c. When mounted on 1" square PCB (FR4 material)
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70W-6L is a leadless package and features wettable flank terminals. The end of the lead terminal is plated with tin.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



Vishay Siliconix

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		•			•	I.	l.
Drain-source breakdown voltage	V _{DS}	V _{GS} =	= 0 V, I _D = 250 μA	80	-	-	V
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		1.5	2.0	2.5	V
Gate-source leakage	I _{GSS}	V _{DS} =	0 V, V _{GS} = ± 20 V	-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = 80 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 80 V, T _J = 125 °C	-	-	50	μΑ
		V _{GS} = 0 V	V _{DS} = 80 V, T _J = 175 °C	-	-	250	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 \text{ V}$	5	-	-	Α
		V _{GS} = 10 V	I _D = 3 A	-	0.0442	0.0546	
Duning and the second of the s	Б	V _{GS} = 10 V	I _D = 3 A, T _J = 125 °C	-	-	0.0902	Ω
Drain-source on-state resistance a	R _{DS(on)}	V _{GS} = 10 V	I _D = 3 A, T _J = 175 °C	-	-	0.1084	
		V _{GS} = 4.5 V	I _D = 2.5 A	-	0.0567	0.0700	
Forward transconductance b	9fs	V _{DS} :	= 15 V, I _D = 2.5 A	-	10	-	S
Dynamic ^b							
Input capacitance	C _{iss}			-	376	540	
Output capacitance	Coss	$V_{GS} = 0 V$	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	-	196	280	рF
Reverse transfer capacitance	C _{rss}	1		-	8	13	
Total gate charge ^c	Qg			-	6	9	
Gate-source charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 40 \text{ V}, I_D = 4.2 \text{ A}$	-	1.6	-	nC
Gate-drain charge ^c	Q _{gd}			-	0.6	-	
Gate resistance	Rg		f = 1 MHz	0.4	0.9	1.4	Ω
Turn-on delay time ^c	t _{d(on)}			-	8	13	
Rise time ^c	t _r	V _{DD} :	= 40 V , $R_L = 20 \Omega$	-	3	6]
Turn-off delay time ^c	t _{d(off)}	$I_D \cong 2 A$,	$I_D \cong 2 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		13	20	ns
Fall time ^c	t _f]		-	3	6	
Source-Drain Diode Ratings and Charact	eristics ^b						
Pulsed current ^a	I _{SM}			-	-	29	Α
Forward voltage	V _{SD}	I _F =	= 3 A, V _{GS} = 0 V	-	0.75	1.2	V
Body diode reverse recovery time	t _{rr}			-	12	48	ns
Body diode reverse recovery charge	Q _{rr}	1		-	4	28	nC
Reverse recovery fall time	ta	$\int_{\mathbb{R}} \mathbf{r} = 2 d\mathbf{r}$	A, di/dt = 100 A/μs	-	7	-	
Reverse recovery rise time	t _b	1		-	5	-	ns
Body diode peak reverse recovery current	I _{RM(REC)}			-	-0.8	-	Α

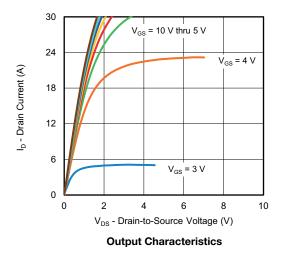
Notes

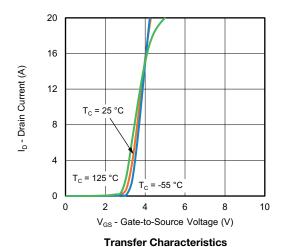
- a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

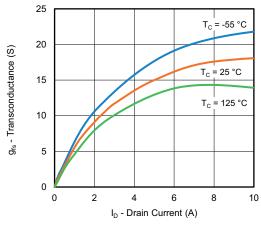
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



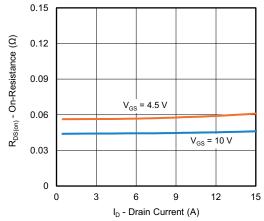
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



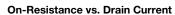


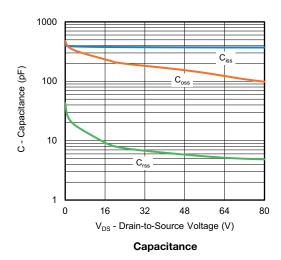


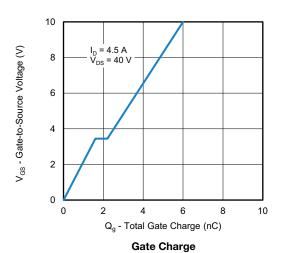






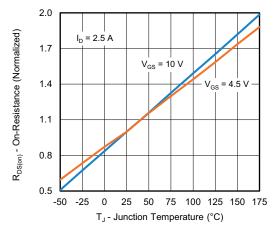




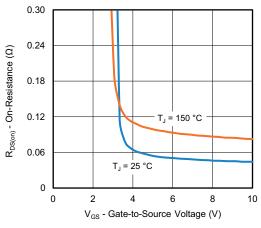




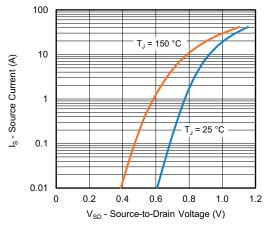
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



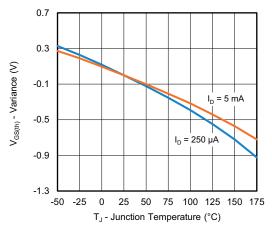
On-Resistance vs. Junction Temperature



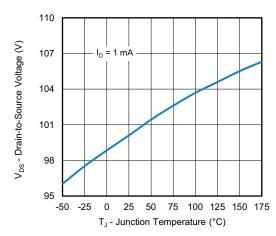
On-Resistance vs. Gate-to-Source Voltage



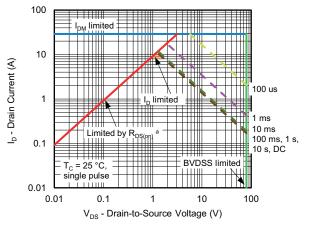
Source Drain Diode Forward Voltage



Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



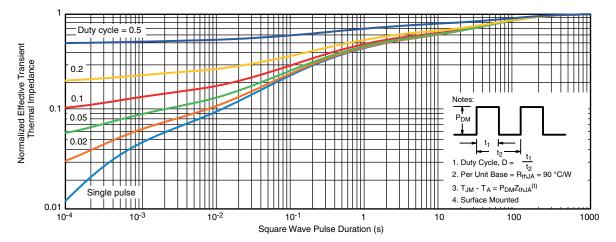
Safe Operating Area

Note

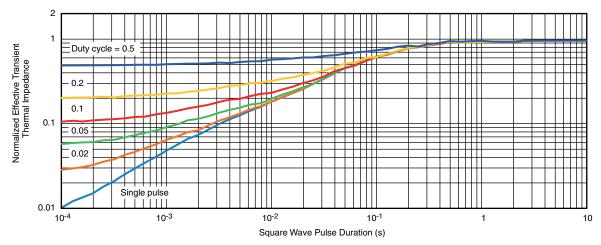
a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

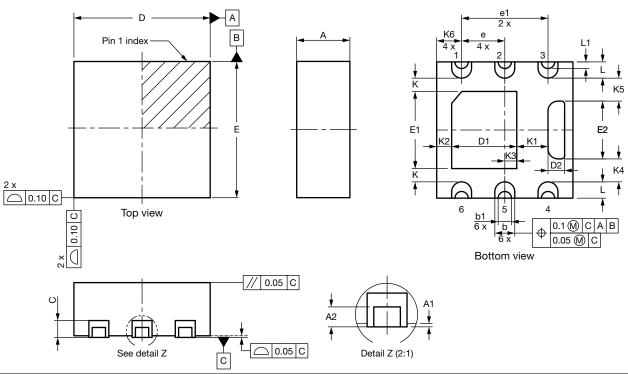


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63082.



PowerPAK® SC70W-6L SIDEWETTABLE



DIM.		MILLIMETERS		INCHES			
DIWI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.70	0.80	0.90	0.027	0.031	0.035	
A1	0.00	0.02	0.05	0.000	0.001	0.002	
A2	0.10	-	-	0.004	-	-	
b	0.25	0.30	0.35	0.010	0.012	0.014	
b1	0.15	0.20	0.23	0.006	0.008	0.009	
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	1.95	2.05	2.15	0.077	0.081	0.085	
D1	0.88	0.98	1.08	0.035	0.039	0.043	
D2	0.20	0.25	0.30	0.008	0.010	0.012	
E	1.95	2.05	2.15	0.077	0.081	0.085	
E1	1.06	1.16	1.26	0.042	0.046	0.050	
E2	0.82	0.87	0.92	0.032	0.034	0.036	
е		0.65 BSC			0.026 BSC		
e1		1.30 BSC			0.051 BSC		
K		0.20 typ.			0.008 typ.		
K1		0.47 typ.			0.019 typ.		
K2		0.23 typ.		0.009 typ.			
K3		0.18 typ.		0.007 typ.			
K4		0.35 typ.			0.014 typ.		
K5		0.35 typ.			0.014 typ.		
K6		0.38 typ.		0.015 typ.			
L	0.15	0.25	0.35	0.006	0.010	0.014	
L1	-	0.10	-	-	0.004	-	

DWG: 6076

Notes

- Package outline exclusive of mold flash and metal burr
- Package outline inclusive of plating

Revison: 10-Jan-2020 1 Document Number: 77413



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