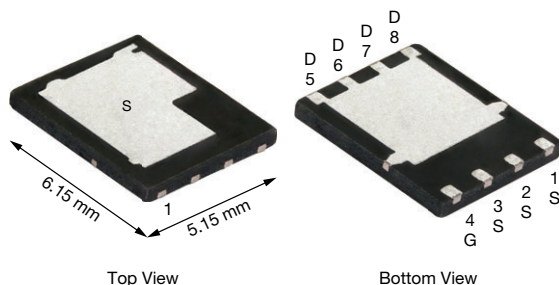


N-Channel 45 V (D-S) 175 °C MOSFET

PowerPAK® SO-8DC



FEATURES

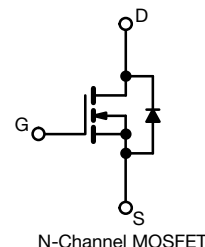
- TrenchFET® Gen IV power MOSFET
- 45 V Drain-source break-down voltage
- Tuned for low Q_g and Q_{oss}
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- Motor drive control



PRODUCT SUMMARY	
V_{DS} (V)	45
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00120
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.00180
Q_g typ. (nC)	50.5
I_D (A) ^a	228
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8DC
Lead (Pb)-free and halogen-free	SiDR608EP-T1-RE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	45	V	
Gate-source voltage	V_{GS}	+20, -16	V	
Continuous drain current ($T_J = 175$ °C)	$T_C = 25$ °C	228	A	
	$T_C = 70$ °C	190		
	$T_A = 25$ °C	56 ^{b, c}		
	$T_A = 70$ °C	47 ^{b, c}		
Pulsed drain current ($t = 100$ μ s)	I_{DM}	400		
Continuous source-drain diode current	$T_C = 25$ °C	113		
	$T_A = 25$ °C	6.8 ^{b, c}		
Single pulse avalanche current	$L = 0.1$ mH	50		
Single pulse avalanche energy	E_{AS}	125	mJ	
Maximum power dissipation	$T_C = 25$ °C	125	W	
	$T_C = 70$ °C	87.5		
	$T_A = 25$ °C	7.5 ^{b, c}		
	$T_A = 70$ °C	5.25 ^{b, c}		
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) ^{d, e}		260		

Notes

- Based on $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8DC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

**THERMAL RESISTANCE RATINGS**

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	15	20	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	0.9	1.2	
Maximum junction-to-case (source)	Steady state	R_{thJC}	1.1	1.4	

Notes

a. Surface mounted on 1" x 1" FR4 board

b. Maximum under steady state conditions is 54 °C/W

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	45	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	29	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-5.8	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.1	-	2.3	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 45 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 45 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.00100	0.00120	Ω
		V _{GS} = 4.5 V, I _D = 20 A	-	0.00136	0.00180	
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 20 A	-	120	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	8900	-	pF
Output capacitance	C _{oss}		-	1244	-	
Reverse transfer capacitance	C _{rss}		-	120	-	
C _{rss} /C _{iss} ratio			-	0.0135	0.0270	-
Total gate charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 20 A	-	111	167	nC
		V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 20 A	-	50.5	76	
Gate-source charge	Q _{gs}		-	26	-	
Gate-drain charge	Q _{gd}		-	7.8	-	
Output charge	Q _{oss}	V _{DS} = 20 V, V _{GS} = 0 V	-	59	-	
Gate resistance	R _g	f = 1 MHz	0.3	0.88	1.5	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 1 Ω I _D ≡ 20 A, V _{GEN} = 10 V, R _g = 1 Ω	-	19	38	ns
Rise time	t _r		-	10	20	
Turn-off delay time	t _{d(off)}		-	50	100	
Fall time	t _f		-	8	16	
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 1 Ω I _D ≡ 20 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	52	104	
Rise time	t _r		-	86	172	
Turn-off delay time	t _{d(off)}		-	50	100	
Fall time	t _f		-	25	50	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	113	A
Pulse diode forward current (t _p = 100 μs)	I _{SM}		-	-	400	
Body diode voltage	V _{SD}	I _S = 10 A	-	0.7	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	52	104	ns
Body diode reverse recovery charge	Q _{rr}		-	71	142	nC
Reverse recovery fall time	t _a		-	32	-	ns
Reverse recovery rise time	t _b		-	20	-	

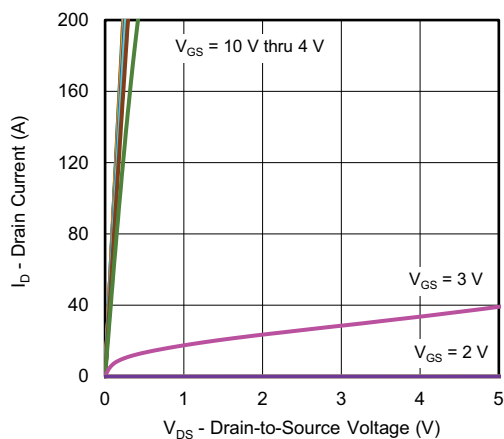
Notesa. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

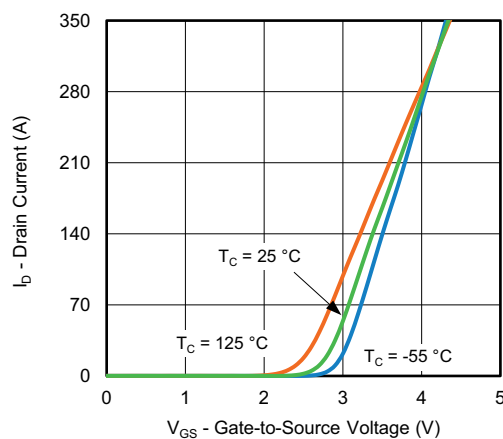
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



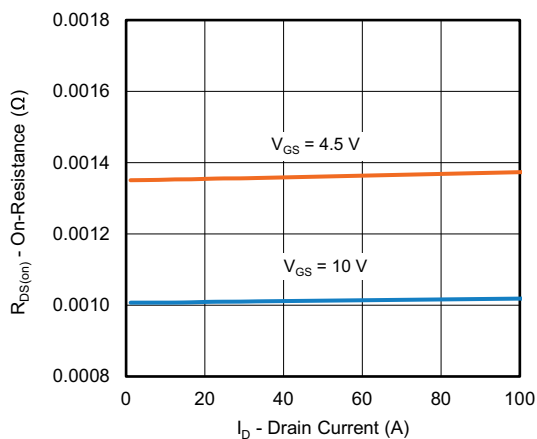
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



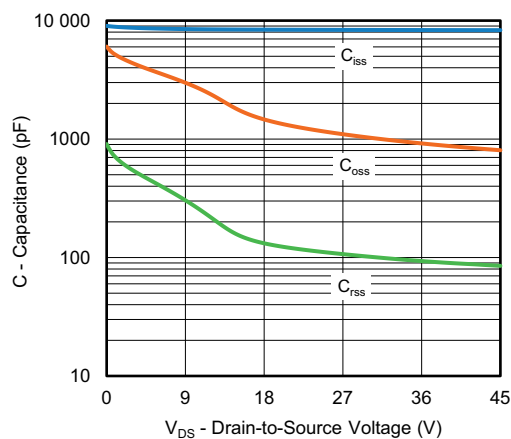
Output Characteristics



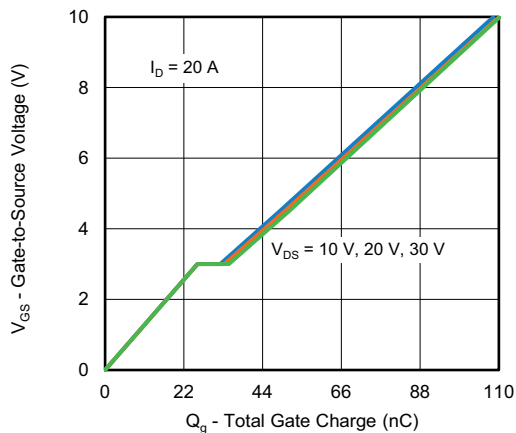
Transfer Characteristics



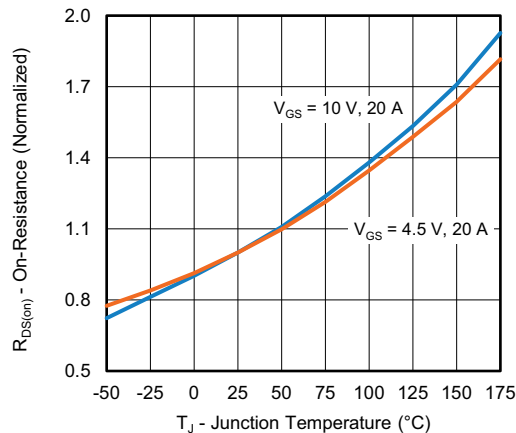
On-Resistance vs. Drain Current



Capacitance



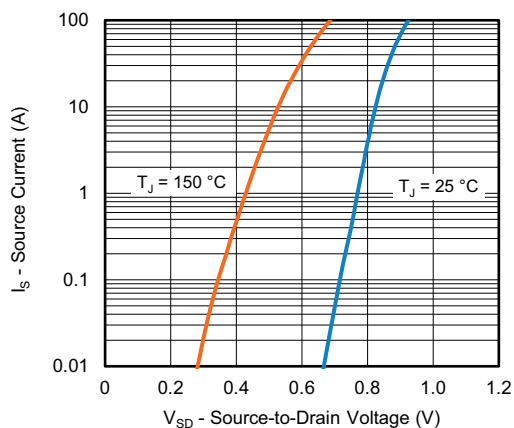
Gate Charge



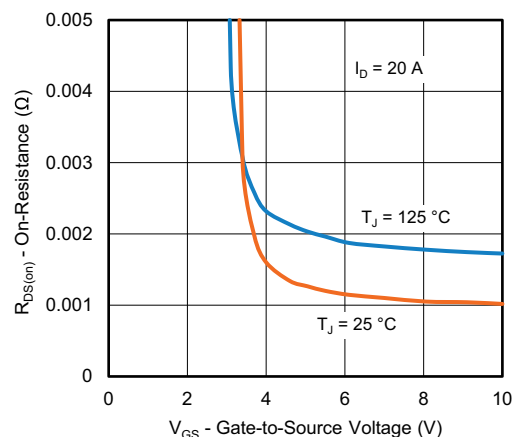
On-Resistance vs. Junction Temperature



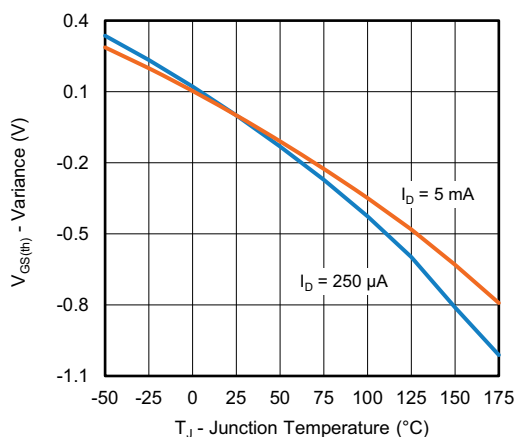
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



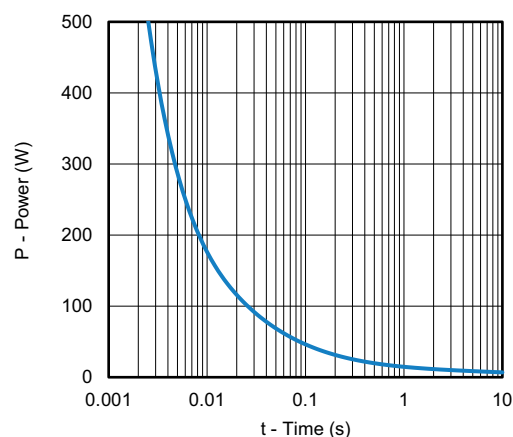
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



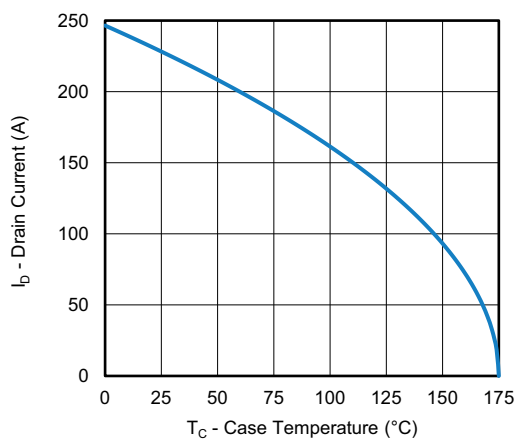
Threshold Voltage



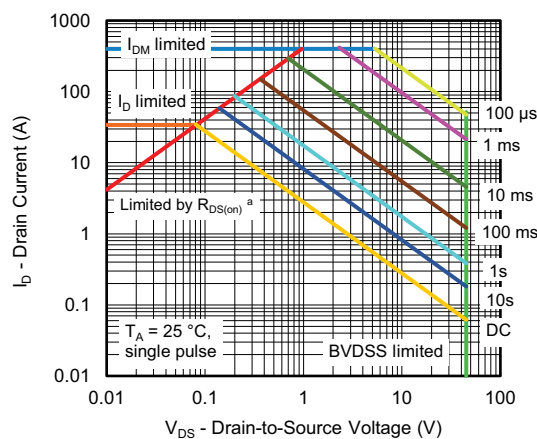
Single Pulse Power, Junction-to-Ambient



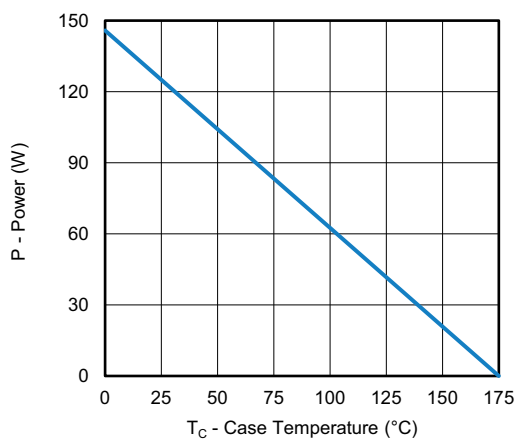
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



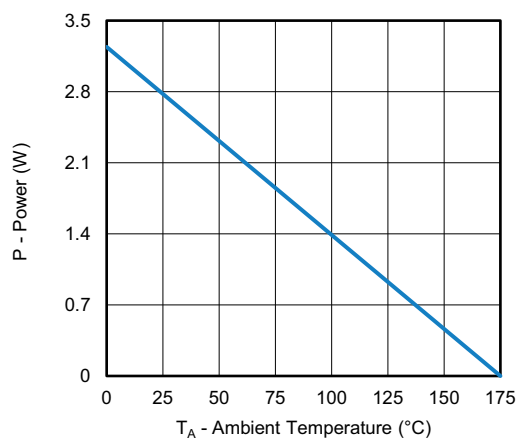
Current Derating ^a



Safe Operating Area ^b



Power, Junction-to-Case



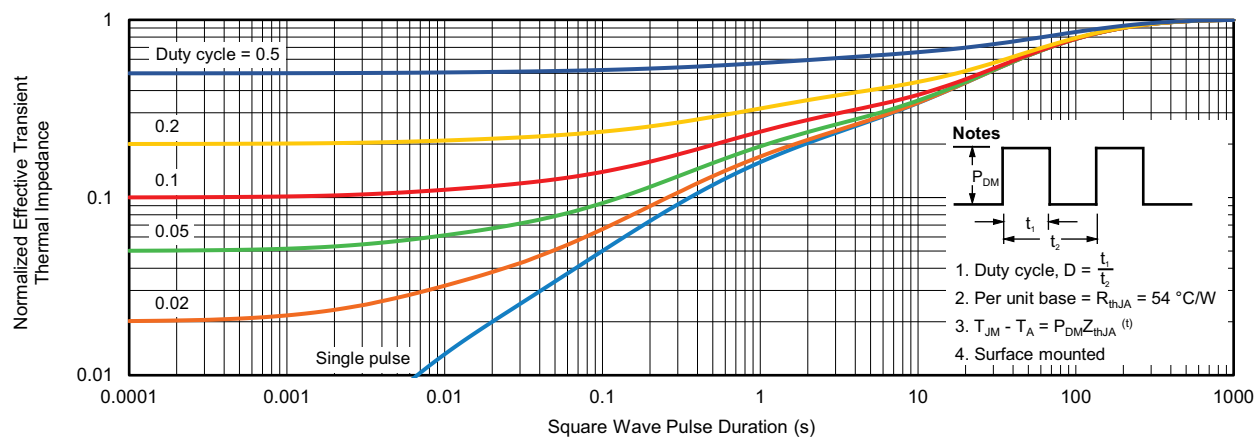
Power, Junction-to-Ambient

Notes

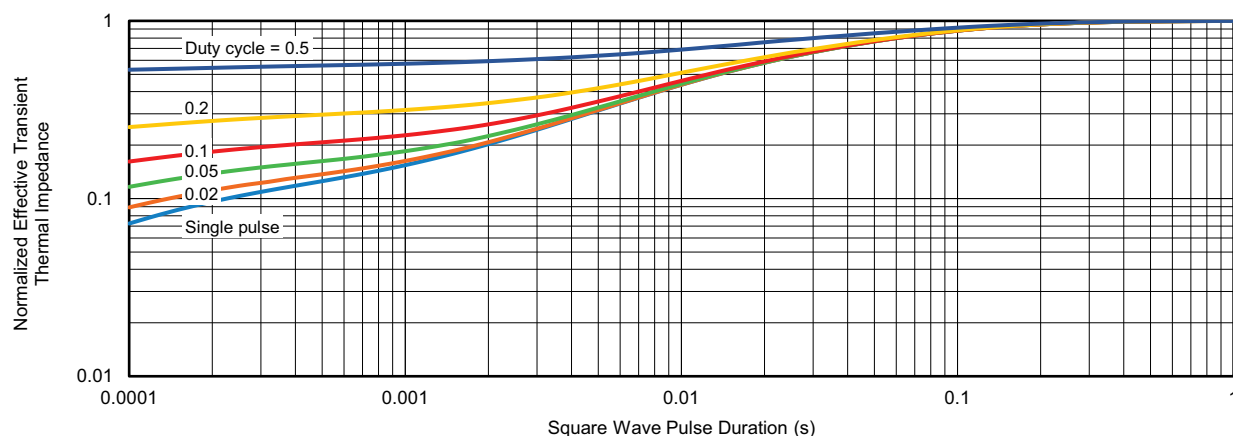
- The power dissipation P_D is based on T_J max. = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit
- $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

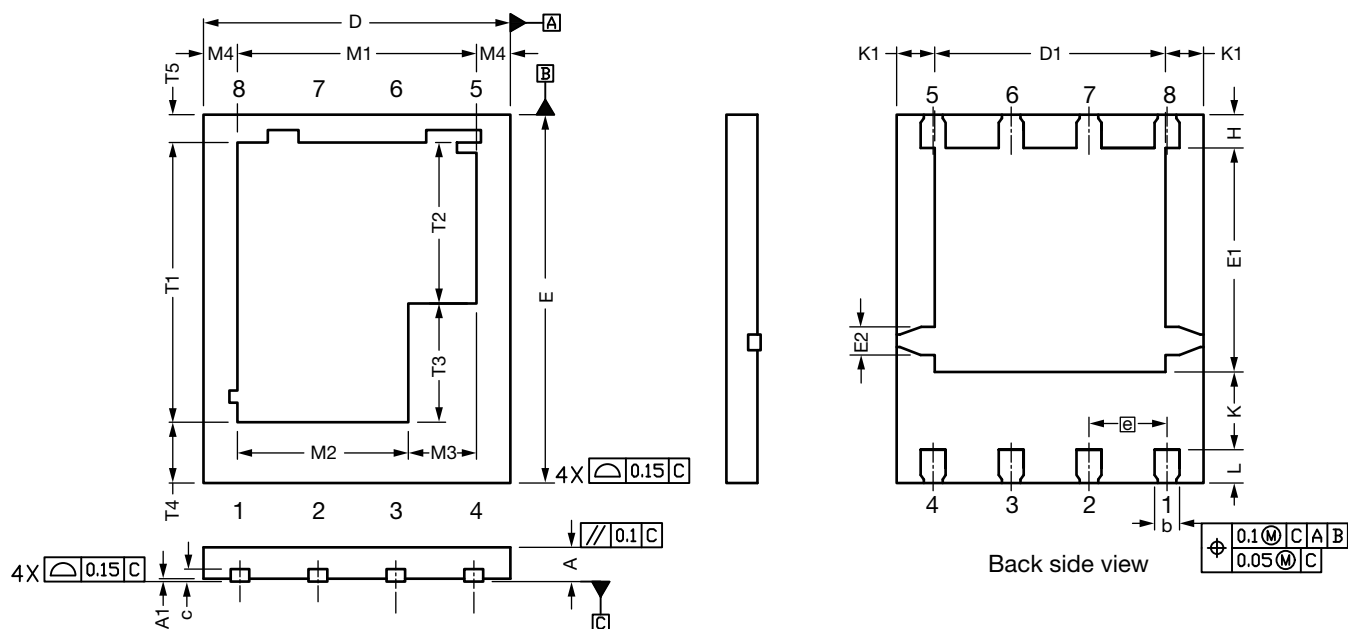


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63123.

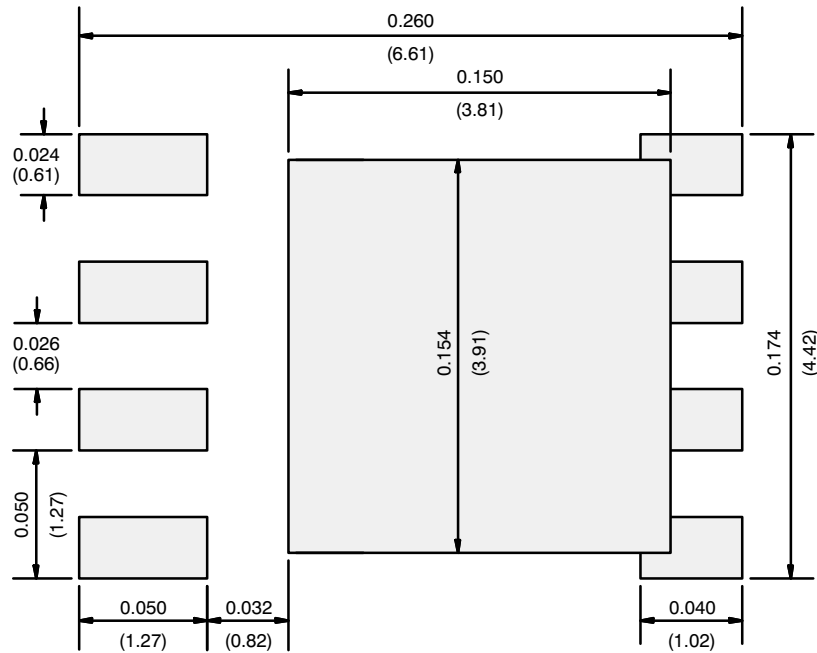


PowerPAK® SO-8 Double Cooling Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.51	0.56	0.61	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.36	0.41	0.46	0.014	0.016	0.018
c	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	3.71	3.76	3.81	0.146	0.148	0.150
e	1.27 BSC			0.050 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.60	3.65	3.70	0.142	0.144	0.146
E2	0.46 typ.			0.018 typ.		
H	0.49	0.54	0.59	0.019	0.021	0.023
K	1.22	1.27	1.32	0.048	0.050	0.052
K1	0.64 typ.			0.025 typ.		
L	0.49	0.54	0.59	0.019	0.021	0.023
M1	3.85	3.90	3.95	0.152	0.154	0.156
M2	2.74	2.79	2.84	0.108	0.110	0.112
M3	1.06	1.11	1.16	0.042	0.044	0.046
M4	0.56 typ.			0.022 typ.		
N	8			8		
T1	4.51	4.56	4.61	0.178	0.180	0.182
T2	2.58	2.63	2.68	0.102	0.104	0.106
T3	1.88	1.93	1.98	0.074	0.076	0.078
T4	0.97 typ.			0.038 typ.		
T5	0.48 typ.			0.019 typ.		
ECN: T21-0014-Rev. B, 08-Feb-2021						
DWG: 6048						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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