1.1 V to 5.5 V, Slew Rate Controlled Load Switch

DESCRIPTION

SiP32408 and SiP32409 are slew rate controlled load switches designed for 1.1 V to 5.5 V operation.

These devices guarantee low switch on-resistance at 1.2 V input. They feature a controlled soft-on slew rate of typical 2.5 ms that limits the inrush current for designs of heavy capacitive load and minimizes the resulting voltage droop at the power rails.

SiP32408 and SiP32409 feature a low voltage control logic interface (on/off interface) that can interface with low voltage control signals without extra level shifting circuit.

Both SiP32408 and SiP32409 have exceptionally low shutdown current and provide reverse blocking to prevent high current flowing into the power source.

SiP32409 integrates a output discharge circuit for fast turn off.

Both SiP32408 and SiP32409 are available in TDFN4 package of 1.2 mm by 1.6 mm.

FEATURES

- 1.1 V to 5.5 V operation voltage range
- Flat row R_{ON} down to 1.2 V
- 42 mΩ typical from 1.5 V to 5 V
- Slew rate controlled turn-on: 2.5 ms at 3.6 V
- Low quiescent current < 1 µA when disabled 10.5 µA typical at V_{IN} = 1.2 V
- Reverse current blocking when switch is off
- Output discharge (SiP32409)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE Available

APPLICATIONS

- PDAs/smart phones
- Notebook/netbook computers
- Tablet PC
- Portable media players
- Digital camera
- GPS navigation devices
- Data storage devices
- Optical, industrial, medical, and healthcare devices

TYPICAL APPLICATION CIRCUIT

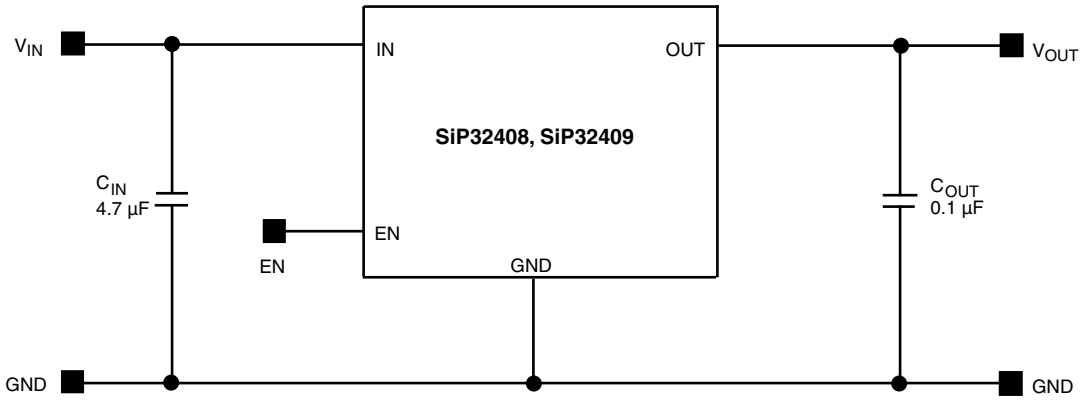


Fig. 1 - SiP32408, SiP32409 Typical Application Circuit

ORDERING INFORMATION			
TEMPERATURE RANGE	**PACKAGE**	**MARKING**	**PART NUMBER**
-40 °C to +85 °C	TDFN4 1.2 mm x 1.6 mm	Jx	SiP32408DNP-T1-GE4
		Kx	SiP32409DNP-T1-GE4

Notes

- x = lot code
- GE4 denotes halogen-free and RoHS-compliant

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	LIMIT	UNIT
Supply input voltage (V_{IN})	-0.3 to 6	V
Enable input voltage (V_{EN})	-0.3 to 6	
Output voltage (V_{OUT})	-0.3 to 6	
Maximum continuous switch current ($I_{max.}$) [c]	3.5	A
Maximum repetitive pulsed current (1 ms, 10 % duty cycle) [c]	6	
Maximum Non-Repetitive Pulsed Current (100 µs, EN = Active) [c]	12	
ESD rating (HBM)	7000	V
Junction temperature (T_J)	-40 to +150	°C
Thermal resistance (q_{JA}) [a]	170	°C/W
Power dissipation (P_D) [a,b]	735	mW

Notes

a. Device mounted with all leads and power pad soldered or welded to PC board, see PCB layout
b. Derate 5.9 mW/°C above T_A = 25 °C, see PCB layout
c. T_A = 25 °C, see PCB layout

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

PARAMETER	LIMIT	UNIT
Input voltage range (V_{IN})	1.1 to 5.5	V
Operating junction temperature range (T_J)	-40 to 125	°C

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V_{IN} = 5 V, T_A = -40 °C to 85 °C (typical values are at T_A = 25 °C)	LIMITS -40 °C to 85 °C			UNIT
			MIN. [a]	TYP. [b]	MAX. [a]	
Operating voltage [c]	V_{IN}		1.1	-	5.5	V
Quiescent current	I_Q	V_{IN} = 1.2 V, EN = active	-	10.5	17	µA
		V_{IN} = 1.8 V, EN = active	-	21	30	
		V_{IN} = 2.5 V, EN = active	-	34	50	
		V_{IN} = 3.6 V, EN = active	-	54	90	
		V_{IN} = 4.3 V, EN = active	-	68	110	
		V_{IN} = 5 V, EN = active	-	105	180	
Off supply current	$I_{Q(off)}$	EN = inactive, OUT = open	-	-	1	
Off switch current	$I_{DS(off)}$	EN = inactive, OUT = GND	-	-	1	
Reverse blocking current	I_{RB}	V_{OUT} = 5 V, V_{IN} = 0 V, V_{EN} = inactive	-	-	10	
On-resistance	$R_{DS(on)}$	V_{IN} = 1.2 V, I_L = 100 mA, T_A = 25 °C	-	45	52	mΩ
		V_{IN} = 1.8 V, I_L = 100 mA, T_A = 25 °C	-	42	50	
		V_{IN} = 2.5 V, I_L = 100 mA, T_A = 25 °C	-	42	50	
		V_{IN} = 3.6 V, I_L = 100 mA, T_A = 25 °C	-	42	50	
		V_{IN} = 4.3 V, I_L = 100 mA, T_A = 25 °C	-	42	50	
		V_{IN} = 5 V, I_L = 100 mA, T_A = 25 °C	-	44	50	
On-resistance temp. coefficient	TC_{RDS}		-	3300	-	ppm/°C

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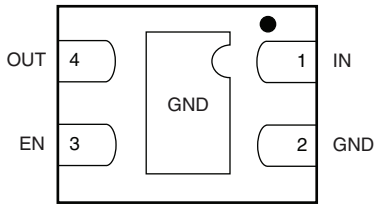
SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V_{IN} = 5 V, T_A = -40 °C to 85 °C (typical values are at T_A = 25 °C)	LIMITS -40 °C to 85 °C MIN. [a]	TYP. [b]	MAX. [a]	UNIT
EN input low voltage [c]	V_{IL}	V_{IN} = 1.2 V	-	-	0.3	V
		V_{IN} = 1.8 V	-	-	0.4 [d]	
		V_{IN} = 2.5 V	-	-	0.5 [d]	
		V_{IN} = 3.6 V	-	-	0.6 [d]	
		V_{IN} = 4.3 V	-	-	0.7 [d]	
		V_{IN} = 5 V	-	-	0.8 [d]	
EN input high voltage [c]	V_{IH}	V_{IN} = 1.2 V	0.9 [d]	-	-	
		V_{IN} = 1.8 V	1.2 [d]	-	-	
		V_{IN} = 2.5 V	1.4 [d]	-	-	
		V_{IN} = 3.6 V	1.6 [d]	-	-	
		V_{IN} = 4.3 V	1.7 [d]	-	-	
		V_{IN} = 5 V	1.8	-	-	
EN input leakage	I_{SINK}	V_{EN} = 5.5 V	-1	-	1	µA
Output pull-down resistance	R_{PD}	EN = inactive, T_A = 25 °C, (for SiP32409 only)	-	217	280	Ω
Output turn-on delay time	$t_{d(on)}$	V_{IN} = 3.6 V, R_{load} = 10 Ω, T_A = 25 °C	-	1.8	-	ms
Output turn-on rise time	$t_{(on)}$		1.2	2.5	3.8	
Output turn-off delay time	$t_{d(off)}$		-	-	0.001	

Notes

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
c. For V_{IN} outside this range consult typical EN threshold curve
d. Not tested, guarantee by design

PIN CONFIGURATION



Bottom View

Fig. 2 - TDFN4 1.2 mm x 1.6 mm Package

PIN DESCRIPTION

PIN NUMBER	NAME	FUNCTION
1	IN	This is the input pin of the switch
2	GND	Ground connection
3	EN	Enable input
4	OUT	This is the output pin of the switch

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BLOCK DIAGRAM

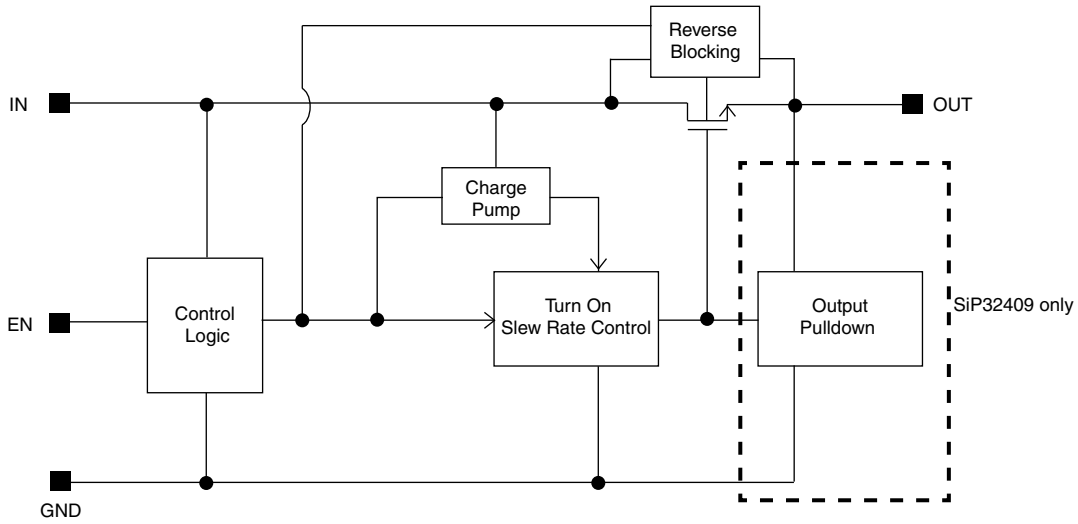


Fig. 3 - Functional Block Diagram

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

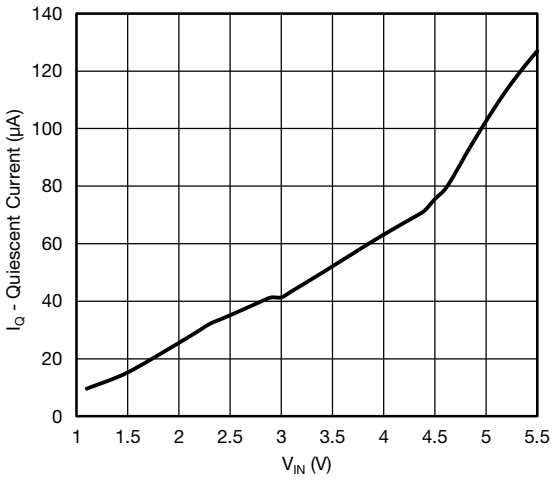


Fig. 4 - Quiescent Current vs. Input Voltage

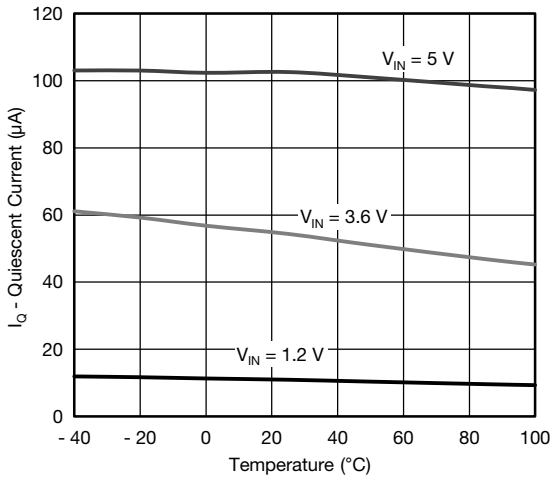


Fig. 5 - Quiescent Current vs. Temperature

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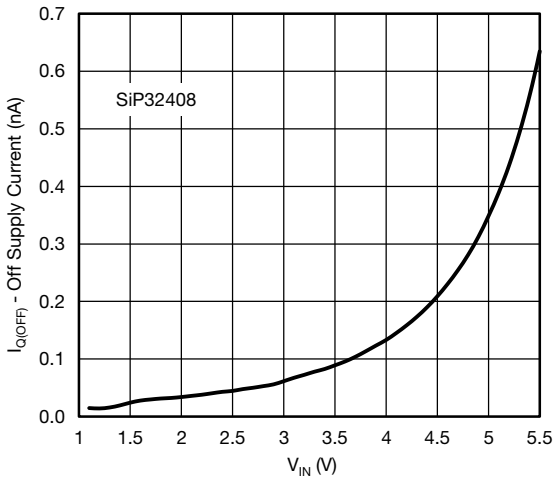


Fig. 6 - Off Supply Current vs. Input Voltage

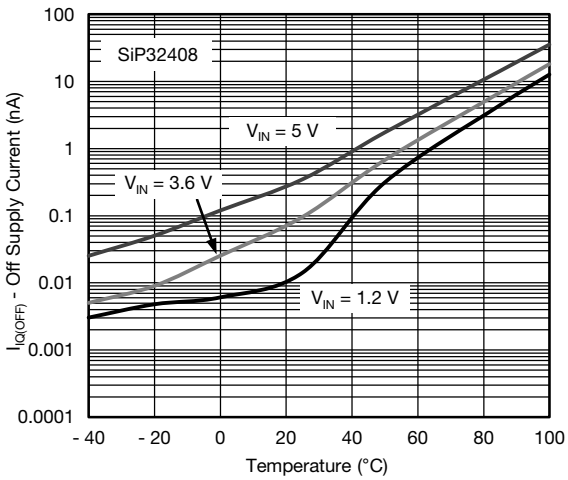


Fig. 9 - Off Supply Current vs. Temperature

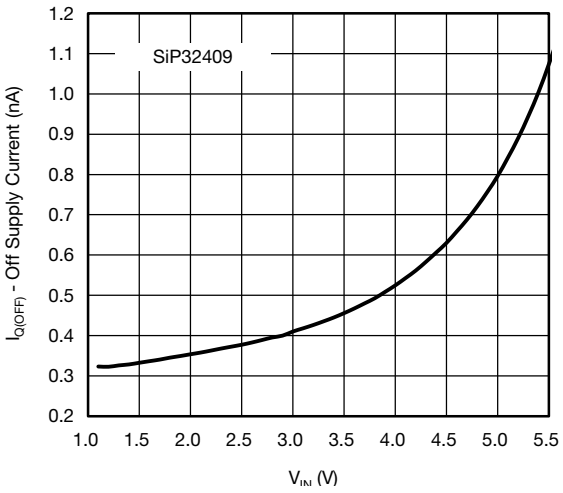


Fig. 7 - Off Supply Current vs. Input Voltage

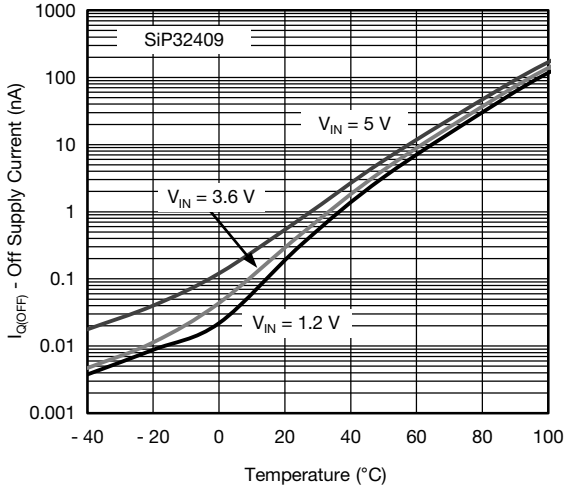


Fig. 10 - Off Supply Current vs. Temperature

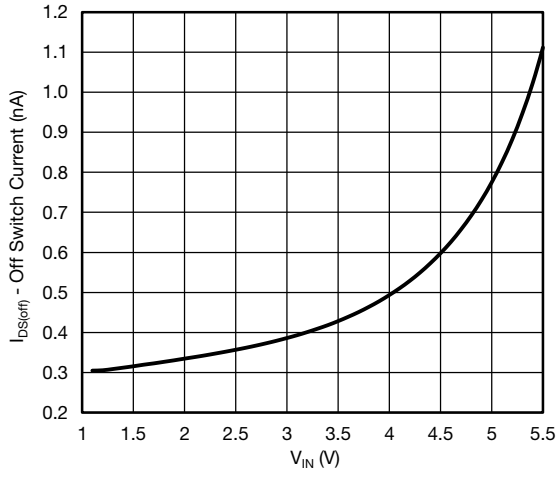


Fig. 8 - Off Switch Current vs. Input Voltage

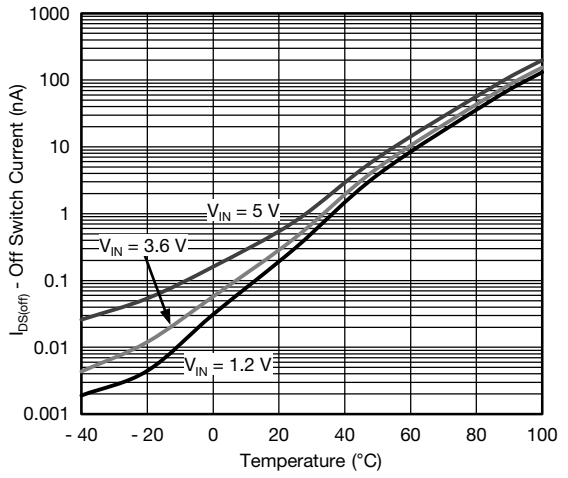


Fig. 11 - Off Switch Current vs. Temperature

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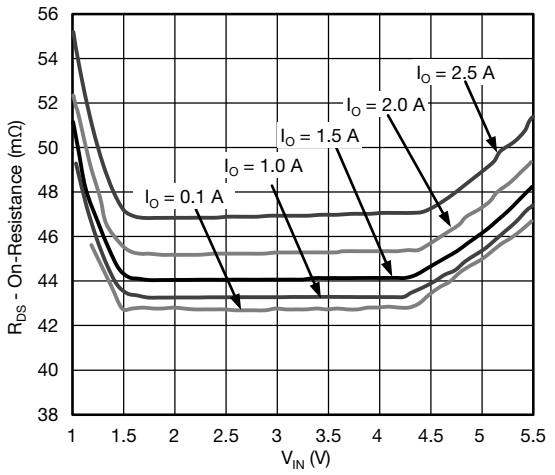


Fig. 12 - $R_{DS(on)}$ vs. V_{IN}

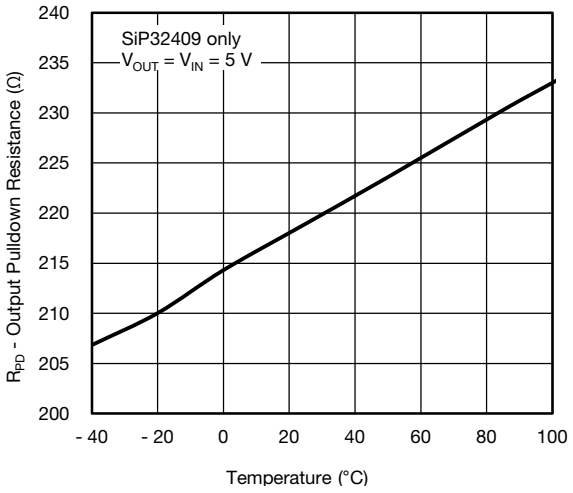


Fig. 15 - Output Pull-down Resistance vs. Temperature

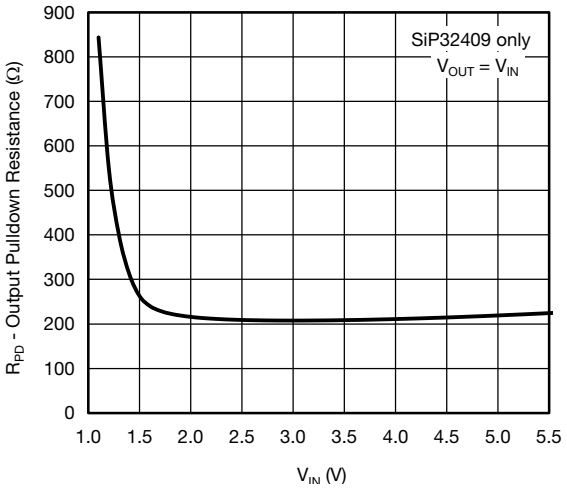


Fig. 13 - Output Pull-down Resistance vs. Input Voltage

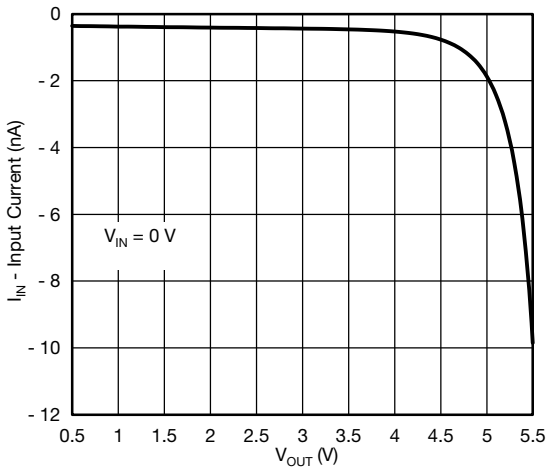


Fig. 16 - Reverse Blocking Current vs. Output Voltage

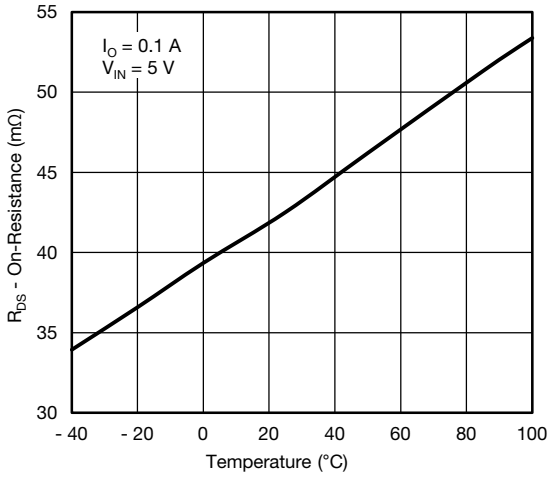


Fig. 14 - $R_{DS(on)}$ vs. Temperature

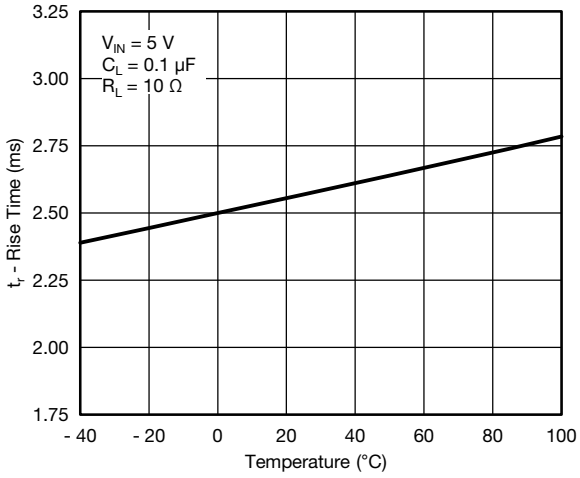


Fig. 17 - Rise Time vs. Temperature

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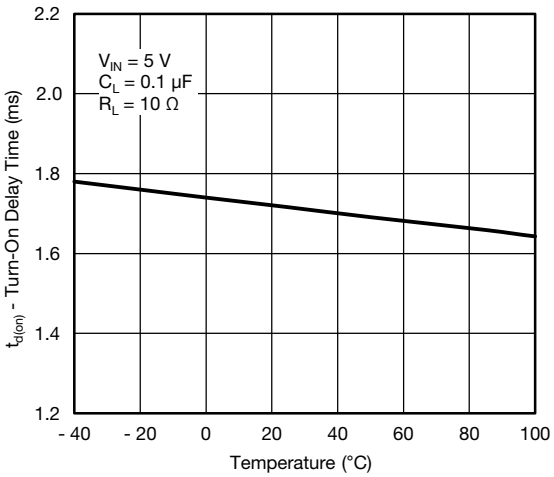


Fig. 18 - Turn-On Delay Time vs. Temperature

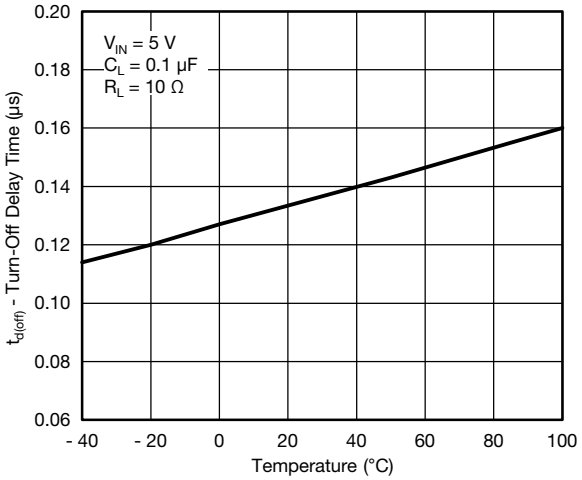


Fig. 19 - Turn-Off Delay Time vs. Temperature

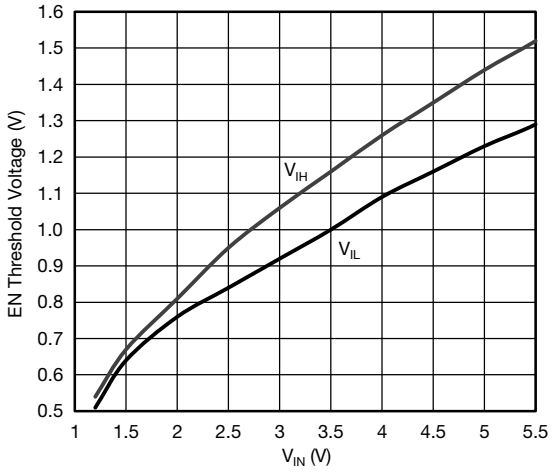


Fig. 20 - EN Threshold Voltage vs. Input Voltage

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TYPICAL WAVEFORMS

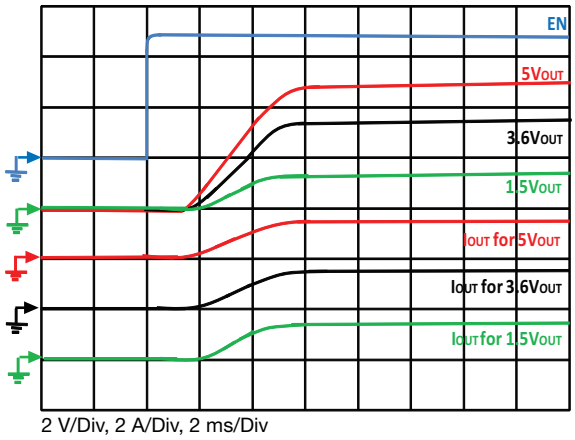


Fig. 21 - Typical Turn-on Delay, Rise Time
C_{OUT} = 0.1 µF, C_{IN} = 4.7 µF, I_{OUT} = 1.5 A

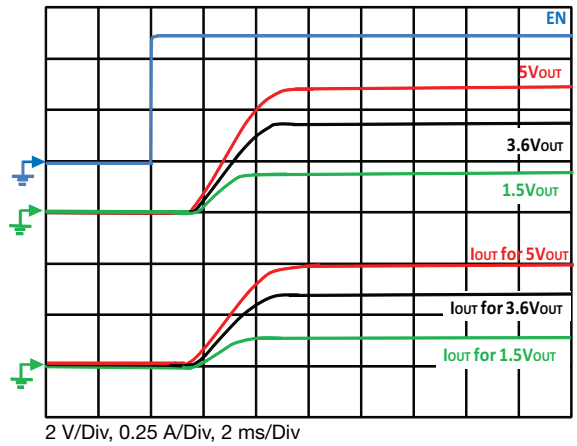


Fig. 22 - Typical Turn-on Delay, Rise Time
C_{OUT} = 0.1 µF, C_{IN} = 4.7 µF, R_{OUT} = 10 Ω

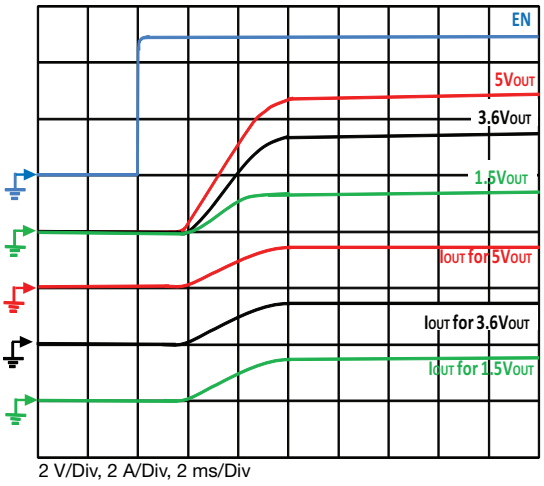


Fig. 23 - Typical Turn-on Delay, Rise Time
C_{OUT} = 200 µF, C_{IN} = 4.7 µF, I_{OUT} = 1.5 A

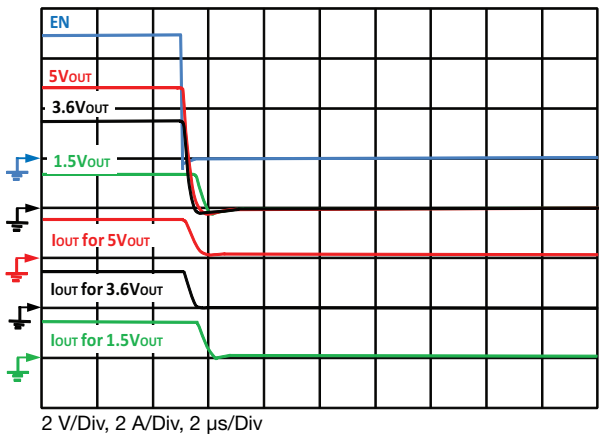


Fig. 24 - Typical Fall Time
C_{OUT} = 0.1 µF, C_{IN} = 4.7 µF, I_{OUT} = 1.5 A

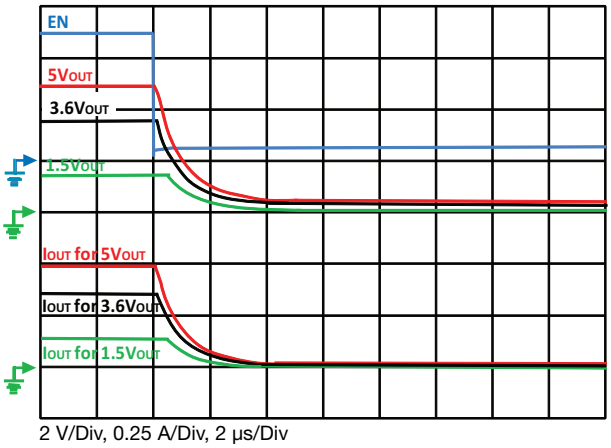


Fig. 25 - Typical Fall Time
C_{OUT} = 0.1 µF, C_{IN} = 4.7 µF, R_{OUT} = 10 Ω

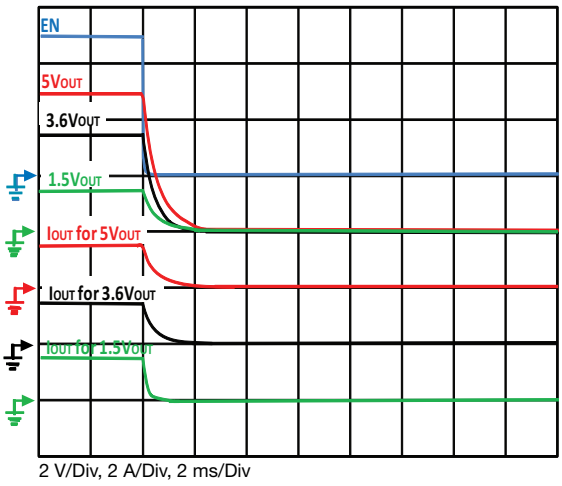


Fig. 26 - Typical Fall Time
C_{OUT} = 200 µF, C_{IN} = 4.7 µF, I_{OUT} = 1.5 A

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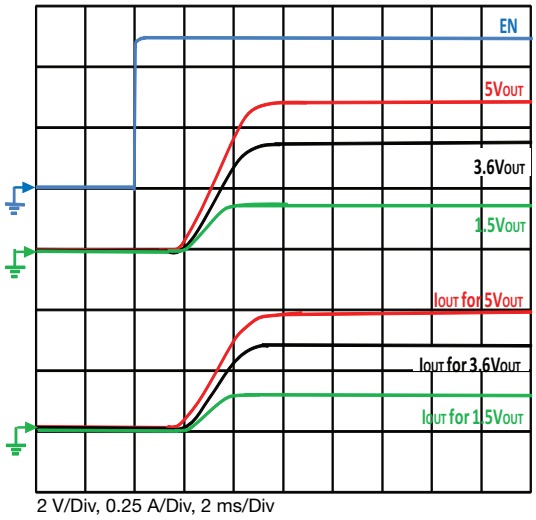


Fig. 27 - Typical Turn-on Delay, Rise Time
C_{OUT} = 200 µF, C_{IN} = 4.7 µF, R_{OUT} = 10 Ω

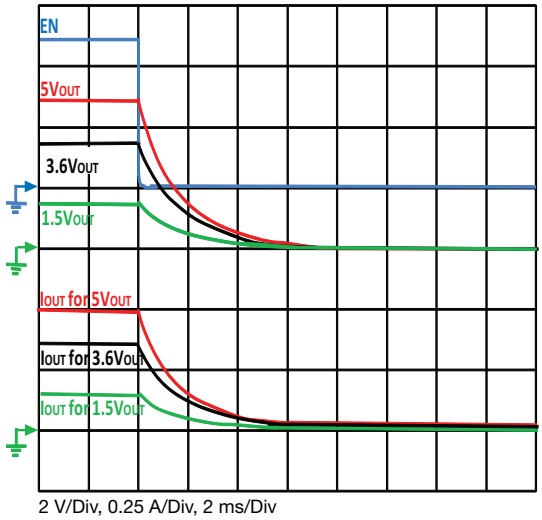


Fig. 28 - Typical Fall Time
C_{OUT} = 200 µF, C_{IN} = 4.7 µF, R_{OUT} = 10 Ω

DETAILED DESCRIPTION

SiP32408 and SiP32409 are advanced slew rate controlled high side load switches consisted of a n-channel power switch. When the device is enable the gate of the power switch is turned on at a controlled rate to avoid excessive in-rush current. Once fully on the gate to source voltage of the power switch is biased at a constant level. The design gives a flat on resistance throughout the operating voltages. When the device is off, the reverse blocking circuitry prevents current from flowing back to input if output is raised higher than input. The reverse blocking mechanism also works in case of no input applied.

APPLICATION INFORMATION

Input Capacitor

SiP32408 and SiP32409 do not require an input capacitor. To limit the voltage drop on the input supply caused by transient inrush currents, an input bypass capacitor is recommended. A 2.2 µF ceramic capacitor placed as close to the V_{IN} and GND should be enough. Higher values capacitor can help to further reduce the voltage drop. Ceramic capacitors are recommended for their ability to withstand input current surge from low impedance sources such as batteries in portable devices.

Output Capacitor

While these devices works without an output capacitor, an 0.1 µF or larger capacitor across V_{OUT} and GND is recommended to accommodate load transient condition. It also help to prevent parasitic inductance forces V_{OUT} below GND when switching off. Output capacitor has minimal affect on device's turn on slew rate time. There is no requirement on capacitor type and its ESR.

Enable

The EN pin is compatible with both TTL and CMOS logic voltage levels. Enable pin voltage can be above IN once it is within the absolute maximum rating range.
For output voltage slew rate control, EN is required to have at least 50 µs delay after the input voltage get ready to enable the device.

Protection Against Reverse Voltage Condition

SiP32408 and SiP32409 contain a reverse blocking circuitry to protect the current from going to the input from the output in case where the output voltage is higher than the input voltage when the main switch is off. Reverse blocking works for input voltage as low as 0 V.

Thermal Considerations

SiP32408 and SiP32409 are designed to maintain a constant output load current. Due to physical limitations of the layout and assembly of the device the maximum switch current is 3.5 A, as stated in the Absolute Maximum Ratings table. However, another limiting characteristic for the safe operating load current is the thermal power dissipation of the package. To obtain the highest power dissipation (and a thermal resistance of 170 °C/W) the power pad of the device should be connected to a heat sink on the printed circuit board. Fig. 21 shows a typical PCB layout. All copper traces and vias for the in and out pins should be sized adequately to carry the maximum continuous current.
The maximum power dissipation in any application is dependent on the maximum junction temperature, $T_{J(max.)}$ = 125 °C, the junction-to-ambient thermal resistance for the TDFN4 1.2 mm x 1.6 mm package, θ_{J-A} = 170 °C/W, and the ambient temperature, T_A, which may be formulaically expressed as:

$$P\ (max.) = \frac{T_J\ (max.) - T_A}{\theta_{J-A}} = \frac{125 - T_A}{170}$$

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It then follows that, assuming an ambient temperature of 70 °C, the maximum power dissipation will be limited to about 324 mW.

So long as the load current is below the 3.5 A limit, the maximum continuous switch current becomes a function of two things: the package power dissipation and the $R_{DS(on)}$ at the ambient temperature.

As an example let us calculate the worst case maximum load current at T_A = 70 °C. The worst case $R_{DS(on)}$ at 25 °C occurs at an input voltage of 1.2 V and is equal to 52 mΩ. The $R_{DS(on)}$ at 70 °C can be extrapolated from this data using the following formula:

$R_{DS(on)}$ (at 70 °C) = $R_{DS(on)}$ (at 25 °C) x (1 + T_C x DT)

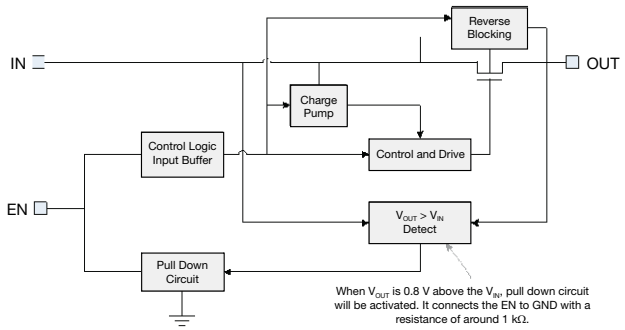
Where T_C is 3300 ppm/°C. Continuing with the calculation we have

$R_{DS(on)}$ (at 70 °C) = 52 mΩ x (1 + 0.0033 x (70 °C - 25 °C)) = 60 mΩ

The maximum current limit is then determined by

$$I_{LOAD}\,(max.) < \sqrt{\frac{P\,(max.)}{R_{DS(ON)}}}$$

which in this case is 2.3 A. Under the stated input voltage condition, if the 2.3 A current limit is exceeded the internal die temperature will rise and eventually, possibly damage the device.

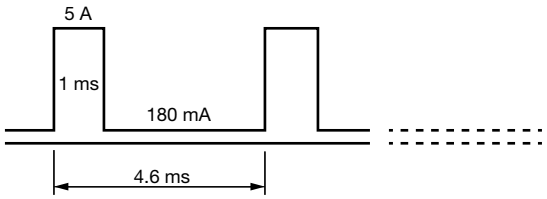


Active EN Pull Down for Reverse Blocking

When an internal circuit detects the condition of V_{OUT} 0.8 V higher than V_{IN}, it will turn on the pull down circuit connected to EN, forcing the switching off. The pull down value is about 1 kΩ.

Pulse Current Capability

The device is mounted on the evaluation board shown in the PCB layout section. It is loaded with pulses of 5 A and 1 ms for periods of 4.6 ms.



SiP32408 and SiP32409 can safely support 5 A pulse current repetitively at 25 °C.

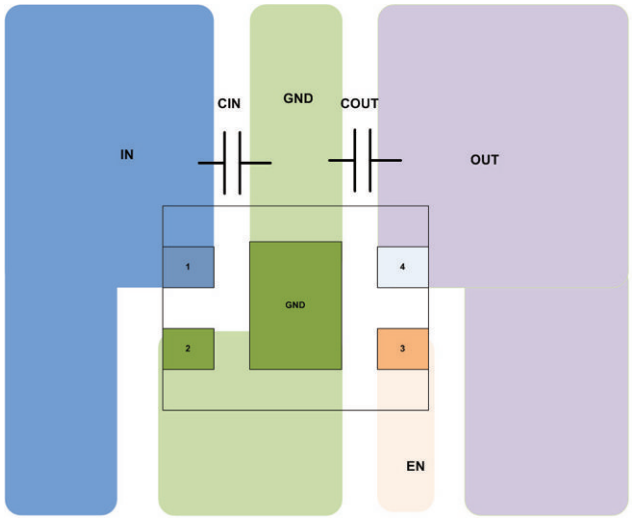
Switch Non-Repetitive Pulsed Current

SiP32408 and SiP32409 can withstand inrush current of up to 12 A for 100 µs at 25 °C when heavy capacitive loads are connected and the part is already enabled.

Recommended Board Layout

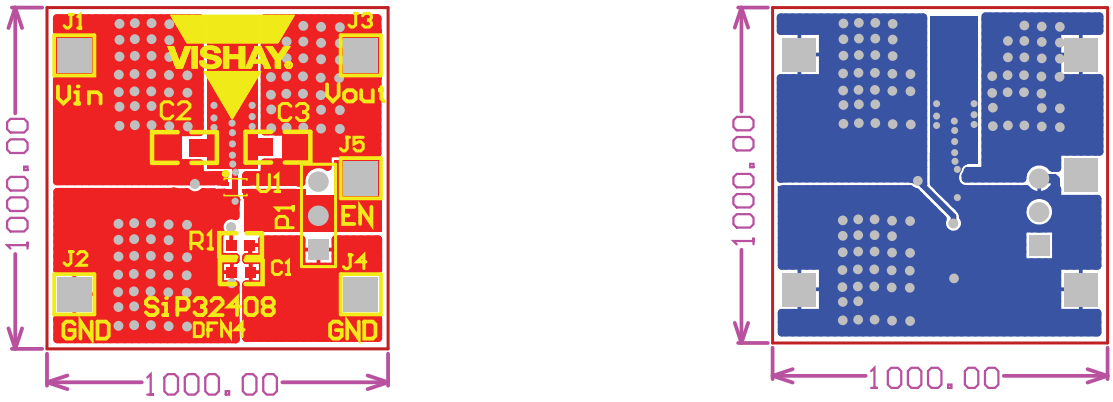
For the best performance, all traces should be as short as possible to minimize the inductance and parasitic effects. The input and output capacitors should be kept as close as possible to the input and output pins respectively.

Connecting the central exposed pad to GND, using wide traces for input, output, and GND help reducing the case to ambient thermal impedance.



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EVALUATION BOARD LAYOUT



Top

Bottom

Fig. 29 - Evaluation board Layout for TDFN4 1.2 mm x 1.6 mm (type: FR4, size: 1" x 1", thickness: 0.062", copper thickness: 2 oz.)

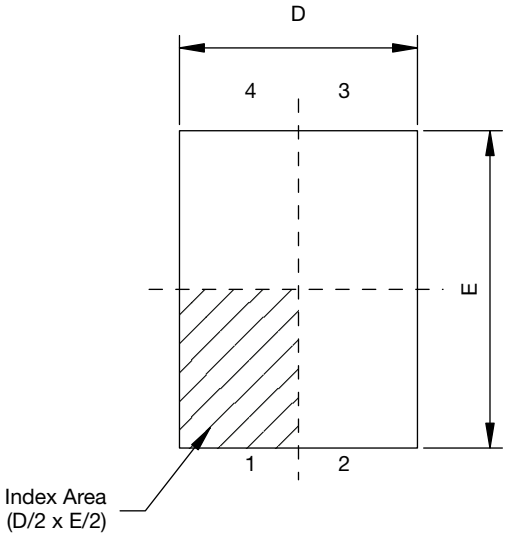
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PRODUCT SUMMARY		
Part number	SiP32408	SiP32409
Description	1.1 V to 5.5 V, 42 mΩ, 2.5 ms rise time, bidirectional off isolation	1.1 V to 5.5 V, 42 mΩ, 2.5 ms rise time, bidirectional off isolation, output discharge
Configuration	Single	Single
Slew rate time (µs)	2500	2500
On delay time (µs)	1800	1800
Input voltage min. (V)	1.1	1.1
Input voltage max. (V)	5.5	5.5
On-resistance at input voltage min. (mΩ)	45	45
On-resistance at input voltage max. (mΩ)	42	42
Quiescent current at input voltage min. (µA)	10.5	10.5
Quiescent current at input voltage max. (µA)	105	105
Output discharge (yes / no)	No	Yes
Reverse blocking (yes / no)	Yes	Yes
Continuous current (A)	3.5	3.5
Package type	TDFN4	TDFN4
Package size (W, L, H) (mm)	1.2 x 1.6 x 0.5	1.2 x 1.6 x 0.5
Status code	2	2
Product type	Slew rate	Slew rate
Applications	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable

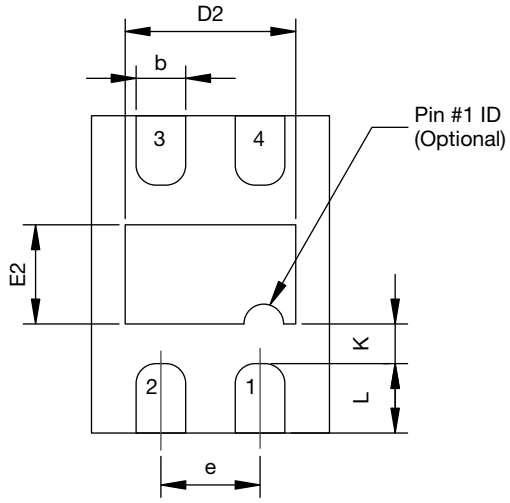
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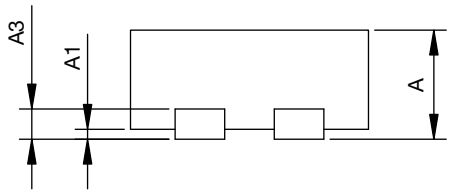
TDFN4 1.2 x 1.6 Case Outline



Top View



Bottom View



Side View

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.45	0.55	0.60	0.017	0.022	0.024
A1	0.00	-	0.05	0.00	-	0.002
A3	0.15 REF. or 0.127 REF. (1)			0.006 or 0.005 (1)		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.15	1.20	1.25	0.045	0.047	0.049
D2	0.81	0.86	0.91	0.032	0.034	0.036
e	0.50 BSC			0.020		
E	1.55	1.60	1.65	0.061	0.063	0.065
E2	0.45	0.50	0.55	0.018	0.020	0.022
K	0.25 typ.			0.010 typ.		
L	0.25	0.30	0.35	0.010	0.012	0.014
ECN: T16-0143-Rev. C, 18-Apr-16 DWG: 5995						

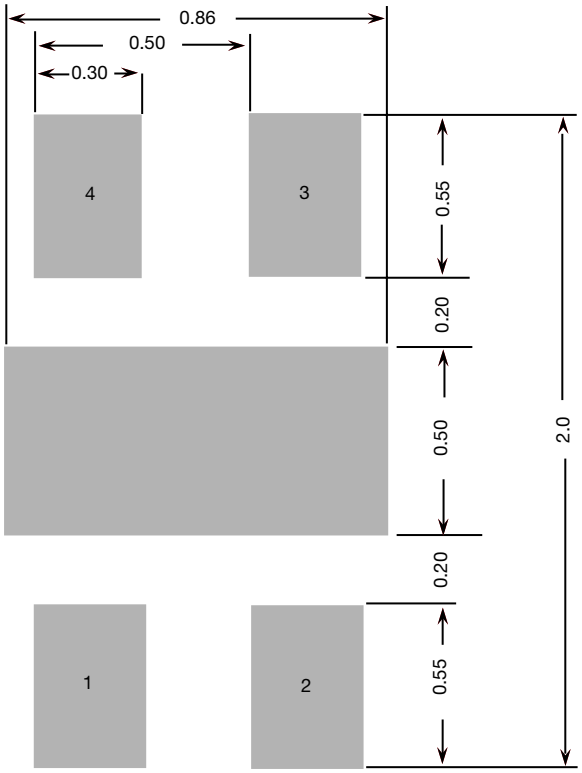
Note

(1) The dimension depends on the leadframe that assembly house used.

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RECOMMENDED MINIMUM PADS FOR TDFN4 1.2 x 1.6



Recommended Minimum Pads
Dimensions in mm

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