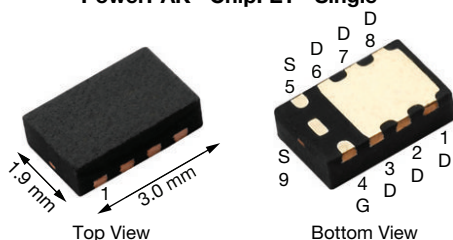


P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (TYP.)
-20	0.052 at V _{GS} = -4.5 V	-8 ^e	8
	0.082 at V _{GS} = -2.5 V	-7.5	

PowerPAK® ChipFET® Single



FEATURES

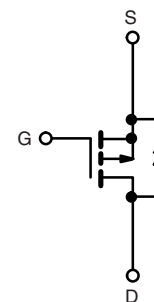
- TrenchFET® power MOSFET
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load switch
- HDD DC/DC



P-Channel MOSFET

Ordering Information:

Si5459DU-T1-GE3 (Lead (Pb)-free and halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{GS}	± 12	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	A
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Pulsed Drain Current (10 μs pulse width)	I _{DM}	-20	A
Source-Drain Current Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	-2.9 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	W
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-50 to 150	°C
Soldering Recommendations (Peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT		UNIT
		TYPICAL	MAXIMUM	
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	30	36	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	9.5	11.5	

Notes

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 72 °C/W.
- Package limited.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP. ^a	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-20	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = -250 μA	-	-19	-	mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	3.1	-	
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.6	-	-1.4	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	-	-	-100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = ≤ -5 V, V _{GS} = -10 V	-20	-	-	A
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -6.7 A	-	0.043	0.052	Ω
		V _{GS} = -2.5 V, I _D = -1 A	-	0.068	0.082	
Forward Transconductance ^b	g _{fs}	V _{DS} = -10 V, I _D = -6.7 A	-	11	-	S
Dynamic ^a						
Input Capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	-	665	-	pF
Output Capacitance	C _{oss}		-	140	-	
Reverse Transfer Capacitance	C _{rss}		-	115	-	
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -10 V, I _D = -6.7 A	-	17	26	nC
		V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -6.7 A	-	8	12	
Gate-Source Charge	Q _{gs}		-	2	-	
Gate-Drain Charge	Q _{gd}		-	3	-	
Gate Resistance	R _g	f = 1 MHz	1.2	6	12	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 1.9 Ω I _D ≅ -5.3 A, V _{GEN} = -10 V, R _g = 1 Ω	-	6	12	ns
Rise Time	t _r		-	15	23	
Turn-Off Delay Time	t _{d(off)}		-	26	39	
Fall Time	t _f		-	9	18	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 1.9 Ω I _D ≅ -5.3 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	21	32	
Rise Time	t _r		-	50	75	
Turn-Off Delay Time	t _{d(off)}		-	29	44	
Fall Time	t _f		-	13	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	-8	A
Pulse Diode Forward Current ^a	I _{SM}		-	-	-20	
Body Diode Voltage	V _{SD}	I _S = -5.3 A	-	-0.77	-1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = -5.3 A, dI/dt = 100 A/μs, T _J = 25 °C	-	30	45	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	17	26	nC
Reverse Recovery Fall Time	t _a		-	16	-	ns
Reverse Recovery Rise Time	t _b		-	14	-	

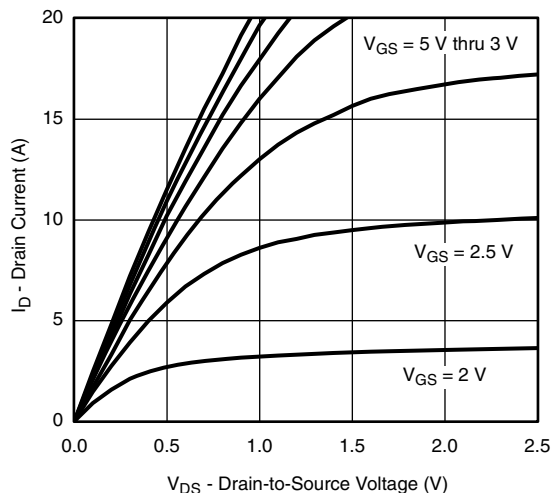
Notes

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

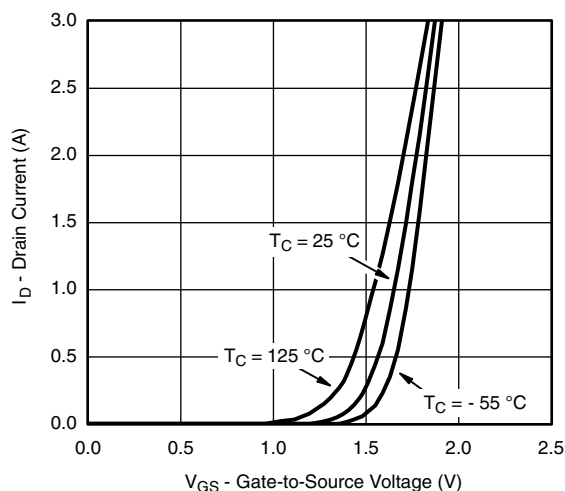
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



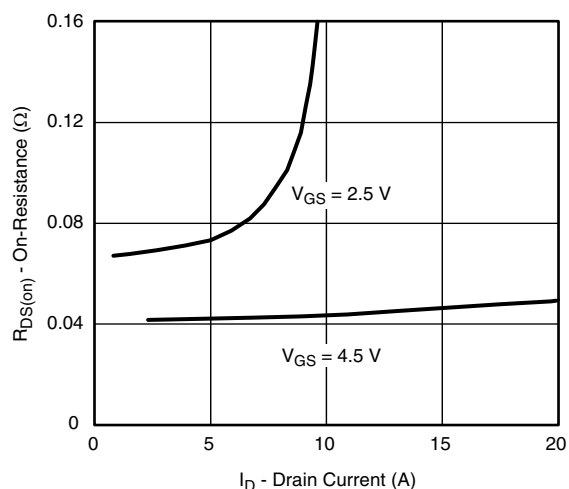
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



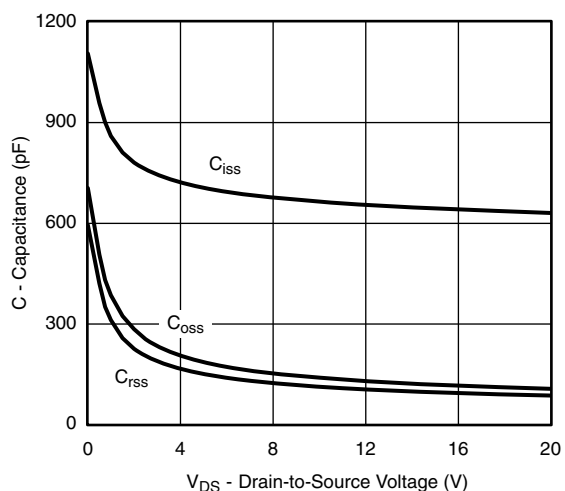
Output Characteristics



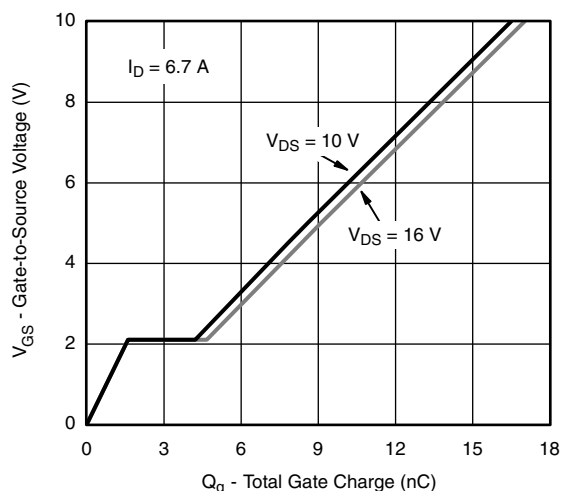
Transfer Characteristics



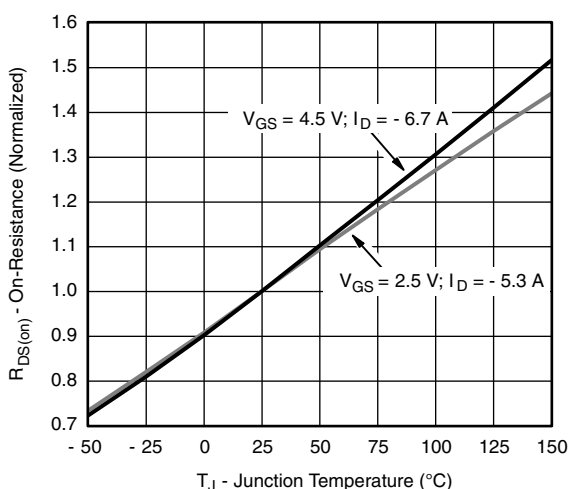
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



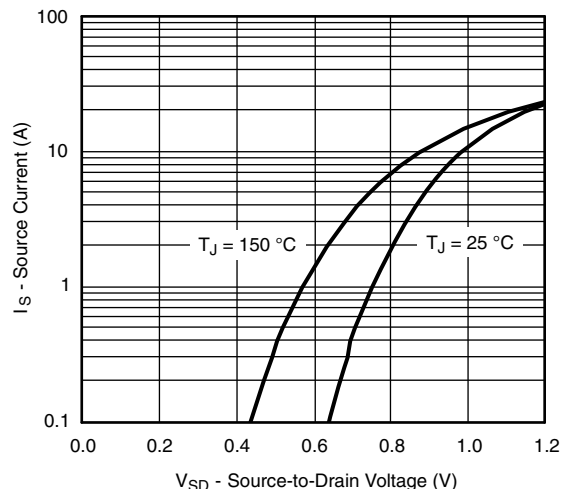
Gate Charge



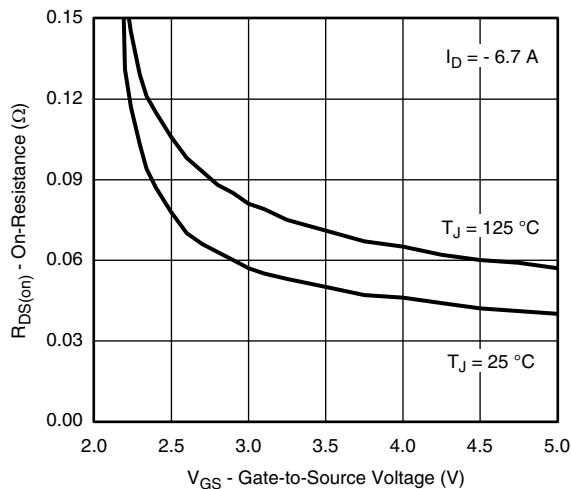
On-Resistance vs. Junction Temperature



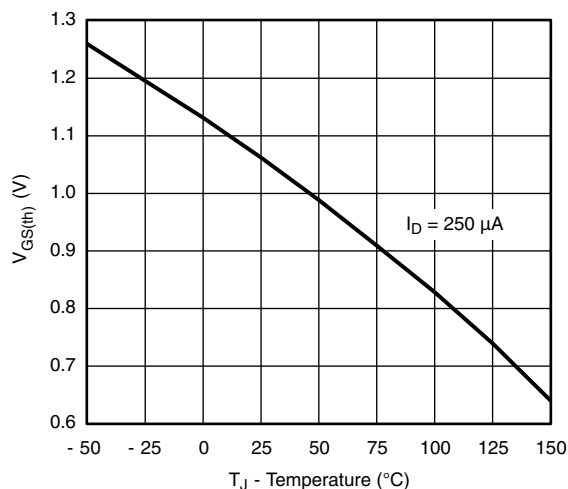
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



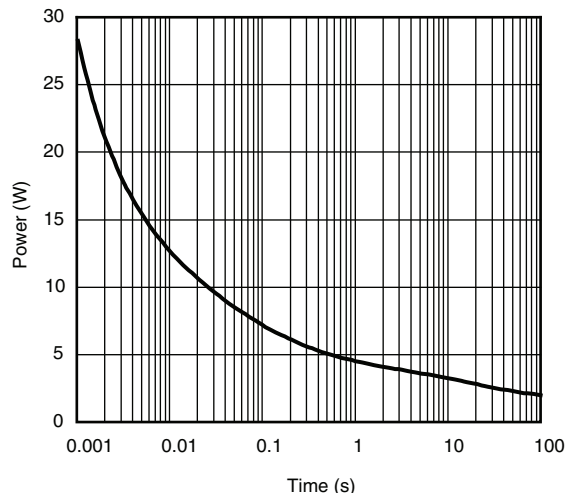
Source-Drain Diode Forward Voltage



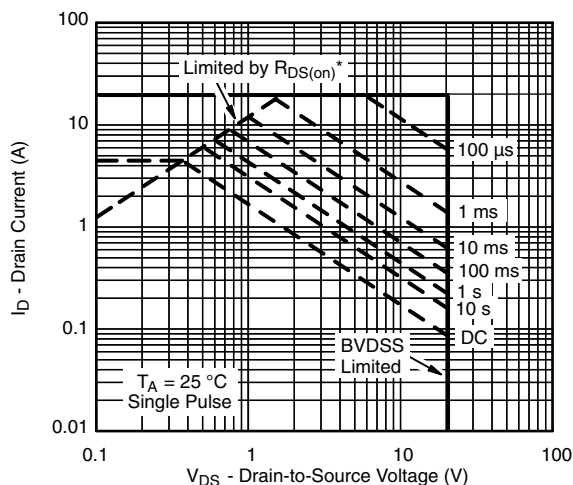
On-Resistance vs. Gate-to-Source Voltage



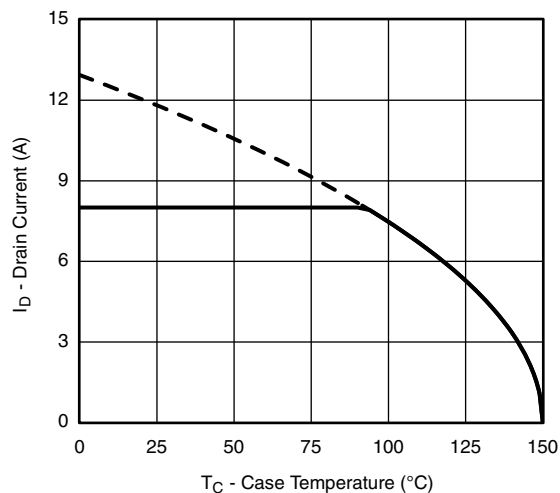
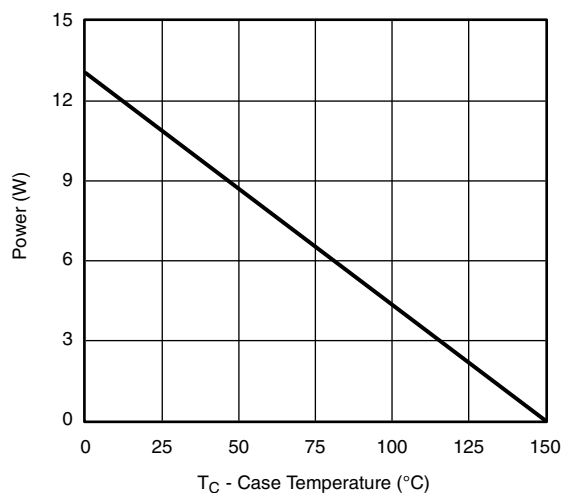
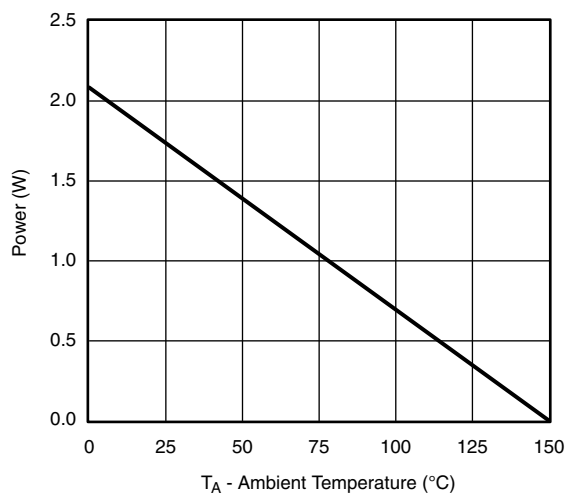
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



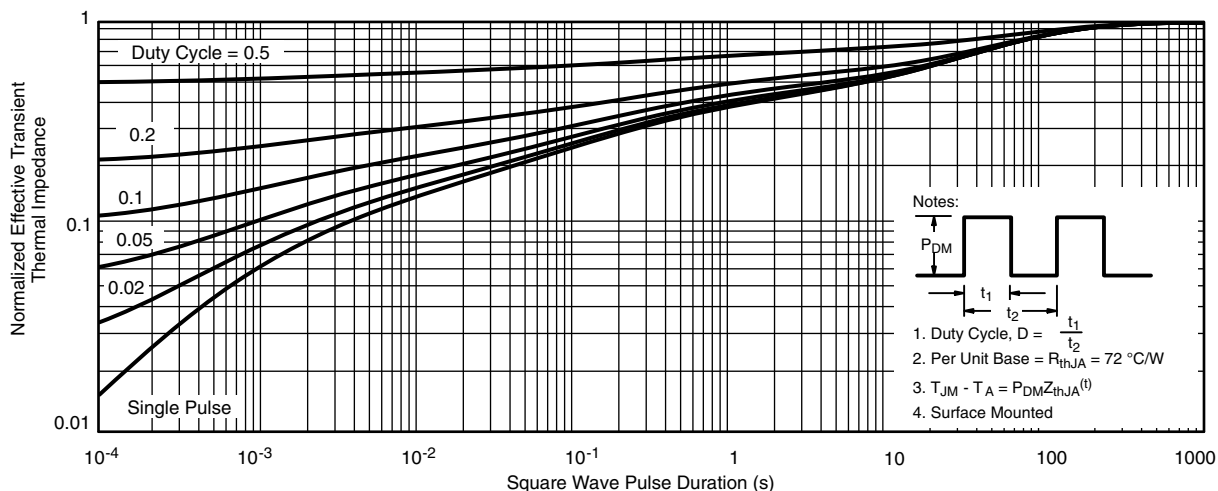
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power Derating, Junction-to-Case

Power Derating, Junction-to-Ambient
Note

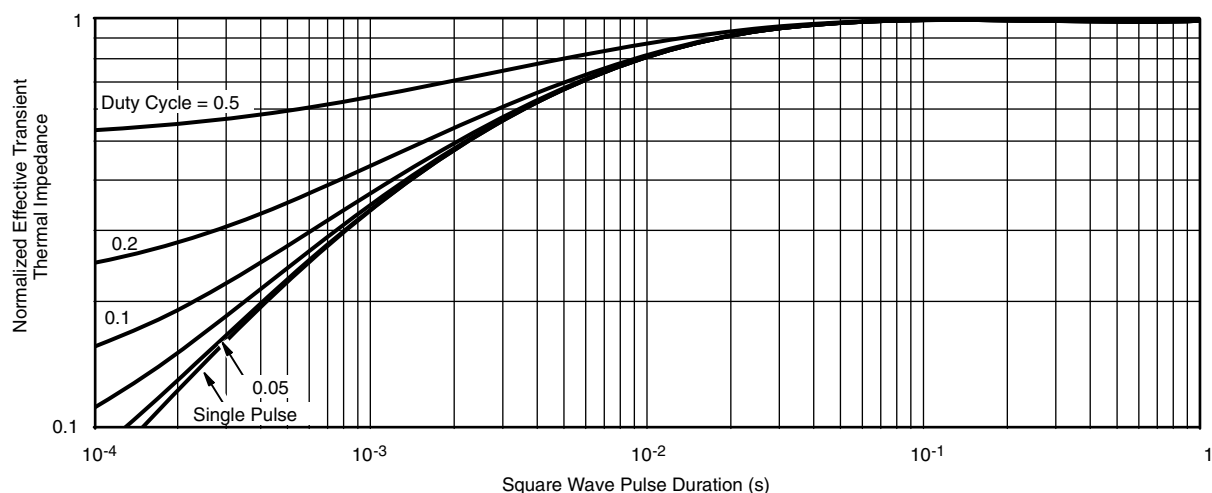
- a. The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



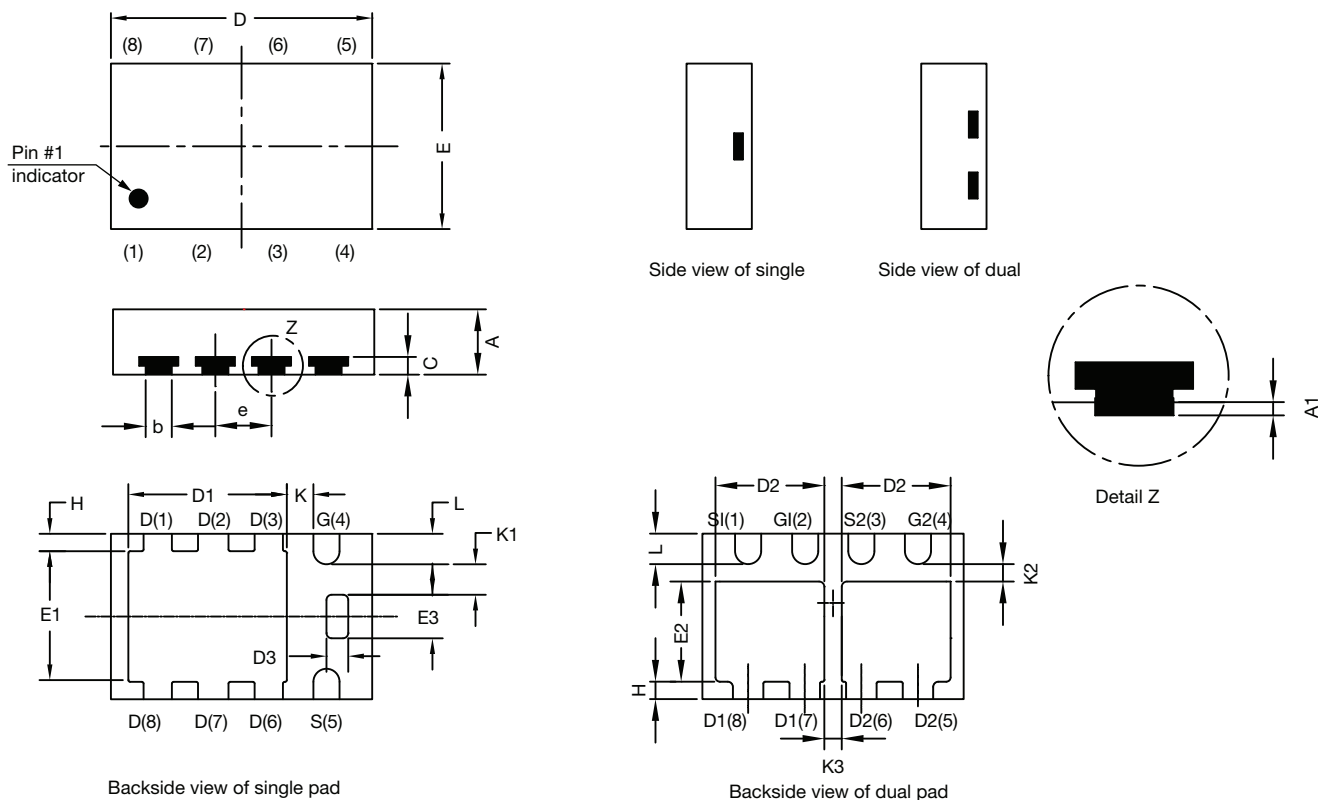
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65017.

PowerPAK® ChipFET® Case Outline

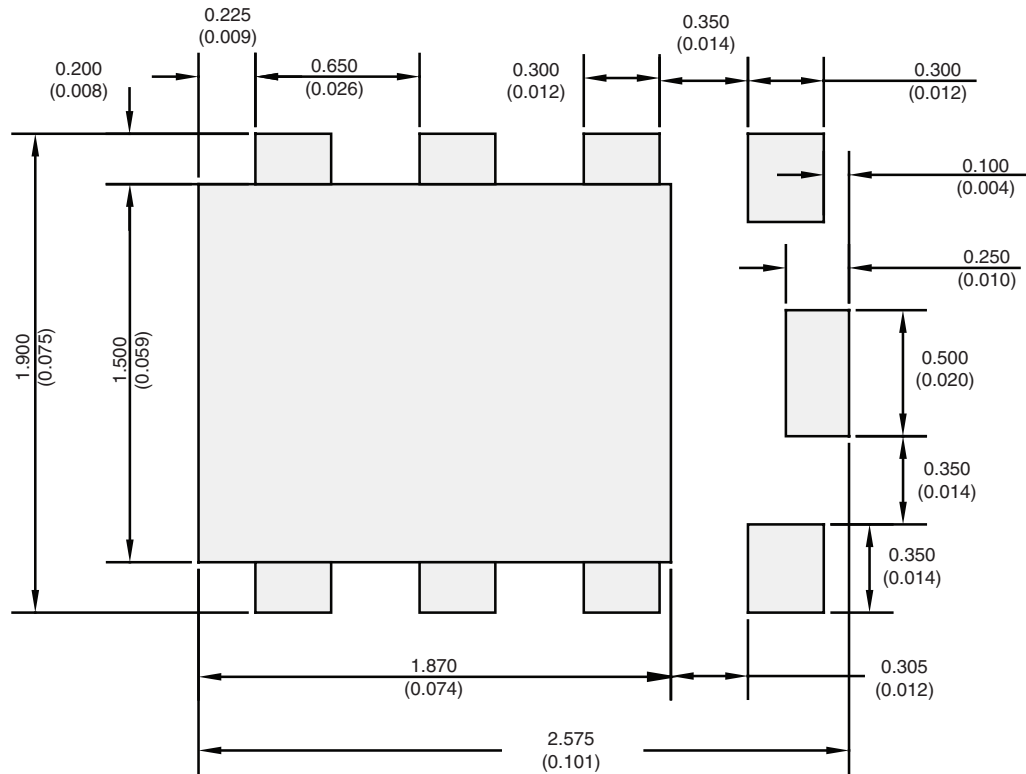


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D1	1.75	1.87	2.00	0.069	0.074	0.079
D2	1.07	1.20	1.32	0.042	0.047	0.052
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E1	1.38	1.50	1.63	0.054	0.059	0.064
E2	0.92	1.05	1.17	0.036	0.041	0.046
E3	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
K2	0.20	-	-	0.008	-	-
K3	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
C14-0630-Rev. E, 21-Jul-14						
DWG: 5940						

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads
Dimensions in mm/(Inches)

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