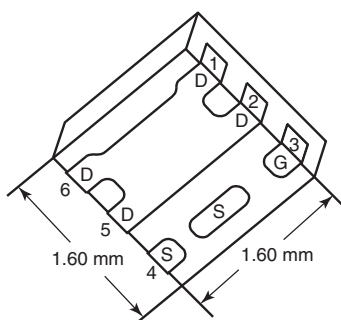


## N-Channel 12 V (D-S) MOSFET

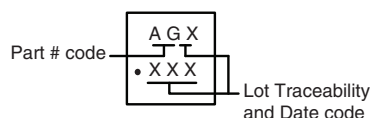
### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
12	0.020 at $V_{GS} = 4.5$ V	9	7.5 nC
	0.024 at $V_{GS} = 2.5$ V	9	
	0.029 at $V_{GS} = 1.8$ V	9	

PowerPAK SC-75-6L-Single



### Marking Code



Ordering Information: SiB488DK-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

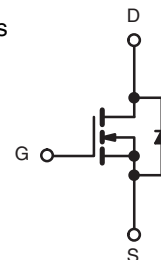
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- New Thermally Enhanced PowerPAK<sup>®</sup> SC-75 Package
  - Small Footprint Area
  - Low On-Resistance
- 100 %  $R_g$  Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Load Switch, PA Switch and Battery Switch for Portable Devices
- High Frequency dc-to-dc Converters



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	12	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	
Continuous Drain Current ( $T_J = 150$ °C)	$T_C = 25$ °C	$9^a$	A
	$T_C = 70$ °C	$9^a$	
	$T_A = 25$ °C	$9^{b,c}$	
	$T_A = 70$ °C	$7.2^{b,c}$	
Pulsed Drain Current	$I_{DM}$	35	W
Continuous Source-Drain Diode Current	$T_C = 25$ °C	$9^a$	
	$T_A = 25$ °C	$2^{b,c}$	
Maximum Power Dissipation	$T_C = 25$ °C	13	W
	$T_C = 70$ °C	8.4	
	$T_A = 25$ °C	$2.4^{b,c}$	
	$T_A = 70$ °C	$1.6^{b,c}$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	$R_{thJA}$	41	51	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	7.5	9.5	

Notes:

- $T_C = 25$  °C, package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$  s.
- See Solder Profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 105 °C/W.

**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	12			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		11		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 2.7		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.4		1.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 12 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 12 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 4.5 V	15			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.3 A		0.016	0.020	Ω
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 5.8 A		0.019	0.024	
		V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 2.5 A		0.023	0.029	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 6.3 A		32		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 6 V, V <sub>GS</sub> = 0 V, f = 1 MHz		725		pF
Output Capacitance	C <sub>oss</sub>			195		
Reverse Transfer Capacitance	C <sub>rss</sub>			90		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 6 V, V <sub>GS</sub> = 8 V, I <sub>D</sub> = 9 A		13.1	20	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 6 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9 A		7.5	12	
Gate-Drain Charge	Q <sub>gd</sub>			1.1		
Gate Resistance	R <sub>g</sub>			0.8		
Turn-On Delay Time	t <sub>d(on)</sub>	f = 1 MHz	0.5	2.5	5	Ω
Rise Time	t <sub>r</sub>	V <sub>DD</sub> = 6 V, R <sub>L</sub> = 0.83 Ω I <sub>D</sub> ≅ 7.2 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		10	15	ns
Turn-Off Delay Time	t <sub>d(off)</sub>			10	15	
Fall Time	t <sub>f</sub>			20	30	
Turn-On Delay Time	t <sub>d(on)</sub>			10	15	
Rise Time	t <sub>r</sub>	V <sub>DD</sub> = 6 V, R <sub>L</sub> = 0.83 Ω I <sub>D</sub> ≅ 7.2 A, V <sub>GEN</sub> = 8 V, R <sub>g</sub> = 1 Ω		5	10	
Turn-Off Delay Time	t <sub>d(off)</sub>			10	15	
Fall Time	t <sub>f</sub>			20	30	
Fall Time	t <sub>f</sub>			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			9	A
Pulse Diode Forward Current	I <sub>SM</sub>				35	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 7.2 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 7.2 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		15	30	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			4	8	nC
Reverse Recovery Fall Time	t <sub>a</sub>			8		ns
Reverse Recovery Rise Time	t <sub>b</sub>			7		

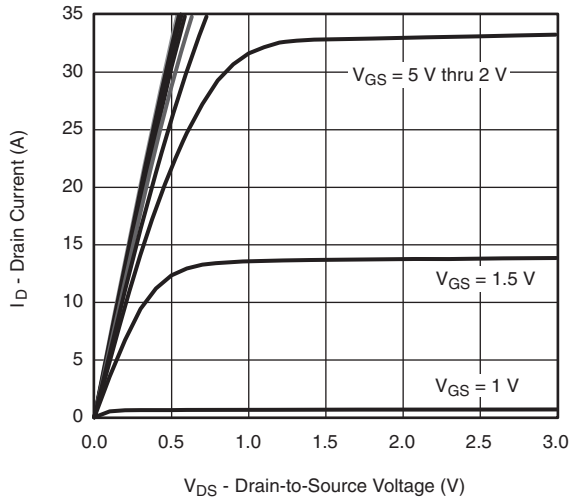
Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

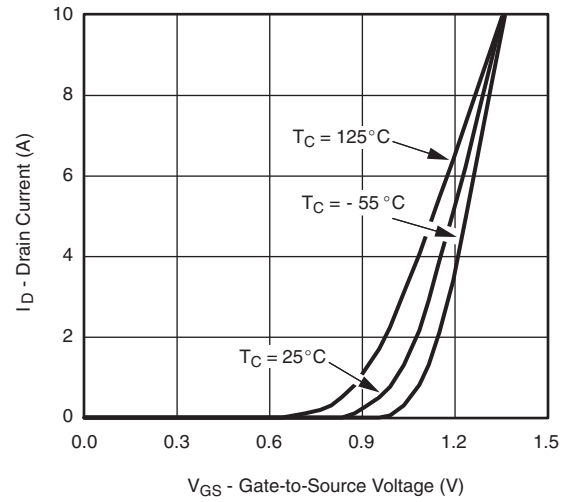
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

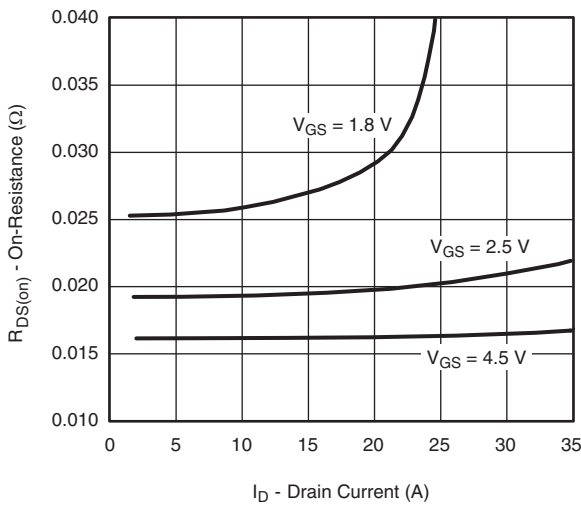
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



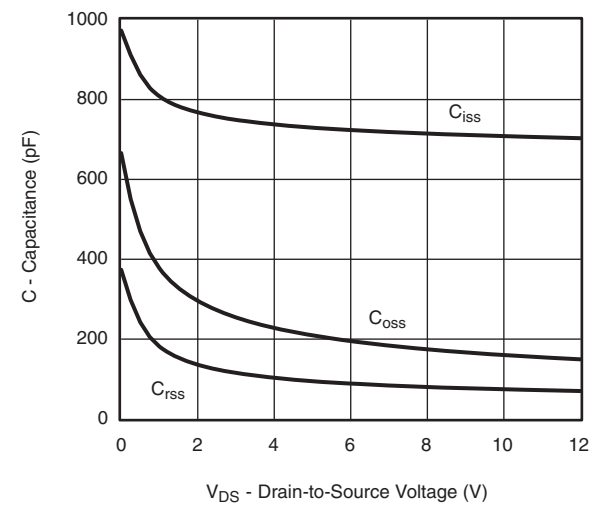
Output Characteristics



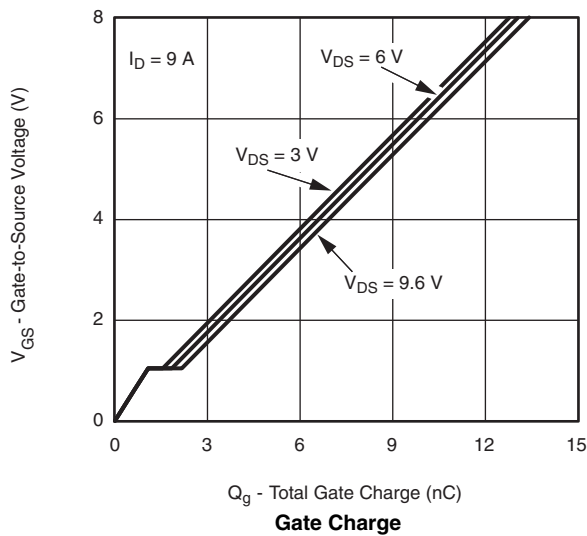
Transfer Characteristics



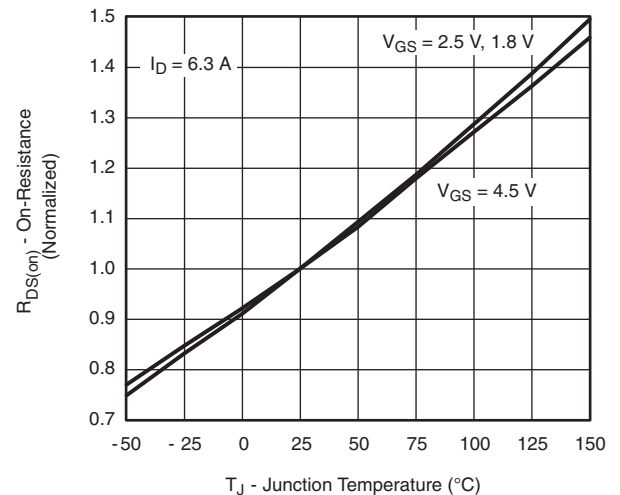
On-Resistance vs. Drain Current and Gate Voltage



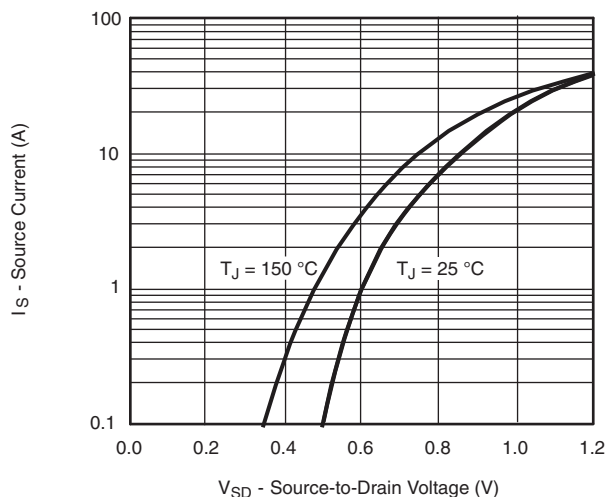
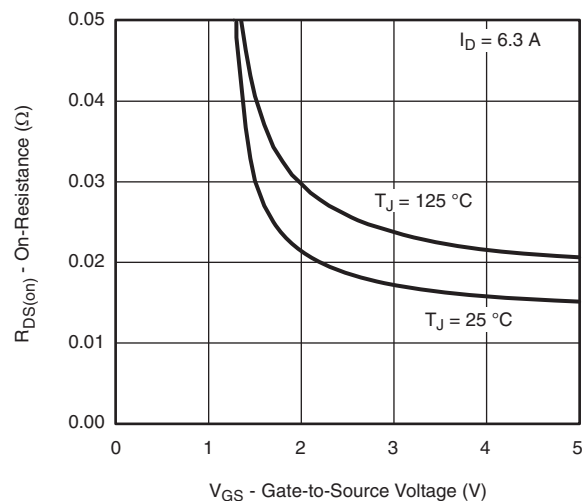
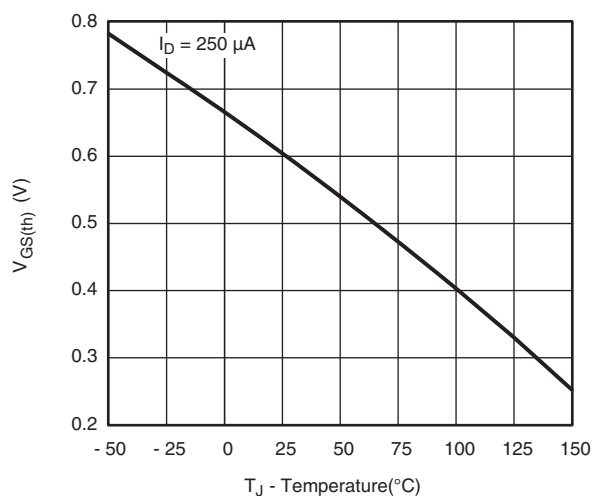
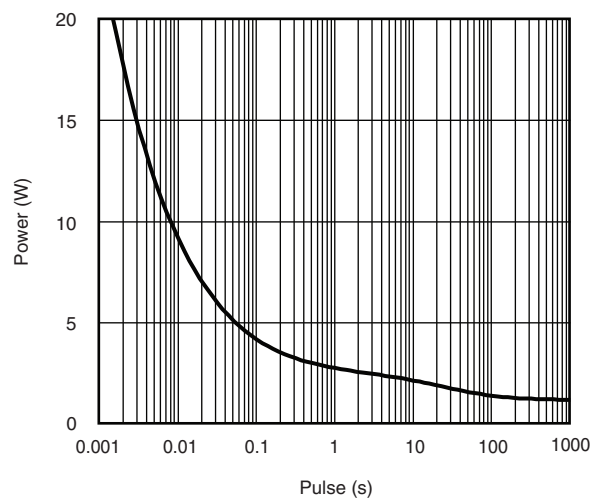
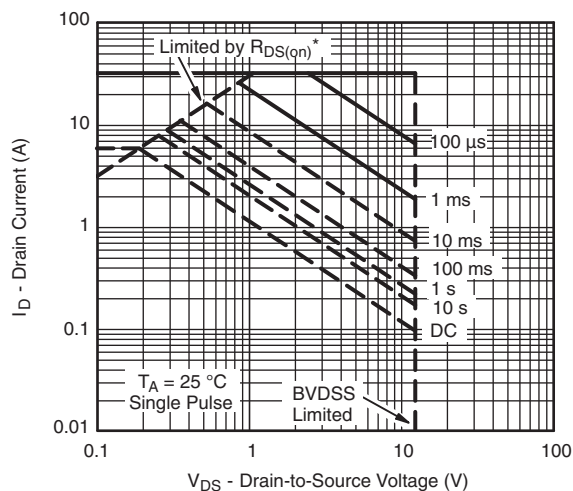
Capacitance



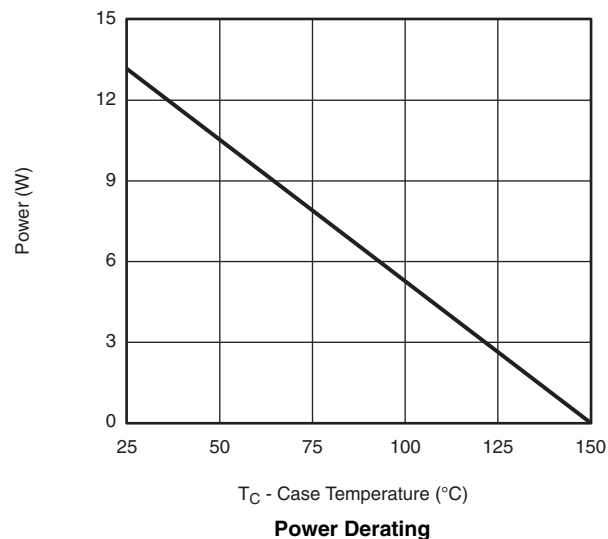
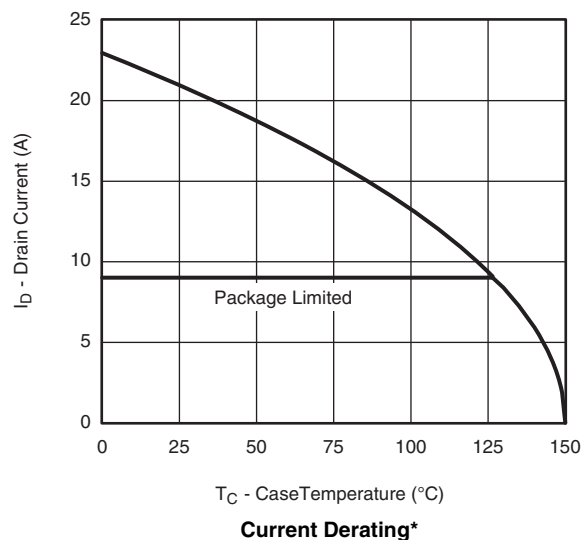
Gate Charge



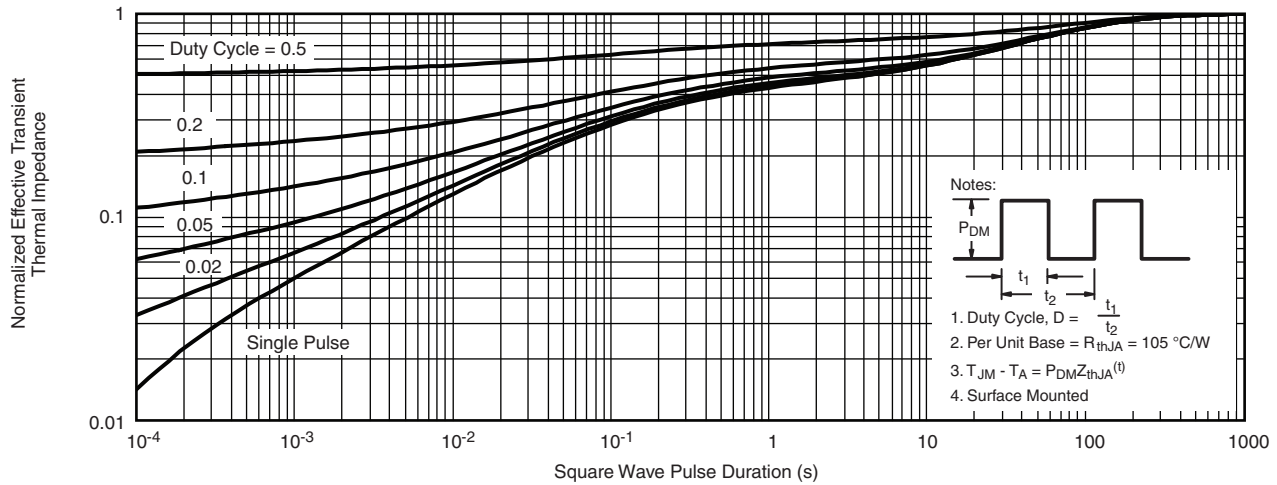
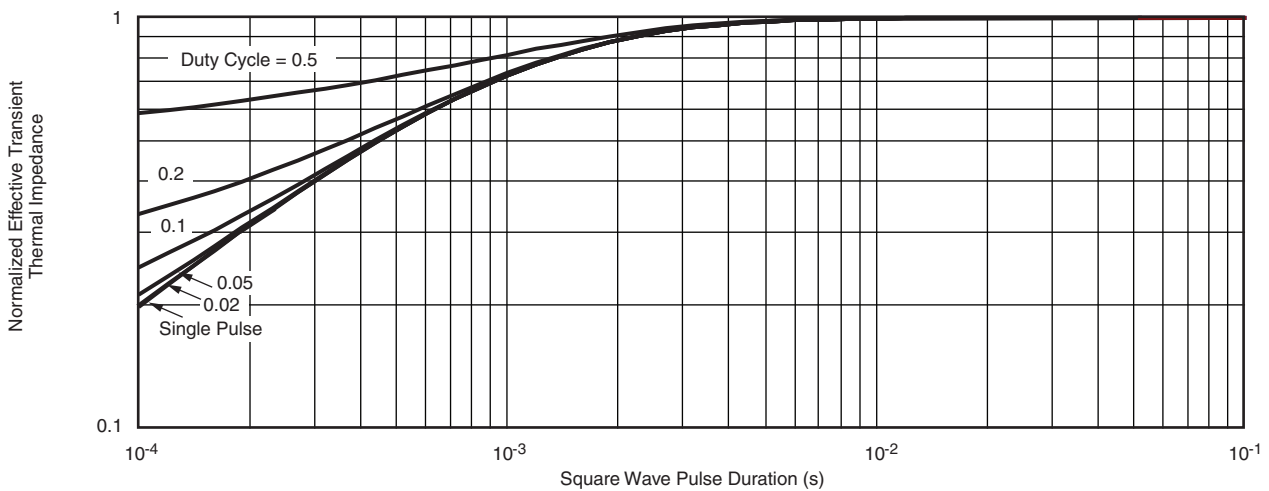
On-Resistance vs. Junction Temperature

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient**\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified**Safe Operating Area, Junction-to-Ambient**

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



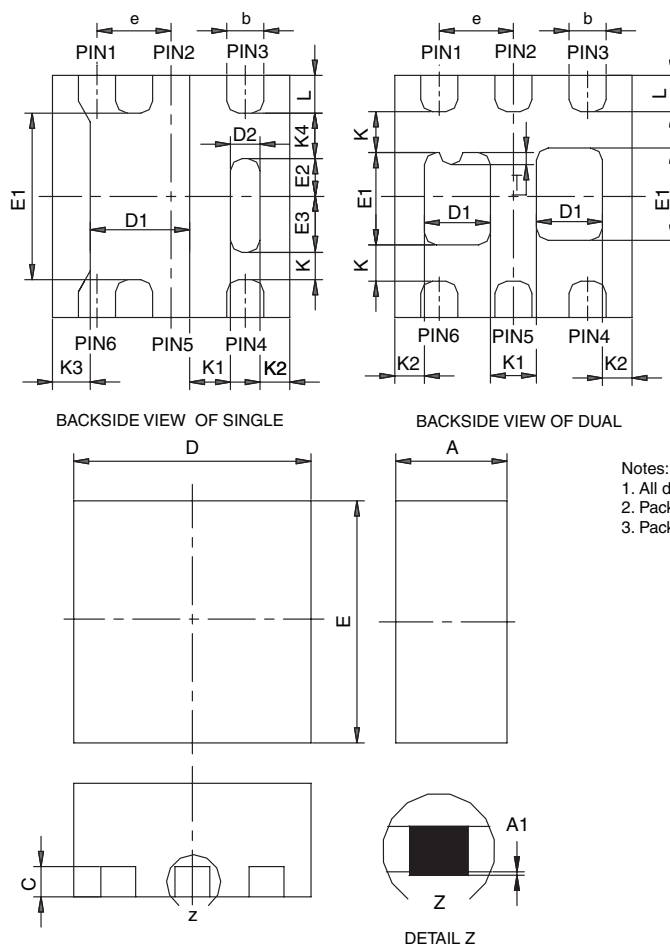
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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### PowerPAK® SC75-6L



- Notes:
1. All dimensions are in millimeters
  2. Package outline exclusive of mold flash and metal burr
  3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

ECN: C-07431 – Rev. C, 06-Aug-07  
DWG: 5935

Technical drawing of a mechanical part, likely a bracket or support, showing dimensions in mm and inches. The drawing includes a central rectangular feature with a circular hole, and several smaller rectangular features (possibly mounting tabs or holes) positioned around it. Dimensions are provided for overall size, hole placement, and feature spacing.

Dimensions (mm / inches):

- Overall width: 2.000 (0.079)
- Overall height: 1.700 (0.067)
- Central hole diameter: 0.250 (0.01)
- Central hole offset from left edge: 0.250 (0.01)
- Central hole offset from right edge: 0.250 (0.01)
- Central hole offset from top edge: 0.300 (0.012)
- Central hole offset from bottom edge: 0.300 (0.012)
- Top feature width: 0.500 (0.02)
- Top feature offset from left edge: 0.250 (0.01)
- Top feature offset from right edge: 0.250 (0.01)
- Top feature offset from top edge: 0.300 (0.012)
- Bottom feature width: 0.500 (0.02)
- Bottom feature offset from left edge: 0.250 (0.01)
- Bottom feature offset from right edge: 0.250 (0.01)
- Bottom feature offset from bottom edge: 0.300 (0.012)
- Left feature width: 0.370 (0.015)
- Left feature offset from left edge: 0.180 (0.007)
- Left feature offset from top edge: 0.300 (0.012)
- Left feature offset from bottom edge: 0.300 (0.012)
- Right feature width: 0.370 (0.015)
- Right feature offset from right edge: 0.180 (0.007)
- Right feature offset from top edge: 0.300 (0.012)
- Right feature offset from bottom edge: 0.300 (0.012)
- Central hole diameter: 0.250 (0.01)
- Central hole offset from left edge: 0.250 (0.01)
- Central hole offset from right edge: 0.250 (0.01)
- Central hole offset from top edge: 0.300 (0.012)
- Central hole offset from bottom edge: 0.300 (0.012)

APPLICATION NOTE





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