Precision CMOS Analog Switches

DESCRIPTION

The DG417, DG418, DG419 monolithic CMOS analog switches were designed to provide high performance switching of analog signals. Combining low power, low leakages, high speed, low on-resistance and small physical size, the DG417 series is ideally suited for portable and battery powered industrial and military applications requiring high performance and efficient use of board space.

To achieve high-voltage ratings and superior switching performance, the DG417 series is built on Vishay Siliconix's high voltage silicon gate (HVSG) process. Break-before-make is guaranteed for the DG419, which is an SPDT configuration. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

The DG417 and DG418 respond to opposite control logic levels as shown in the truth table.

BENEFITS

- Wide dynamic range
- Low signal errors and distortion
- Break-before-make switching action
- Simple interfacing
- Reduced board space
- Improved reliability

FEATURES

- ± 15 V analog signal range
- On-resistance - $R_{DS(on)}$: 20 Ω
- Fast switching action - t_{on}: 100 ns
- Ultra low power requirements - P_D: 35 nW
- TTL and CMOS compatible
- MiniDIP and SOIC packaging
- 44 V supply max. rating

Pb-free

RoHS*
Available

Note

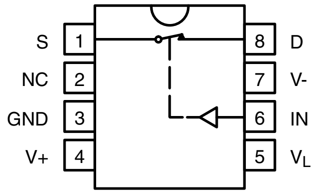
* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Precision test equipment
- Precision instrumentation
- Battery powered systems
- Sample-and-hold circuits
- Military radios
- Guidance and control systems
- Hard disk drives

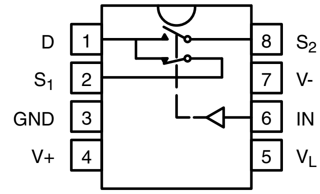
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG417
Dual-In-Line and SOIC



Top View

DG419
Dual-In-Line and SOIC



Top View

TRUTH TABLE		
LOGIC	**DG417**	**DG418**
0	On	Off
1	Off	On

Note

- Logic "0" ≤ 0.8 V
  Logic "1" ≥ 2.4 V

TRUTH TABLE DG419		
LOGIC	**SW_1**	**SW_2**
0	On	Off
1	Off	On

Note

- Logic "0" ≤ 0.8 V
  Logic "1" ≥ 2.4 V

ORDERING INFORMATION

TEMP. RANGE	PACKAGE	PART NUMBER
DG417, DG418		
-40 °C to +85 °C	8 pin plastic MiniDIP	DG417DJ DG417DJ-E3
		DG418DJ DG418DJ-E3
	8 pin narrow SOIC	DG417DY DG417DY-E3 DG417DY-T1 DG417DY-T1-E3
		DG418DY DG418DY-E3 DG418DY-T1 DG418DY-T1-E3
DG419		
-40 °C to +85 °C	8 pin plastic MiniDIP	DG419DJ DG419DJ-E3
	8 pin narrow SOIC	DG419DY DG419DY-E3 DG419DY-T1 DG419DY-T1-E3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER (VOLTAGES REFERENCED TO V-)		LIMIT	UNIT
V+		44	V
GND		25	
V_L		(GND - 0.3) to (V+) + 0.3	
Digital inputs [a], V_S, V_D		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Current (any terminal) continuous		30	mA
C, S or D (pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage temperature	(AK suffix)	-65 to +150	°C
	(DJ, DY suffix)	-65 to +125	
Power dissipation (package) [b]	8 pin plastic MiniDIP [c]	400	mW
	8 pin narrow SOIC [d]	400	
	8 pin CerDIP [e]	600	

Notes
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 6 mW/°C above 25 °C
d. Derate 6.5 mW/°C above 75 °C
e. Derate 12 mW/°C above 75 °C

SCHEMATIC DIAGRAM (typical channel)

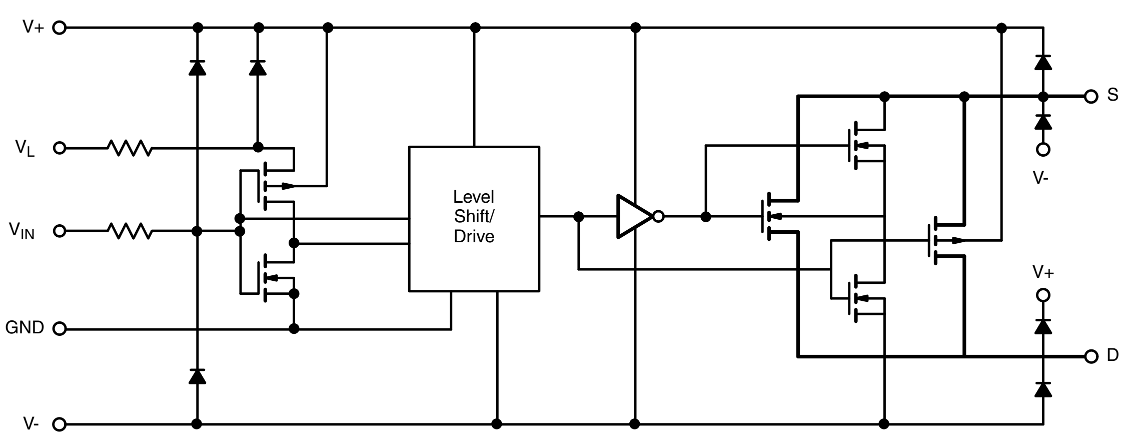


Fig. 1

SPECIFICATIONS [a]

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 15 V, V- = -15 V, V_L = 5 V, V_{IN} = 2.4 V, 0.8 V [f]		TEMP. [b]	TYP. [c]	A SUFFIX LIMITS -55 °C to +125 °C		D SUFFIX LIMITS -40 °C to +85 °C		UNIT
						MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Analog Switch										
Analog signal range [e]	V_{ANALOG}			Full	-	-15	15	-15	15	V
Drain-source on-resistance	$R_{DS(on)}$	I_S = -10 mA, V_D = ± 12.5 V, V+ = 13.5 V, V- = -13.5 V		Room	20	-	35	-	35	Ω
				Full	-	-	45	-	45	
Switch off leakage current	$I_{S(off)}$	V+ = 16.5, V- = -16.5 V, V_D = ± 15.5 V, V_S = ± 15.5 V		Room	-0.1	-0.25	0.25	-0.25	0.25	nA
				Full	-	-20	20	-5	5	
	$I_{D(off)}$		DG417 DG418	Room	-0.1	-0.25	0.25	-0.25	0.25	
				Full	-	-20	20	-5	5	
			DG419	Room	-0.1	-0.75	0.75	-0.75	0.75	
				Full	-	-60	60	-12	12	
Channel off leakage current	$I_{D(on)}$	V+ = 16.5 V, V- = -16.5 V, V_S = V_D = ± 15.5 V	DG417 DG418	Room	-0.4	-0.4	0.4	-0.4	0.4	
				Full	-	-40	40	-10	10	
			DG419	Room	-0.4	-0.75	0.75	-0.75	0.75	
				Full	-	-60	60	-12	12	
Digital Control										
Input current V_{IN} low	I_{IL}			Full	0.005	-0.5	0.5	-0.5	0.5	µA
Input current V_{IN} high	I_{IH}			Full	0.005	-0.5	0.5	-0.5	0.5	
Dynamic Characteristics										
Turn-on time	t_{on}	R_L = 300 Ω, C_L = 35 pF, V_S = ± 10 V, see Switching Time Test Circuit	DG417 DG418	Room	100	-	175	-	175	ns
				Full	-	-	250	-	250	
Turn-off time	t_{off}		DG417 DG418	Room	60	-	145	-	145	
				Full	-	-	210	-	210	
Transition time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF, V_{S1} = ± 10 V, V_{S2} = ± 10 V	DG419	Room	-	-	175	-	175	
				Full	-	-	250	-	250	
Break-before-make time delay (DG403)	t_D	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = ± 10 V	DG419	Room	13	5	-	5	-	
Charge injection	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω		Room	60	-	-	-	-	pC
Source off capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V		Room	8	-	-	-	-	pF
Drain off capacitance	$C_{D(off)}$		DG417 DG418	Full	8	-	-	-	-	
Channel on capacitance	$C_{D(on)}$	f = 1 MHz, V_S = 0 V	DG417 DG418	Room	30	-	-	-	-	
			DG419	Room	35	-	-	-	-	
Power Supplies										
Positive supply current	I+	V+ = 16.5 V, V- = -16.5 V, V_{IN} = 0 V or 5 V		Room	0.001	-	1	-	1	µA
				Full	-	-	5	-	5	
Negative supply current	I-			Room	-0.0001	-1	-	-1	-	
				Full	-	-5	-	-5	-	
Logic supply current	I_L			Room	0.001	-	1	-	1	
				Full	-	-	5	-	5	
Ground current	I_{GND}			Room	-0.0001	-1	-	-1	-	
				Full	-	-5	-	-5	-	

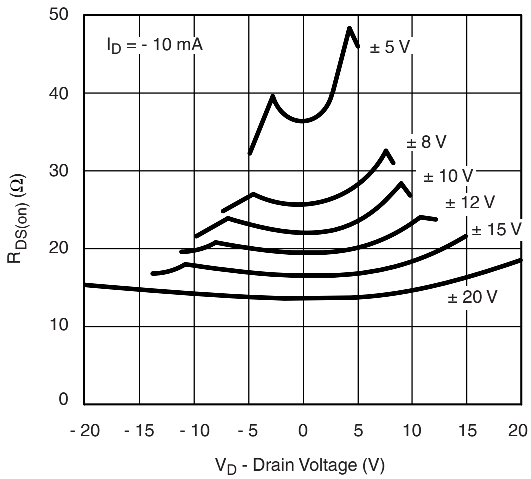
SPECIFICATIONS a (unipolar supplies)									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 12 V, V- = 0 V, V_L = 5 V, V_{IN} = 2.4 V, 0.8 V f	TEMP. b	TYP. c	A SUFFIX LIMITS -55 °C to +125 °C		D SUFFIX LIMITS -40 °C to +85 °C		UNIT
					MIN. d	MAX. d	MIN. d	MAX. d	
Analog Switch									
Analog signal range e	V_{ANALOG}		Full	-	0	12	0	12	V
Drain-source on-resistance	$R_{DS(on)}$	I_S = -10 mA, V_D = 3.8 V, V+ = 10.8 V	Room	40	-	-	-	-	Ω
Dynamic Characteristics									
Turn-on time	t_{on}	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V, see Switching Time Test Circuit	Room	110	-	-	-	-	ns
Turn-off time	t_{off}		Room	40	-	-	-	-	
Break-before-make time delay	t_D	DG419 only, R_L = 300 Ω, C_L = 35 pF	Room	60	-	-	-	-	
Charge injection	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room	5	-	-	-	-	pC
Power Supplies									
Positive supply current	I+	V+ = 13.2 V, V_L = 5.25 V, V_{IN} = 0 V or 5 V	Room	0.001	-	-	-	-	μA
Negative supply current	I-		Room	-0.001	-	-	-	-	
Logic supply current	IL		Room	0.001	-	-	-	-	
Ground current	I_{GND}		Room	-0.001	-	-	-	-	

Notes

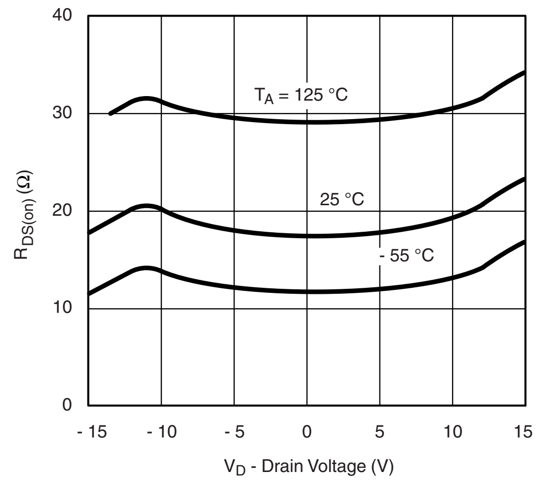
a. Refer to PROCESS OPTION FLOWCHART
b. Room = 25 °C, full = as determined by the operating temperature suffix
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
e. Guaranteed by design, not subject to production test
f. V_{IN} = input voltage to perform proper function

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

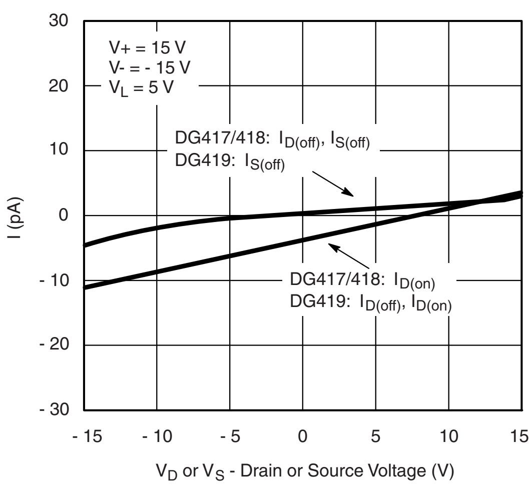
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



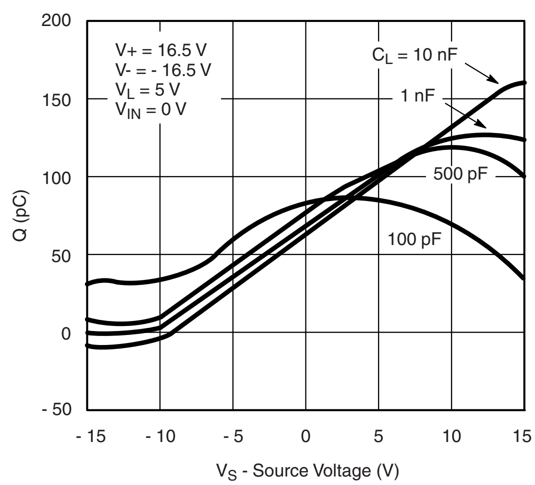
$R_{DS(on)}$ vs. V_D and Supply Voltage



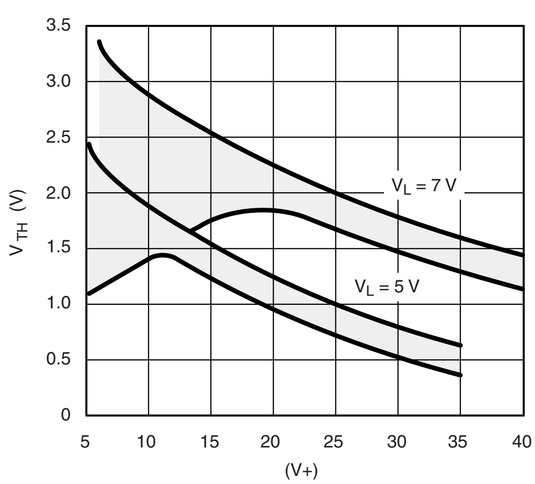
$R_{DS(on)}$ vs. Temperature



Leakage Currents vs. Analog Voltage

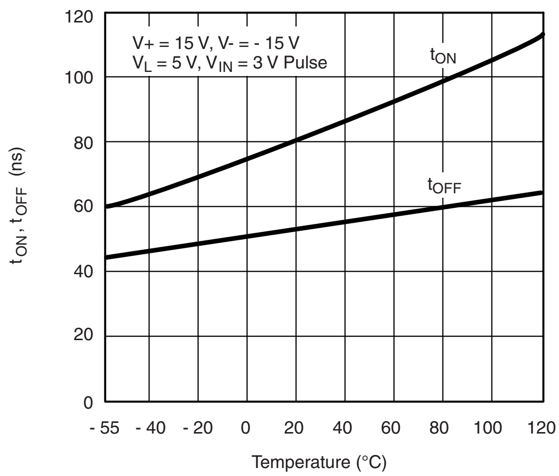


Drain Charge Injection

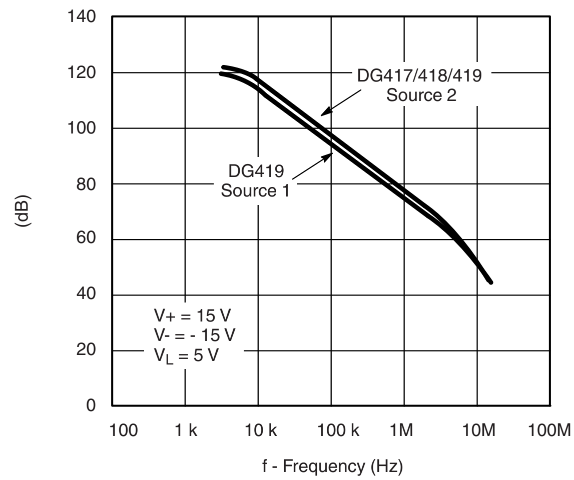


Input Switching Threshold vs. Supply Voltages

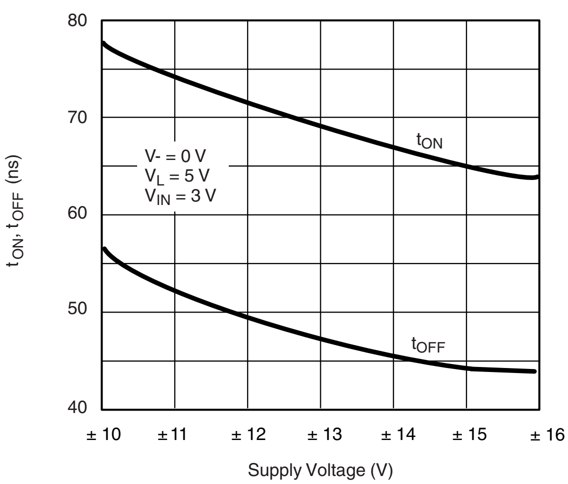
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



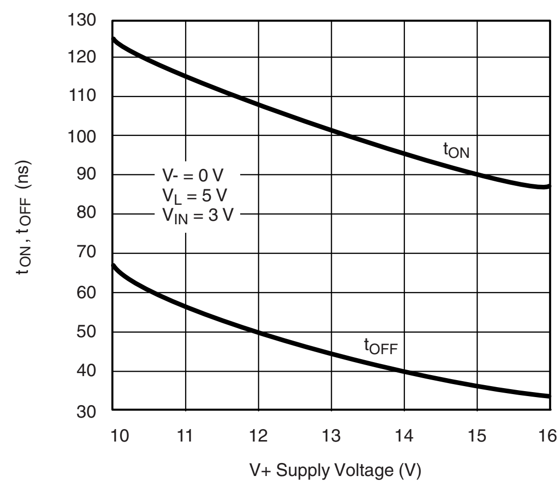
Switching Time vs. Temperature



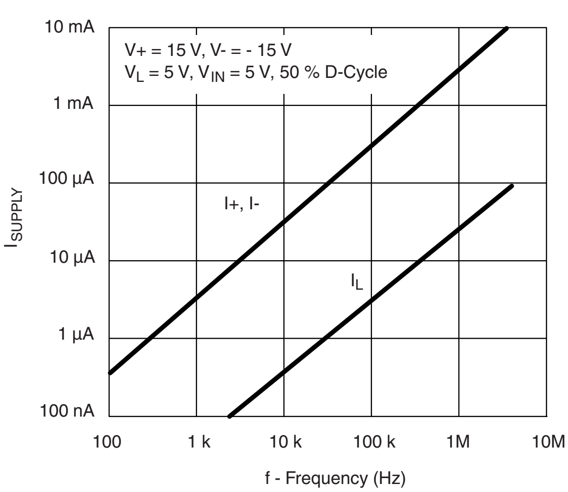
Crosstalk and Off Isolation vs. Frequency



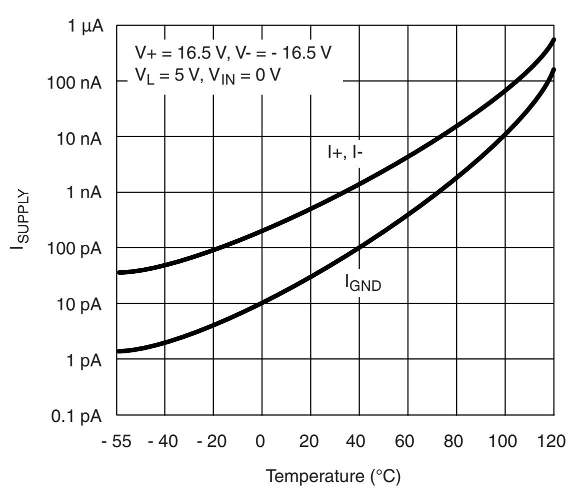
Switching Time vs. Supply Voltages



Switching Time vs. V+



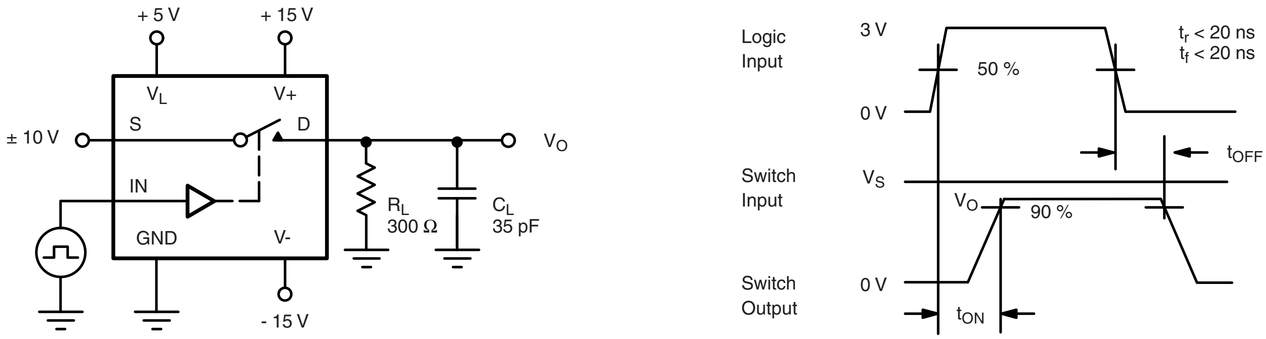
Power Supply Currents vs. Switching



Supply Current vs. Temperature

TEST CIRCUITS

V_O is the steady state output with the switch on.



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Note: Logic input waveform is inverted for switches that have the opposite logic sense.

Fig. 2 - Switching Time (DG417, DG418)

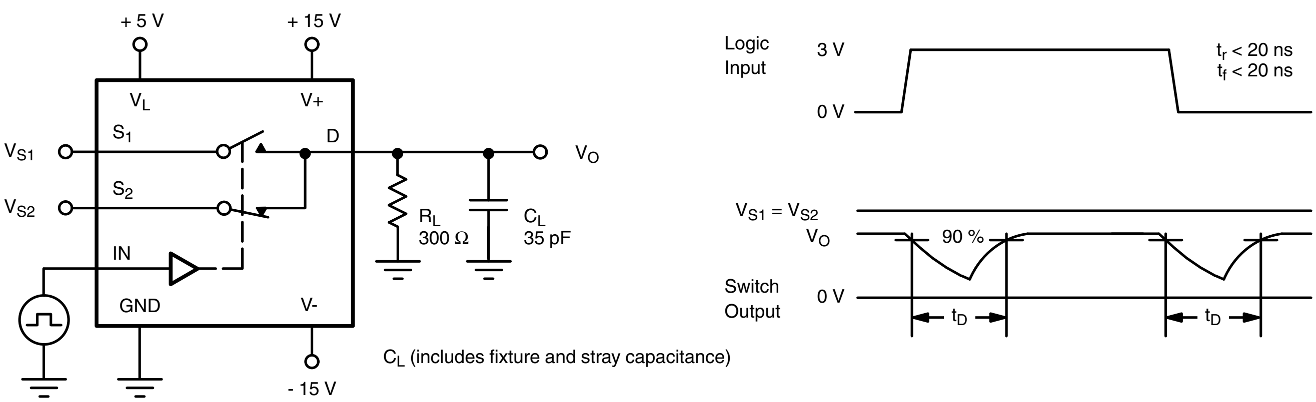
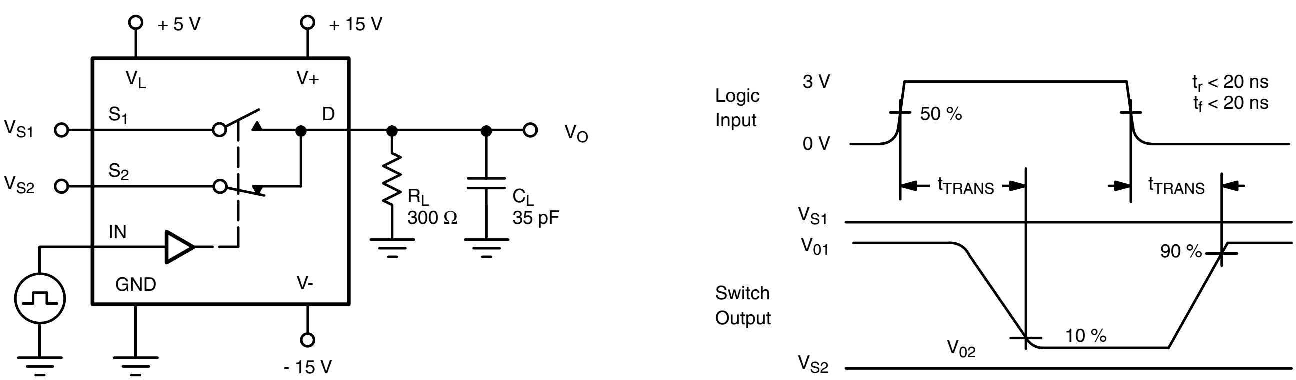


Fig. 3 - Break-Before-Make (DG419)



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Fig. 4 - Transition Time (DG419)

TEST CIRCUITS

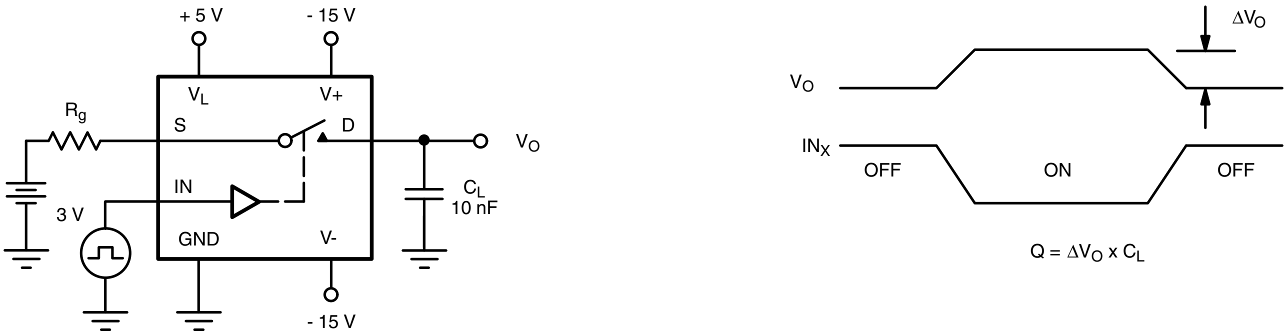
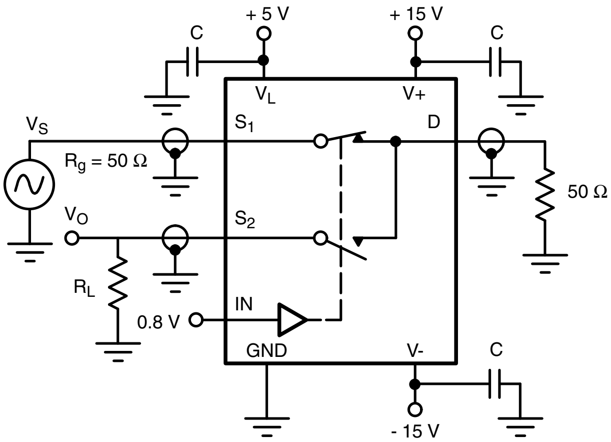


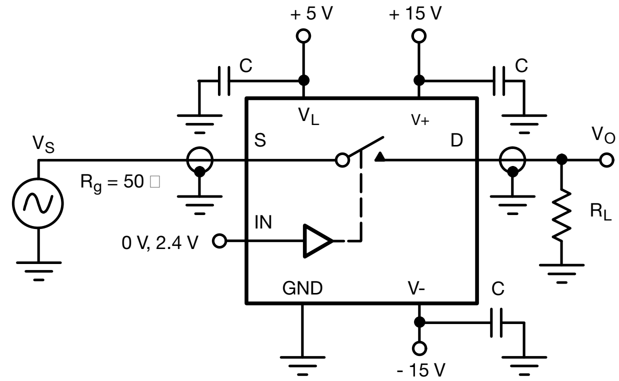
Fig. 5 - Charge Injection



X_{TALK} Isolation = 20 log $\left|\dfrac{V_S}{V_O}\right|$

C = RF bypass

Fig. 6 - Crosstalk (DG419)



Off isolation = 20 log $\left|\dfrac{V_S}{V_O}\right|$

Fig. 7 - Off Isolation

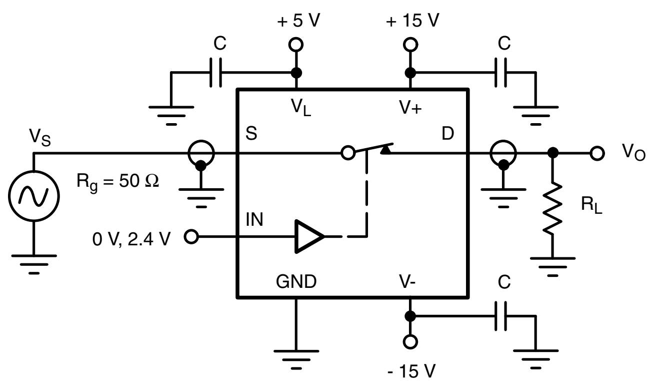


Fig. 8 - Insertion Loss

TEST CIRCUITS

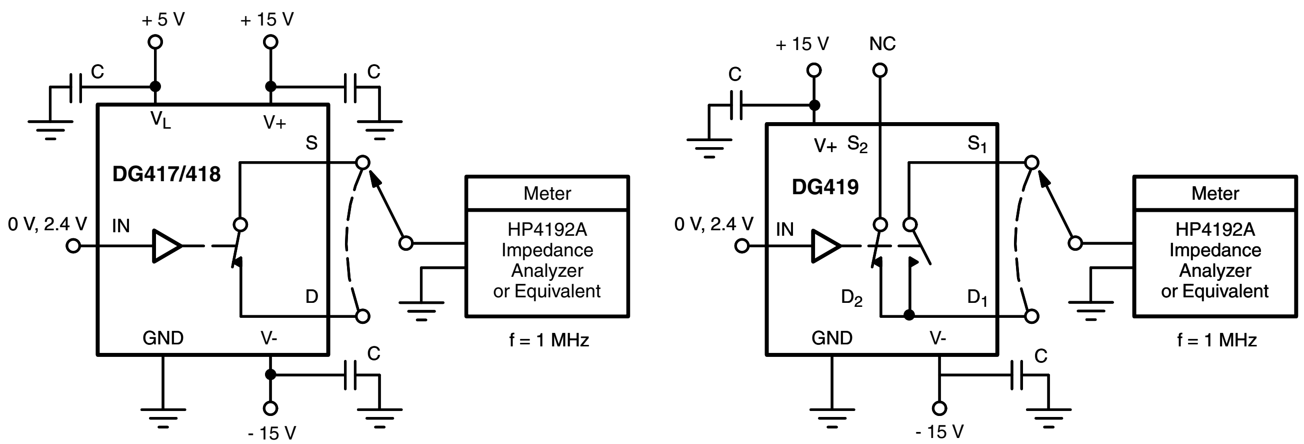


Fig. 9 - Source/Drain Capacitances

APPLICATIONS

Switched Signal Powers Analog Switch

The analog switch in Fig. 10 derives power from its input signal, provided the input signal amplitude exceeds 4 V and its frequency exceeds 1 kHz.

This circuit is useful when signals have to be routed to either of two remote loads. Only three conductors are required: one for the signal to be switched, one for the control signal and a common return.

A positive input pulse turns on the clamping diode D_1 and charges C_1. The charge stored on C_1 is used to power the chip; operation is satisfactory because the switch requires less than 1 µA of stand-by supply current. Loading of the signal source is imperceptible. The DG419's on-resistance is a low 100 Ω for a 5 V input signal.

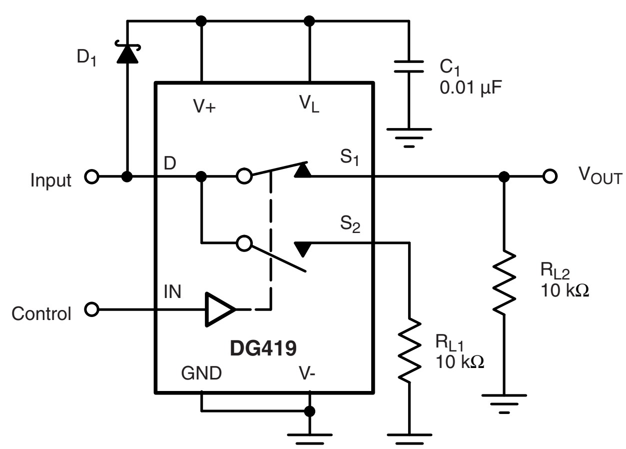


Fig. 10 - Switched Signal Powers Remote SPDT Analog Switch

APPLICATIONS

Micropower UPS Transfer Switch

When V_{CC} drops to 3.3 V, the DG417 changes states, closing S_{W1} and connecting the backup cell, as shown in Fig. 10. D_1 prevents current from leaking back towards the rest of the circuit. Current consumption by the CMOS analog switch is around 100 pA; this ensures that most of the power available is applied to the memory, where it is really needed. In the stand-by mode, hundreds of A are sufficient to retain memory data.

When the 5 V supply comes back up, the resistor divider senses the presence of at least 3.5 V, and causes a new change of state in the analog switch, restoring normal operation.

Programmable Gain Amplifier

The DG419, as shown in Fig. 11, allows accurate gain selection in a small package. Switching into virtual ground reduces distortion caused by $R_{DS(on)}$ variation as a function of analog signal amplitude.

GaAs FET Driver

The DG419, as shown in Fig.12 may be used as a GaAs FET driver. It translates a TTL control signal into -8 V, 0 V level outputs to drive the gate.

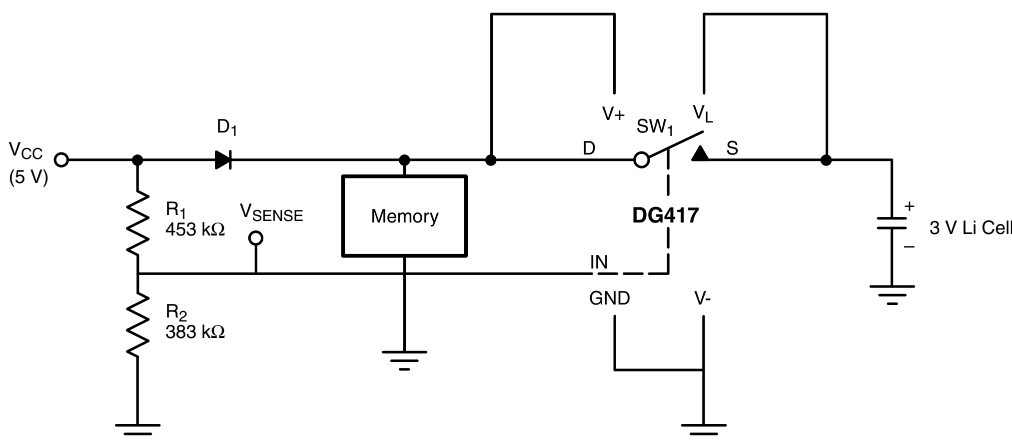


Fig. 11 - Micropower UPS Circuit

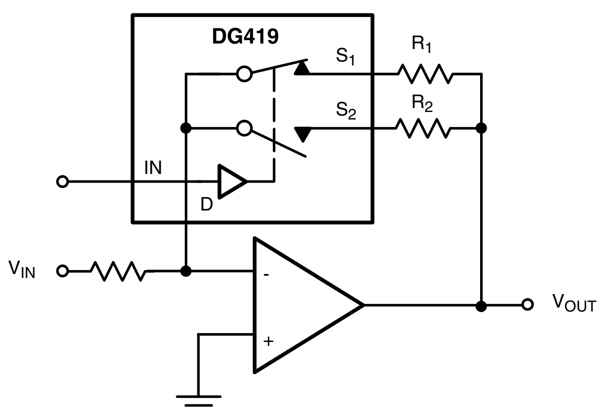


Fig. 12 - Programmable Gain Amplifier

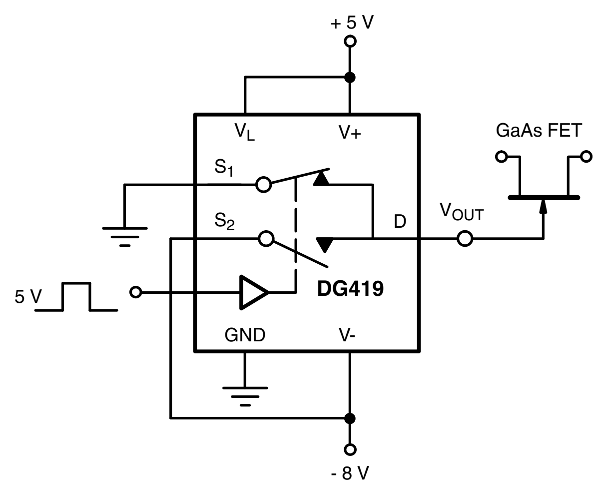


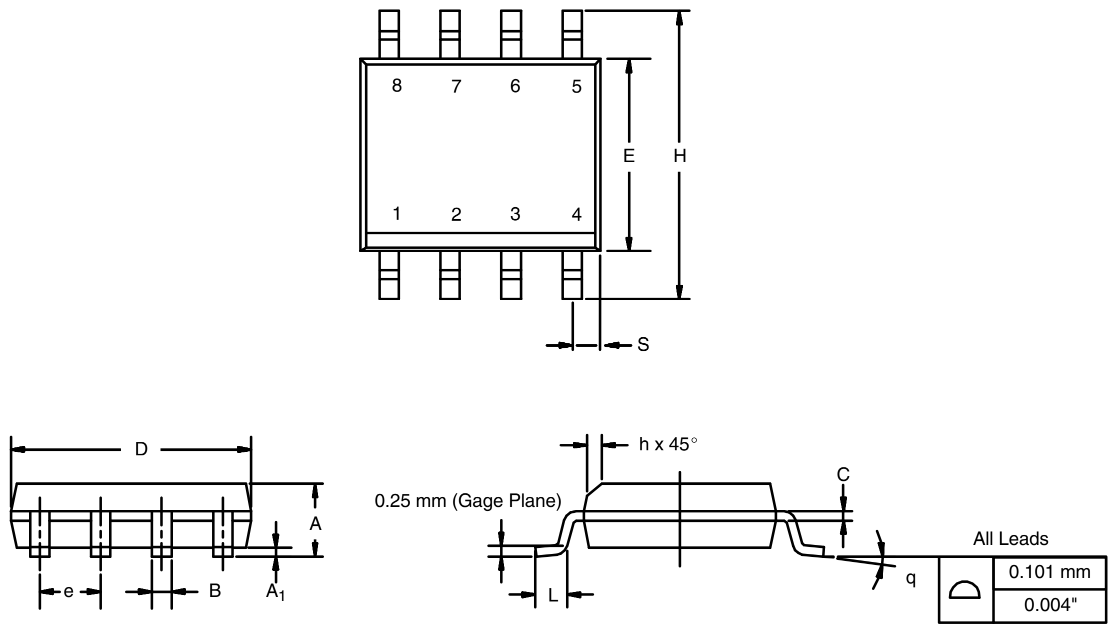
Fig. 13 - GaAs FET Driver

PRODUCT SUMMARY						
Part number	DG417	DG417	DG418	DG418	DG419	DG419
Status code	2	2	2	2	2	2
Configuration	SPST x 1, NC	SPST x 1, NC	SPST x 1, NO	SPST x 1, NO	SPDT x 1	SPDT x 1
Single supply min. (V)	5	5	5	5	5	5
Single supply max. (V)	40	40	40	40	40	40
Dual supply min. (V)	5	5	5	5	5	5
Dual supply max. (V)	20	20	20	20	20	20
On-resistance (Ω)	20	20	20	20	20	20
Charge injection (pC)	60	60	60	60	60	60
Source on capacitance (pF)	30	30	30	30	30	30
Source off capacitance (pF)	8	8	8	8	8	8
Leakage switch on typ. (nA)	0.4	0.4	0.4	0.4	0.4	0.4
Leakage switch off max. (nA)	0.25	0.25	0.25	0.25	0.25	0.25
-3 dB bandwidth (MHz)	-	-	-	-	-	-
Package	SO-8 (narrow) AS	Plastic DIP-8	SO-8 (narrow) AS	Plastic DIP-8	SO-8 (narrow) AS	Plastic DIP-8
Functional circuit / applications	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare
Interface	Parallel	Parallel	Parallel	Parallel	Parallel	Parallel
Single supply operation	Yes	Yes	Yes	Yes	Yes	Yes
Dual supply operation	Yes	Yes	Yes	Yes	Yes	Yes
Turn on time max. (ns)	175	175	175	175	175	175
Crosstalk and off isolation	-60	-60	-60	-60	-60	-60

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70051.

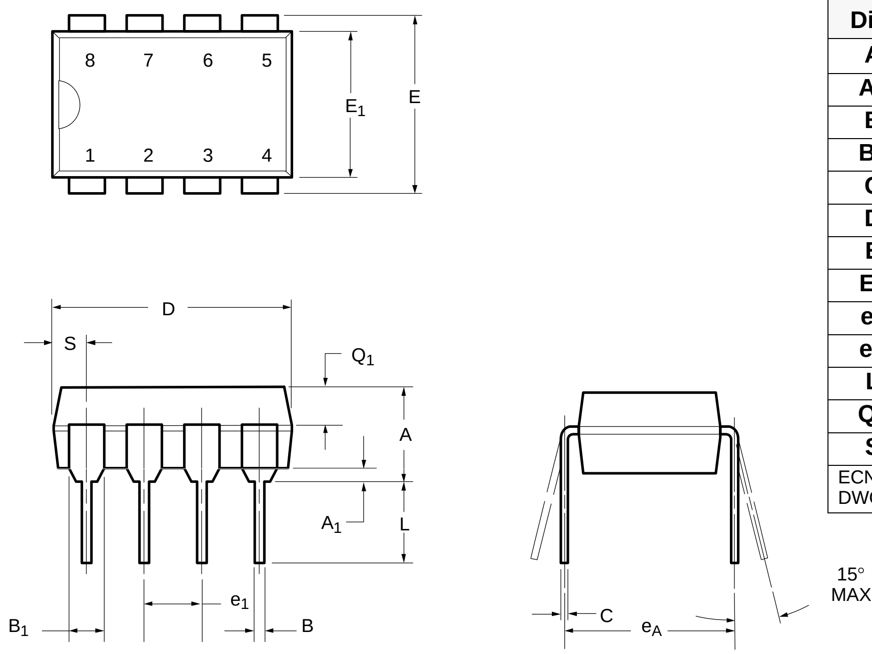
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

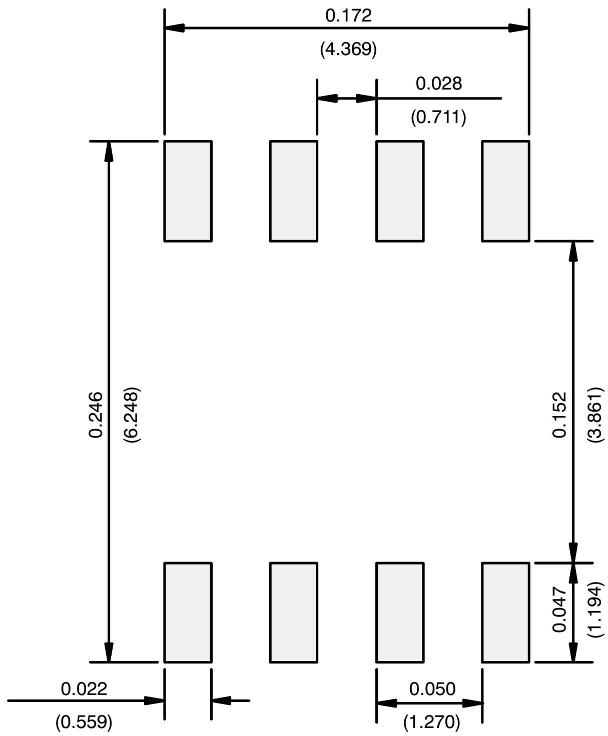
PDIP: 8-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	9.02	10.92	0.355	0.430
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.76	1.65	0.030	0.065
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5478				

NOTE: End leads may be half leads.

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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