

Monolithic General-Purpose CMOS Analog Switch

FEATURES

- ±15-V Input Range
- On-Resistance: <50 Ω
- Break-Before-Make Switching
- TTL and CMOS Compatible

BENEFITS

- Improved Signal Headroom
- Reduced Switching Errors
- No Shorting of Inputs
- Simple Interfacing

APPLICATIONS

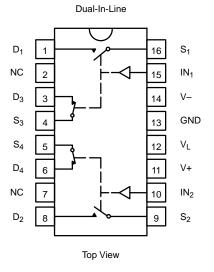
- Audio Switching
- Instrumentation
- Battery Powered Systems

DESCRIPTION

The DG5043 solid state analog switch is recommended for general purpose applications in instrumentation, and process control. Built on the Vishay Siliconix PLUS-40 high voltage CMOS process, this device provides ease-of-use and performance advantages to the system designer. Key performance features of the DG5043 are 1- μ s switching, low

power supply requirements, and break-before-make switching. Each switch conducts equally well in either direction, when on, and blocks up to 30 V peak-to-peak when off. Off leakage current is 1-nA maximum. An epitaxial layer prevents latch up. For new designs, DG403 is recommended.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE					
Logic	SW_1, SW_2	SW ₃ , SW ₄			
0	OFF	ON			
1	ON	OFF			

ORDERING INFORMATION					
Temp Range	Package	Part Number			
0 to 70°C	16-Pin Plastic DIP	DG5043CJ			

ABSOLUTE MAXIMUM RATINGS

V+ to V	44 V
GND to V-	25 V
V _L (GND – 0.3 \	/) to 44 V
Digital Inputs ^a V _S , V _D (V–) –2 V to (V+	plus 2 V)
or 30 mA, whichever or	ccurs first
Current (Any Terminal) Continuous	. 30 mA
Current, S or D (Pulsed 1 ms 10% duty)	100 mA
Storage Temperature	to 125°C

Power Dissipation (Package)b

16-Pin Plastic DIP^c 470 mW

Notes:

- a. Signals on S_X , D_X , or IN_X exceeding V+ or V- will be clamped by internal diada. Unit for word diada
- diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C

Vishay Siliconix



SPECIFICATIONS								
Parameter		Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V $V_L = 5 V, V_{IN} = 2 V, 0.8 V^e$		C Suffix 0 to 70°C				
	Symbol		Temp ^a	Min ^c	Тур ^ь	Max ^c	Unit	
Analog Switch			•					
Analog Signal Range ^d	VANALOG		Full	-15		15	V	
Drain-Source On-Resistance	r _{DS(on)}	$I_{S} = -10 \text{ mA}, V_{D} = \pm 10 \text{ V}$	Room Full			50 75	Ω	
Switch Off Leakage Current	I _{S(off)}	V _S = V _D = 14 V	Room Full	-1 -100		1 100	nA	
	'S(off)	$V_{S} = V_{D} = -14 V$	Room Full	-1 -100		1 100		
Channel On Leakage Current		$V_{S} = V_{D} = 14 V$	Room Full			2 200		
	D(on)	$V_{S} = V_{D} = -14 V$	Room Full	-2 -200				
Digital Control								
Input Current with VIN Low	Ι _{ΙL}	V _{IN} Under Test = 0.8 V	Full	-1		1		
Input Current with VIN High	lін	V _{IN} Under Test = 2 V	Full	-1		1	μA	
Dynamic Characteristics			-	-	-	-	-	
Turn-On Time	t _{ON}	Vo = +10 V R = 1 kQ C = 35 pE	Room			1200	ns	
Turn-Off Time	t _{OFF}	V_{S} = \pm 10 V, R_{L} = 1 k Ω,C_{L} = 35 pF See Figure 1	Room			700		
Charge Injection ^d	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		30		рС	
Off Isolation ^d	OIRR	$R_L = 75 \Omega$, $C_L = 5 pF$, f = 1 MHz	Room		75		dB	
Crosstalk (Channel-to-Channel) ^d	X _{TALK}	R_L = 75 Ω , V_S = 2 V_{P-P} , f = 1 MHz	Room		89			
Source Off Capacitance	C _{S(off)}		Room		15		pF	
Drain Off Capacitanced	C _{D(off)}	$V_D = V_S = 0 V$, f = 1 MHz	Room		17			
Channel On Capacitanced	C _{D(on)}	1	Room		45			
Power Supplies	-			-	-	-	-	
Positive Supply Current	l+	V _{IN} = 0 or 2.4 V	Full			300		
Negative Supply Current	I–		Full	-300			1.	
Logic Supply Current	١L	V _{IN} = 0 or 2.4 V	Full		<u> </u>	300	μA	
Ground Current	I _{GND}		Full	-300			1	

Notes:

a.

b.

Room = 25°C, Full = as determined by the operating temperature suffix. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

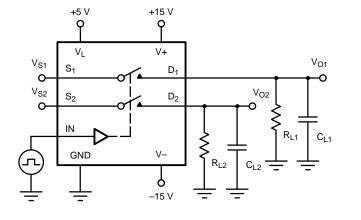
c. d. Guaranteed by design, not subject to production test. V_{IN} = input voltage to perform proper function.

e.

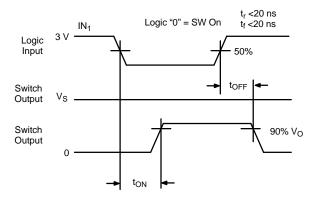


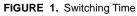
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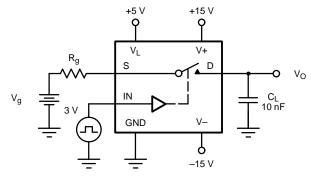
TEST CIRCUITS



CL (includes fixture and stray capacitance)







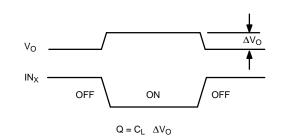


FIGURE 2. Charge Injection



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