Single 8-Ch/Differential 4-Ch Latchable Analog Multiplexers

DESCRIPTION

The DG428, DG429 analog multiplexers have on-chip address and control latches to simplify design in microprocessor based applications. Break-before-make switching action protects against momentary crosstalk of adjacent input signals.

The DG428 selects one of eight single-ended inputs to a common output, while the DG429 selects one of four differential inputs to a common differential output.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

The silicon-gate CMOS process enables operation over a wide range of supply voltages. The absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed and an epitaxial layer prevents latchup.

On-board TTL-compatible address latches simplify the digital interface design and reduce board space in bus-controlled systems such as data acquisition systems, process controls, avionics, and ATE.

FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- Low $R_{DS(on)}$: 55 Ω
- Low Charge Injection: 1 pC
- On-Board TTL Compatible Address Latches
- High Speed - t_{TRANS}: 160 ns
- Break-Before-Make
- Low Power Consumption: 0.3 mW
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE

BENEFITS

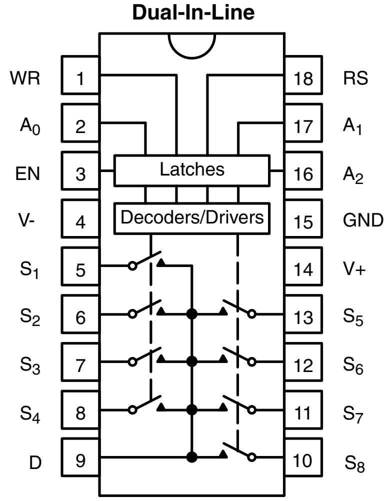
- Improved System Accuracy
- Microprocessor Bus Compatible
- Easily Interfaced
- Reduced Crosstalk
- High Throughput
- Improved Reliability

APPLICATIONS

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics and Military Systems
- Communication Systems
- Microprocessor-Controlled Analog Systems
- Medical Instrumentation

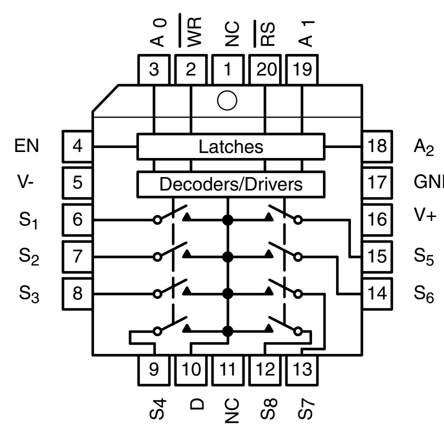
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG428
Dual-In-Line



Top View

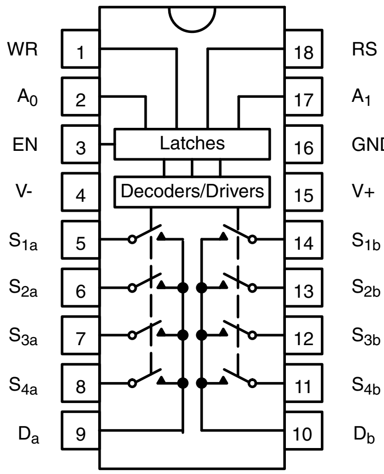
DG428
PLCC



Top View

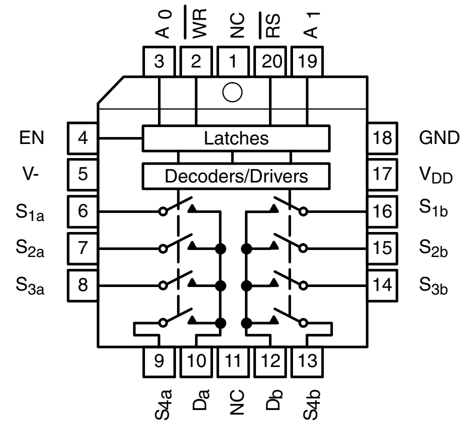
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG429
Dual-In-Line and SOIC



Top View

DG429
PLCC



Top View

TRUTH TABLE - DG428

8-Channel Single-Ended Multiplexer						
A_2	A_1	A_0	EN	WR	RS	On Switch
Latching						
X	X	X	X	↑	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	None (latches cleared)
Transparent Operation						
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

TRUTH TABLE - DG429

Differential 4-Channel Multiplexer					
A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching					
X	X	X	↑	1	Maintains previous switch condition
Reset					
X	X	X	X	0	None (latches cleared)
Transparent Operation					
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

ORDERING INFORMATION - DG428

Temp Range	Package	Part Number
- 40 °C to 85 °C	18-pin Plastic DIP	DG428DJ
		DG428DJ-E3
	20-pin PLCC	DG428DN
		DG428DN-E3

ORDERING INFORMATION - DG429

Temp Range	Package	Part Number
- 40 °C to 85 °C	18-pin Plastic DIP	DG429DJ
		DG429DJ-E3
	20-pin PLCC	DG429DN
		DG429DN-E3
	18-pin Widebody SOIC	DG429DW
		DG429DW-E3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Voltages Referenced to V-	V+		44	V
	GND		25	
Digital Inputs[a], V_S, V_D			(V-) - 2 V to (V+) + 2 V or 30 mA, whichever occurs first	
Current (Any Terminal)			30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % Duty Cycle Max)			100	
Storage Temperature	(AK Suffix)		- 65 to 150	°C
	(DJ, DN Suffix)		- 65 to 125	
Power Dissipation (Package)[b]	18-pin Plastic DIP[c]		470	mW
	18-pin CerDIP[d]		900	
	20-pin PLCC[f]		800	
	28-Pin Widebody SOIC[f]		450	

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6.3 mW/°C above 75 °C.
d. Derate 12 mW/°C above 75 °C.
e. Derate 10 mW/°C above 75 °C.
f. Derate 6 mW/°C above 75 °C.

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V, $\overline{WR}$ = 0, $\overline{RS}$ = 2.4 V, V_{IN} = 2.4 V, 0.8 V[f]		Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C Min.[d]	A Suffix Max.[d]	D Suffix - 40 °C to 85 °C Min.[d]	D Suffix Max.[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_D = ± 10 V, V_{AL} = 0.8 V I_S = - 1 mA, V_{AH} = 2.4 V		Room Full	55		100 125		100 125	Ω
Greatest Change in $R_{DS(on)}$ Between Channels[g]	$\Delta R_{DS(on)}$	- 10 V < V_S < 10 V I_S = - 1 mA		Room	5					%
Source Off Leakage Current	$I_{S(off)}$	V_S = ± 10 V, V_{EN} = 0 V, V_D = ± 10 V		Room Full	± 0.03	- 0.5 - 50	0.5 50	- 0.5 - 50	0.5 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_{EN} = 0 V V_D = ± 10 V V_S = ± 10 V	DG428	Room Full	± 0.07	- 1 - 100	1 100	- 1 - 100	1 100	nA
			DG429	Room Full	± 0.05	- 1 - 50	1 50	- 1 - 50	1 50	nA
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ± 10 V V_{EN} = 2.4 V V_{AL}= 0.8 V V_{AH} = 2.4 V	DG428	Room Full	± 0.07	- 1 - 100	1 100	- 1 - 100	1 100	nA
			DG429	Room Full	± 0.05	- 1 - 50	1 50	- 1 - 50	1 50	nA
Digital Control										
Logic Input Current Input Voltage High	I_{AH}	V_A = 2.4 V		Full	0.01		1		1	µA
		V_A = 15 V		Full	0.01		1		1	µA
Logic Input Current Input Voltage Low	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V $\overline{RS}$ = 0 V, $\overline{WR}$ = 0 V		Full	- 0.01	- 1		- 1		µA
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	8					pF
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 5		Room Full	150		250 300		250 300	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 4		Full	30	10		10		ns
Enable and Write Turn-On Time	$t_{ON(EN,WR)}$	See Figure 6 and 7		Room Full	90		150 225		150 225	ns
Enable and Reset Turn-Off Time	$t_{OFF(EN,RS)}$	See Figure 6 and 8		Room Full	55		150 300		150 300	ns
Charge Injection	Q	V_{GEN} = 0 V, R_{GEN} = 0 Ω C_L = 1 nF, See Figure 9		Room	1					pC
Off Isolation	OIRR	V_{EN} = 0 V, R_L = 300 Ω C_L = 15 pF, V_S = 7 V_{RMS} f = 100 kHz		Room	- 75					dB
Source Off Capacitance	$C_{S(off)}$	V_S = 0 V, V_{EN} = 0 V, f = 1 MHz		Room	11					pF
Drain Off Capacitance	$C_{D(off)}$	V_D = 0 V V_{EN} = 0 V f = 1 MHz	DG428	Room	40					pF
			DG429	Room	20					pF
Drain On Capacitance	$C_{D(on)}$		DG428	Room	54					pF
			DG429	Room	34					pF
Minimum Input Timing Requirements										
Write Pulse Width	t_W	See Figure 2		Full		100		100		ns
A_X, EN Data Set Up time	t_S			Full		100		100		ns
A_X, EN Data Hold Time	t_H			Full		10		10		ns
Reset Pulse Width	t_{RS}	V_S = 5 V, See Figure 3		Full		100		100		ns
Power Supplies										
Positive Supply Current	I+	V_{EN} = V_A = 0, $\overline{RS}$ = 5 V		Room	20		100		100	µA
Negative Supply Current	I-			Room	- 0.001	- 5		- 5		µA

SPECIFICATIONS[a] (for single supply)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V- = 0 V, $\overline{WR}$ = 0, $\overline{RS}$ = 2.4 V, V_{IN} = 2.4 V, 0.8 V[f]		Temp.[b]	Typ.[c]	A Suffix - 55°C to 125 °C Min.[d]	A Suffix - 55°C to 125 °C Max.[d]	D Suffix - 40 °C to 85 °C Min.[d]	D Suffix - 40 °C to 85 °C Max.[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		0	12	0	12	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_D = ± 10 V, V_{AL} = 0.8 V I_S = - 500 µA, V_{AH} = 2.4 V		Room	80		150		150	Ω
$R_{DS(on)}$ Match[g]	$\Delta R_{DS(on)}$	0 V < V_S < 10 V I_S = - 1 mA		Room	5					%
Source Off Leakage Current	$I_{S(off)}$	V_S = 0 V, 10 V, V_{EN} = 0 V, V_D = 10 V, 0 V		Room Full	± 0.03	- 0.5 - 50	0.5 50	- 0.5 - 50	0.5 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = 0 V, 10 V V_S = 10 V, 0 V V_{EN} = 0 V	DG428	Room Full	± 0.07	- 1 - 100	1 100	- 1 - 100	1 100	nA
			DG429	Room Full	± 0.05	- 1 - 50	1 50	- 1 - 50	1 50	nA
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V, 10 V V_{EN} = 2.4 V V_{AL}= 0.8 V V_{AH} = 2.4 V	DG428	Room Full	± 0.07	- 1 - 100	1 100	- 1 - 100	1 100	nA
			DG429	Room Full	± 0.05	- 1 - 50	1 50	- 1 - 50	1 50	nA
Digital Control										
Logic Input Current Input Voltage High	I_{AH}	V_A = 2.4 V		Full			1		1	µA
		V_A = 12 V		Full			1		1	µA
Logic Input Current Input Voltage Low	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V $\overline{RS}$ = 0 V, $\overline{WR}$ = 0 V		Full		- 1		- 1		µA
Dynamic Characteristics										
Transition Time	t_{TRANS}	S_1 = 10 V/ 2 V, S_8 = 2 V/ 10 V See Figure 5		Room Full	160		280 350		280 350	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 4		Room Full	40	25 10		25 10		ns
Enable and WriteTurn-On Time	$t_{ON(EN,WR)}$	S_1 = 5 V See Figure 6 and 7		Room Full	110		300 400		300 400	ns
Enable and Reset Turn-Off Time	$t_{OFF(EN,RS)}$	S_1 = 5 V See Figure 6 and 8		Room Full	70		300 400		300 400	ns
Charge Injection	Q	V_{GEN} = 6 V, R_{GEN} = 0 Ω C_L = 1 nF, See Figure 9		Room	4					pC
Off Isolation	OIRR	V_{EN} = 0 V, R_L = 300 Ω C_L = 15 pF, V_S = 7 V_{RMS} f = 100 kHz		Room	- 75					dB
Minimum Input Timing Requirements										
Write Pulse Width	t_W	See Figure 2		Full		100		100		ns
A_X, EN Data Set Up time	t_S	See Figure 2		Full		100		100		ns
A_X, EN Data Hold Time	t_H	See Figure 2		Full		10		10		ns
Reset Pulse Width	t_{RS}	V_S = 5 V, See Figure 3		Full		100		100		ns
Power Supplies										
Positive Supply Current	I+	V_{EN} = 0 V, V_A = 0, $\overline{RS}$ = 5 V		Room	20		100		100	µA

Notes:

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 °C, full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

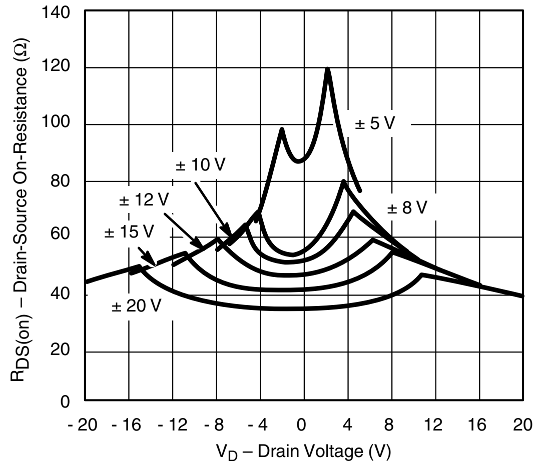
e. Guaranteed by design, not subject to production test.

f. V_{IN} = input voltage to perform proper function.

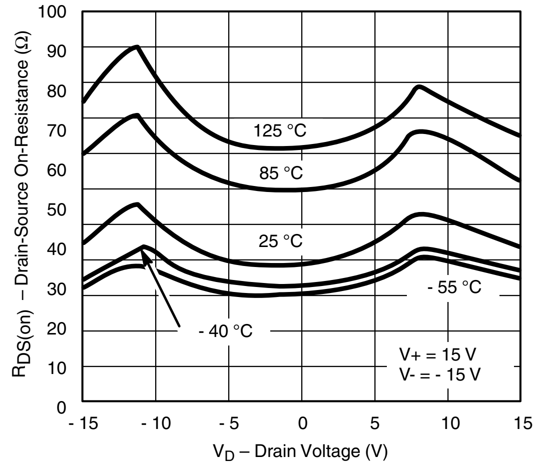
g. $$\Delta R_{DS(on)} = \left(\frac{R_{DS(on)}\ MAX - R_{DS(on)}\ MIN}{R_{DS(on)}\ AVE}\right) \times 100\ \%$$

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

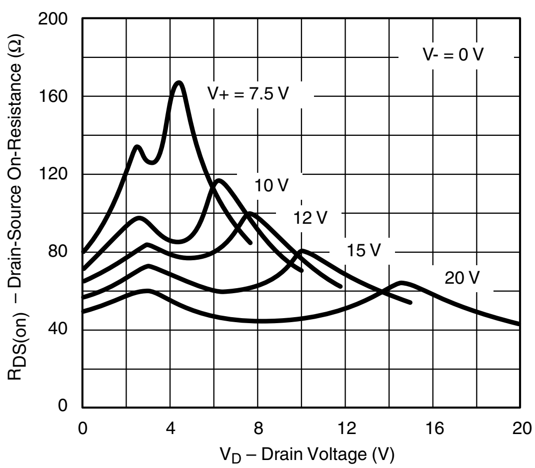
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



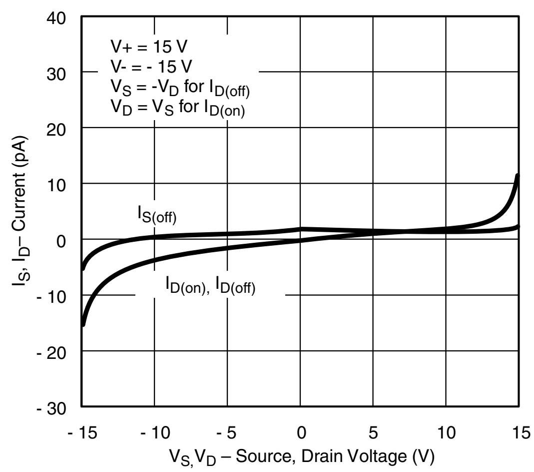
$R_{DS(on)}$ vs. V_D and Supply Voltage



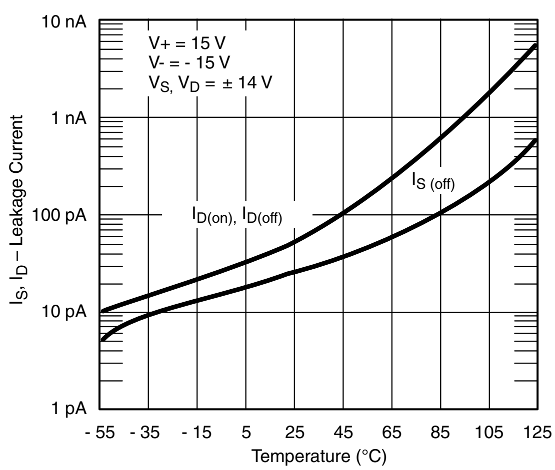
$R_{DS(on)}$ vs. V_D and Temperature



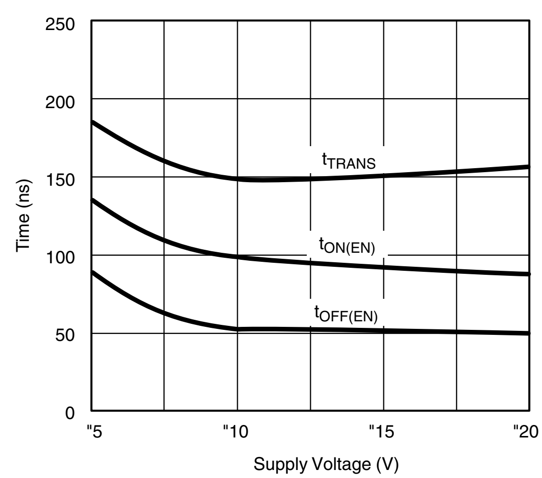
Single Supply $R_{DS(on)}$ vs. V_D and Supply



I_D , I_S Leakage Currents vs. Analog Voltage

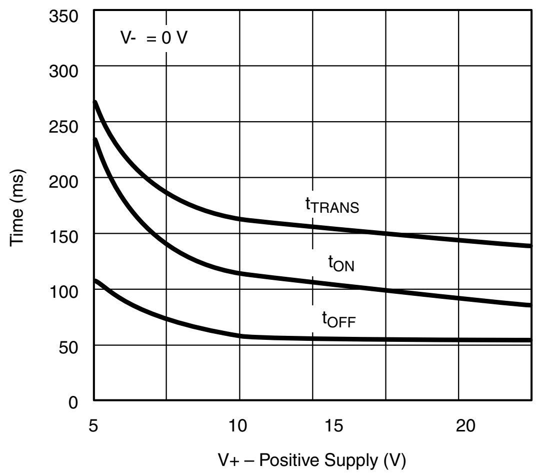


I_D , I_S Leakages vs. Temperature

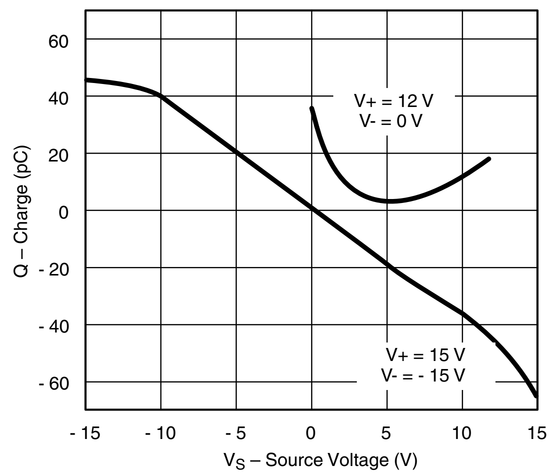


Switching Times vs. Power Supply Voltage

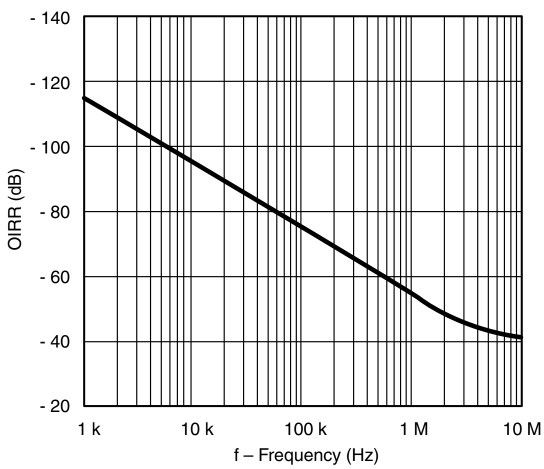
TYPICAL CHARACTERISTICS (T$_A$ = 25 °C, unless otherwise noted)



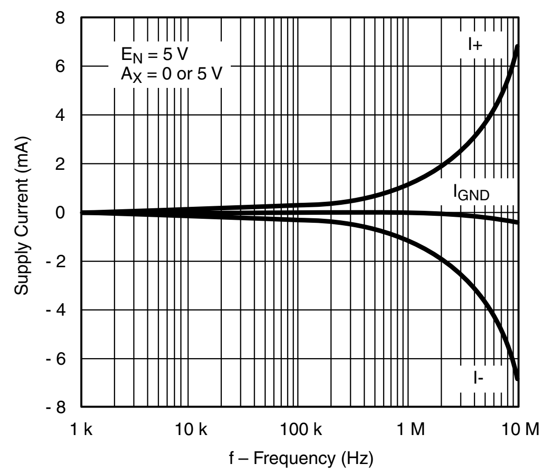
Switching Times vs. Single Supply



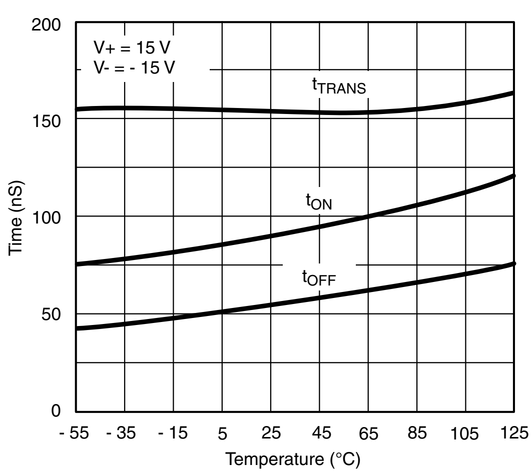
Charge Injection vs. Analog Voltage



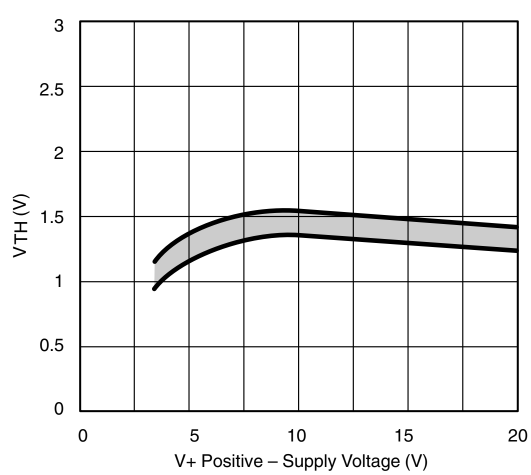
Off-Isolation vs. Frequency



Supply Currents vs. Switching Frequency



Switching Times vs. Temperature



Input Switching Threshold vs. Positive Supply Voltage

SCHEMATIC DIAGRAM (Typical Channel)

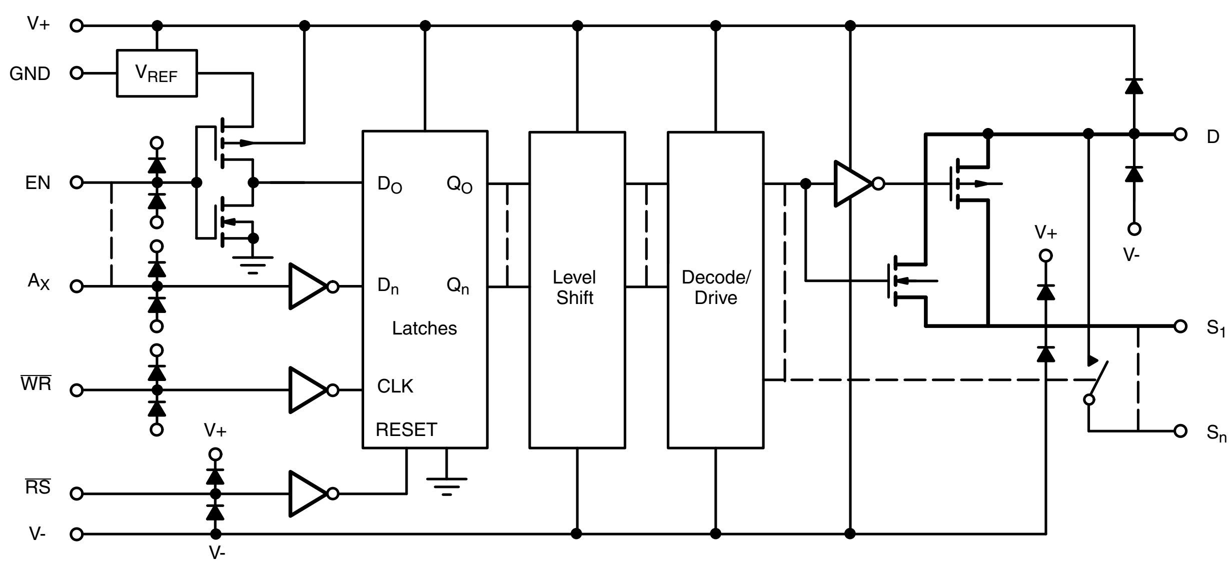


Figure 1.

TIMING DIAGRAMS

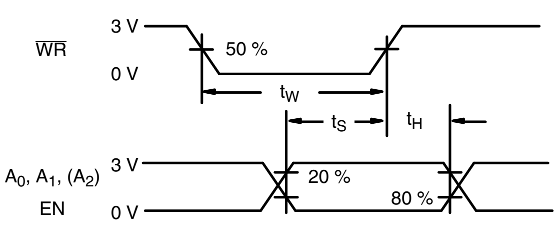


Figure 2.

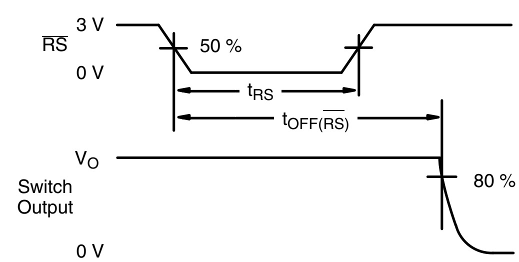


Figure 3.

TEST CIRCUITS

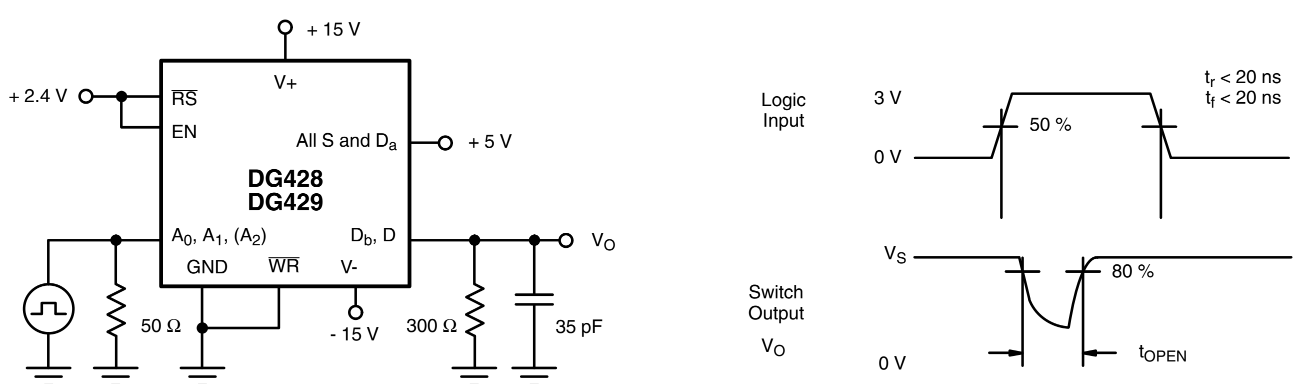


Figure 4. Break-Before-Make

TEST CIRCUITS

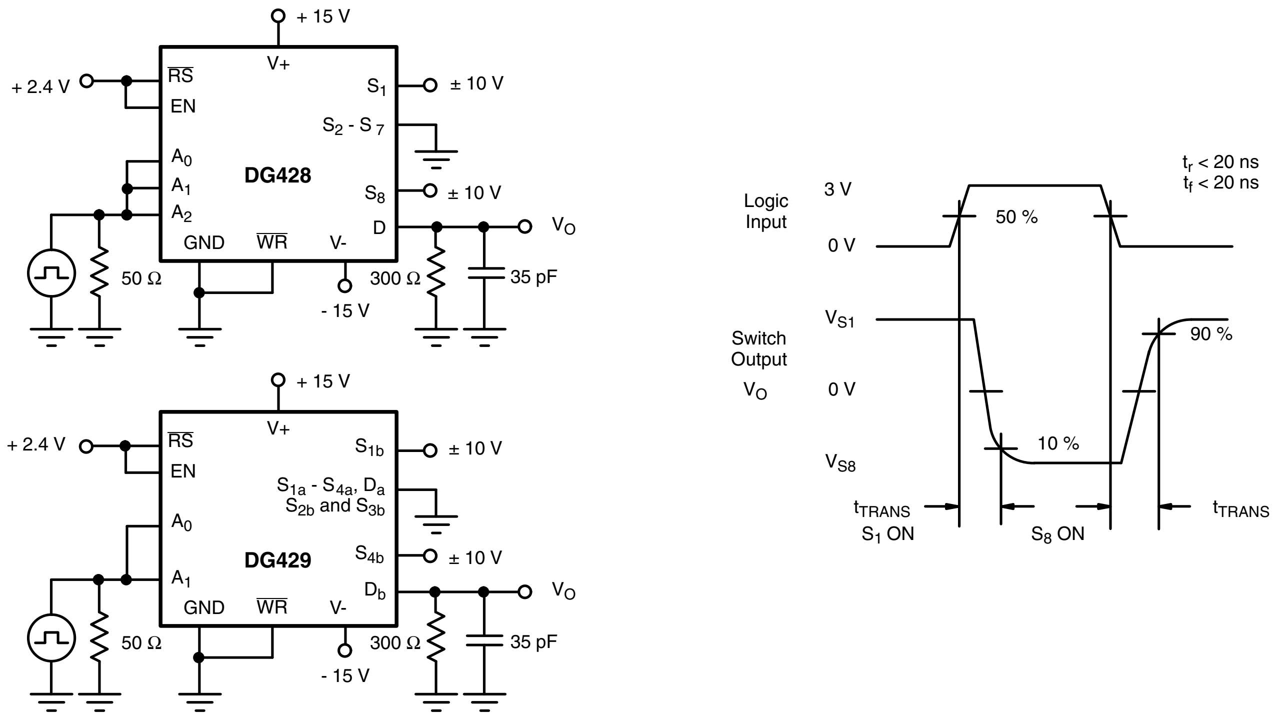


Figure 5. Transition Time

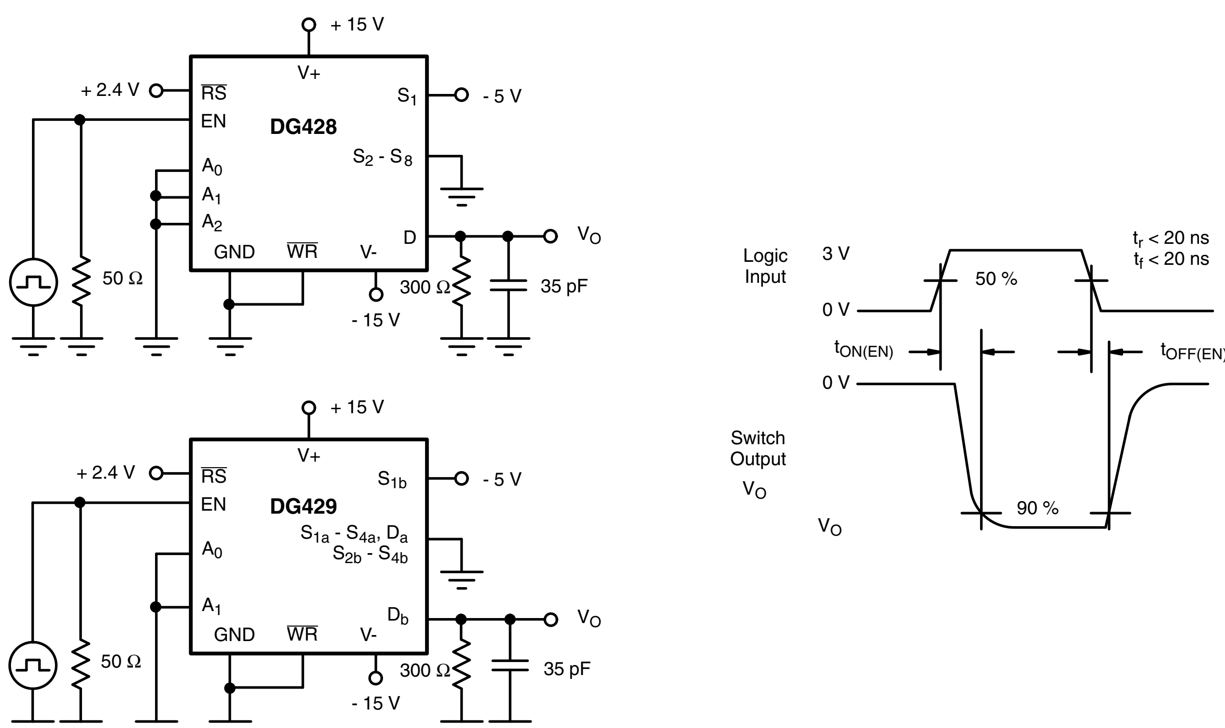


Figure 6. Enable t_{ON}/t_{OFF} Time

TEST CIRCUITS

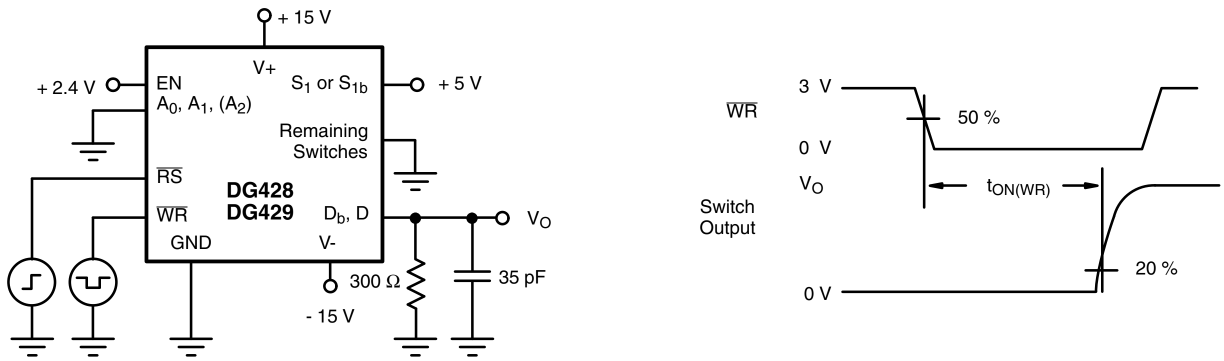


Figure 7. Write Turn-On Time $t_{ON(WR)}$

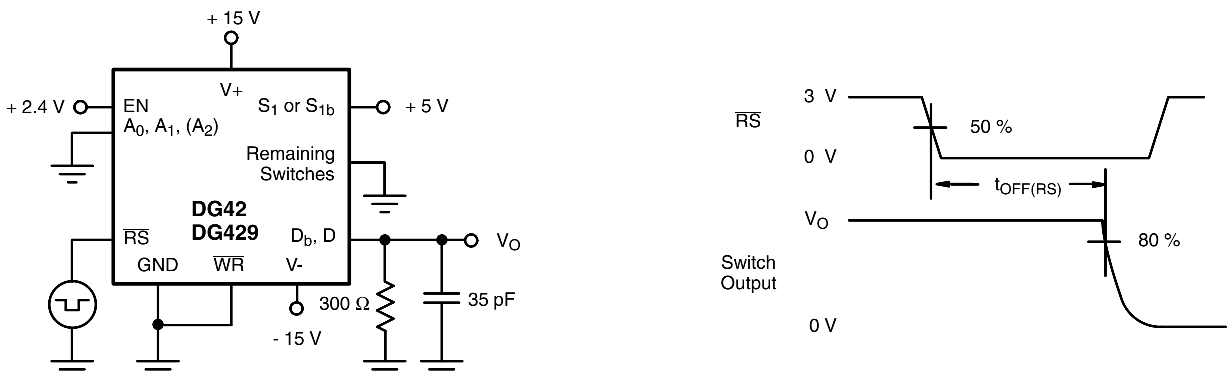
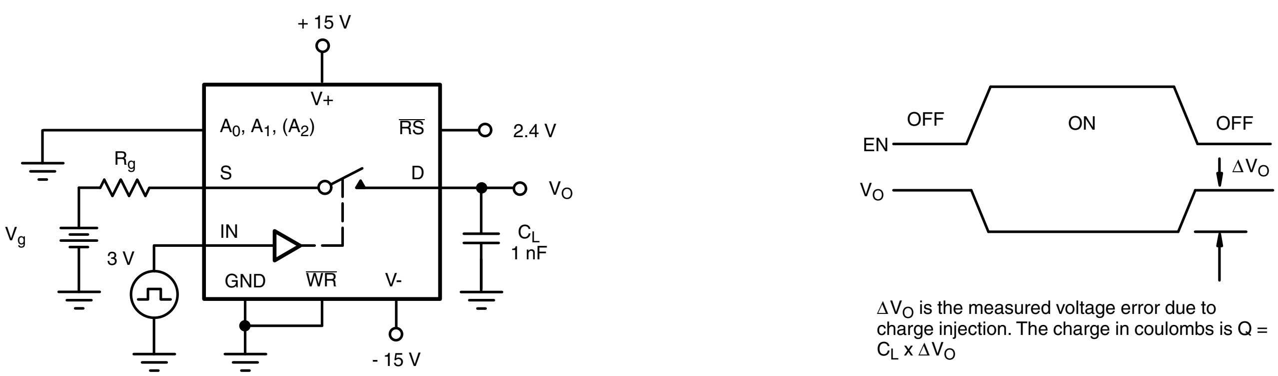


Figure 8. Reset Turn-Off Time $t_{OFF(RS)}$



ΔV_O is the measured voltage error due to charge injection. The charge in coulombs is Q = C_L x ΔV_O

Figure 9. Charge Injection

DETAILED DESCRIPTION

The internal structure of the DG428, DG429 includes a 5 V logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel n- and p-channel MOSFETs (see Figure 1).

The input protection on the logic lines A_0, A_1, A_2, EN and control lines $\overline{WR}$, $\overline{RS}$ shown in Figure 1 minimizes susceptibility to ESD that may be encountered during handling and operational transients.

The logic interface is a CMOS logic input with its supply voltage from an internal + 5 V reference voltage. The output of the input inverter feeds the data input of a D type latch. The level sensitive D latch continuously places the D_X input signal on the Q_X output when the $\overline{WR}$ input is low, resulting in transparent latch operation. As soon as $\overline{WR}$ returns high the latch holds the data last present on the D_n input, subject to the "Minimum Input Timing Requirements" table.

Following the latches the Q_n signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting ensures full on/off switch operation for any analog signal level between the V+ and V- supply rails.

The EN pin is used to enable the address latches during the $\overline{WR}$ pulse. It can be hard wired to the logic supply or to V+ if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The $\overline{RS}$ pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The $\overline{WR}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Truth Tables).

APPLICATIONS HINTS

Bus Interfacing

The DG428, DG429 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers write-only memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 on) until the microprocessor determines it is necessary to turn different switches on or turn all switches off (see Figure 10).

The input latches become transparent when $\overline{WR}$ is held low; therefore, these multiplexers operate by direct command of the coded switch state on A_2, A_1, A_0. In this mode the DG428 is identical to the popular DG408. The same is true of the DG429 versus the popular DG409.

During system power-up, $\overline{RS}$ would be low, maintaining all eight switches in the off state. After $\overline{RS}$ returned high the DG428 maintains all switches in the off state.

When the system program performs a write operation to the address assigned to the DG428, the address decoder provides a $\overline{CS}$ active low signal which is gated with the WRITE ($\overline{WR}$) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the $\overline{WR}$ signal returns to the high state, (positive edge) the input latches of the DG428 save the data from the DATA BUS. The coded information in the A_0, A_1, A_2 and EN latches is decoded and the appropriate switch is turned on.

The EN latch allows all switches to be turned off under program control. This becomes useful when two or more DG428s are cascaded to build 16-line and larger multiplexers.

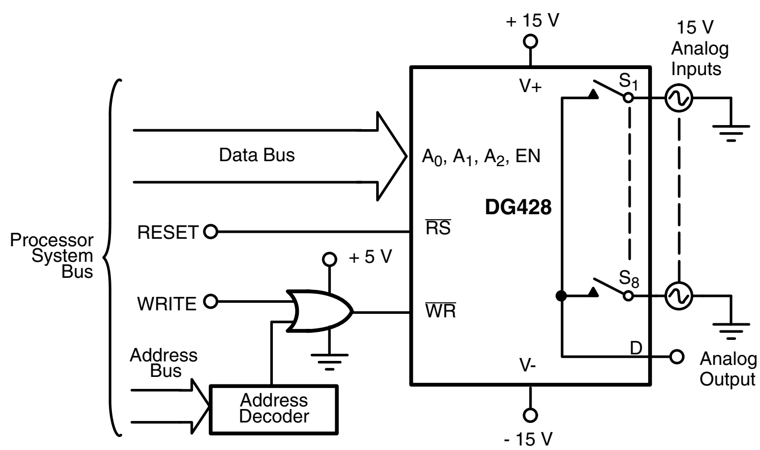
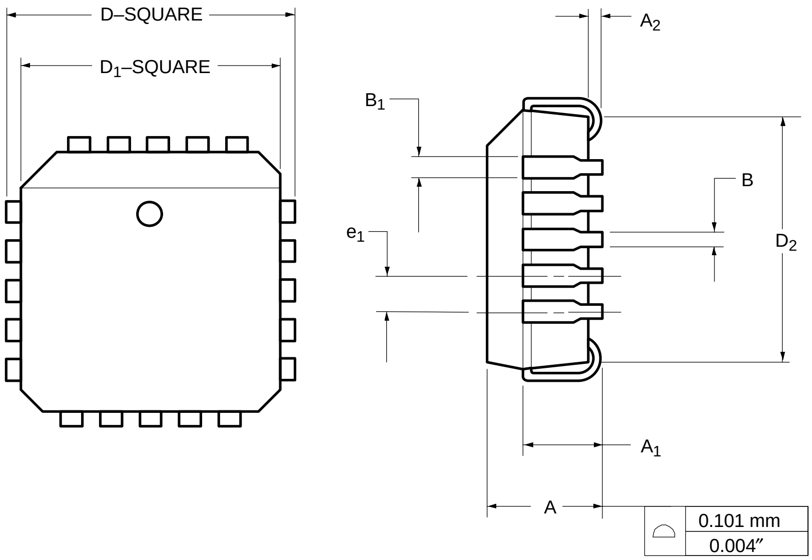


Figure 10. Bus Interface

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70063.

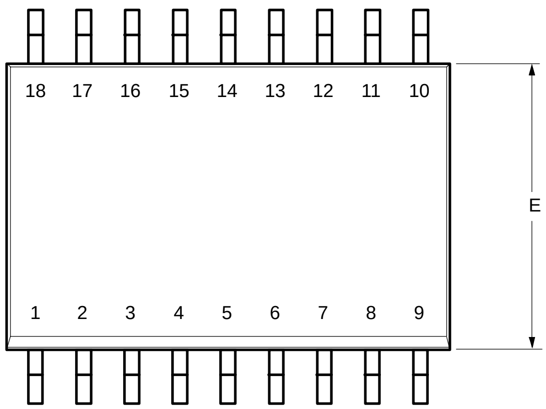
PLCC: 20-LEAD



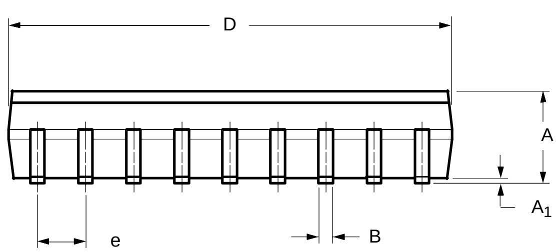
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.20	4.57	0.165	0.180
A_1	2.29	3.04	0.090	0.120
A_2	0.51	–	0.020	–
B	0.331	0.553	0.013	0.021
B_1	0.661	0.812	0.026	0.032
D	9.78	10.03	0.385	0.395
D_1	8.890	9.042	0.350	0.356
D_2	7.37	8.38	0.290	0.330
e_1	1.27 BSC		0.050 BSC	

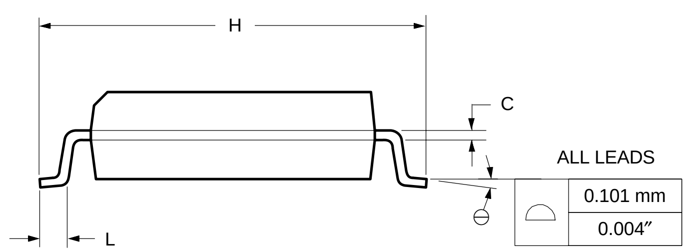
ECN: S-03946—Rev. C, 09-Jul-01
DWG: 5306

SOIC (WIDE-BODY): 18-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.15	2.90	0.085	0.114
A_1	0.10	0.30	0.004	0.012
B	0.35	0.45	0.014	0.018
C	0.23	0.28	0.009	0.011
D	11.25	12.45	0.443	0.490
E	7.25	8.00	0.285	0.315
e	1.27 BSC		0.050 BSC	
H	9.80	10.60	0.386	0.417
L	0.60	1.00	0.024	0.039
θ	0°	8°	0°	8°
ECN: S-03946—Rev. C, 09-Jul-01 DWG: 5302				





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