Designing A High-Frequency, Self-Resonant Reset Forward DC/DC For Telecom Using Si9118/9 PWM/PSM Controller

by Thong Huynh

FEATURES

- Fixed Telecom Input Voltage Range: 30 V to 80 V
- 5-V Output Voltage, 5-A Max., Total 25-W Continuous Power
- High Efficiency 500-kHz Switching Frequency
- Integrated Start-Up Circuitry
- Self-Resonant Reset
- Current Mode Control with Slope Compensation
- Optional Pulse Skipping Mode for Light Load Efficiency

DESIGN CALCULATION

Circuit parameter definition:

V_I:	Input Voltage
V_O:	Output Voltage
I_O:	Output Current
L_O:	Output Inductor
N_P:	Power Transformer Primary Winding Number of Turns
N_S:	Power Transformer Secondary Winding Number of Turns
F_{SW}:	Switching Frequency
T_{SW}:	Switching Period
D:	Switching Duty Cycle in Percent

Power Transformer Design

Duty Cycle Range

The Si9118/Si9119 is capable of operating at up to 80% duty cycles, leaving adequate margins for leakage inductance effects and load transient response. Its >50% duty cycle capability reduces rms current in the transformer windings and the primary circuitry, thus reducing circuit conduction losses. For most circuits, the maximum duty cycle should be fixed at around 65% at the minimum input voltage.

The transformer turn ratio can be determined using the equation below:

$$\frac{N_S}{N_P} = \frac{(V_O + 0.5)}{V_{Im}} \cdot \frac{1}{DM} \quad (1)$$

Where:

V_{Im} is the minimum input voltage
DM is the maximum duty cycle chosen

Example: For V_O = 5 V. V_{Im} = 30 V, DM = 0.65 $\Rightarrow$ N_S/N_P = 0.28. Choose N_S = 7 and N_P = 22 gives N_S/N_P = 0.31 which give DM = 60%.

Self-Resonant Reset

After each switching duty cycle, the magnetizing current in the power transformer has to be reset to prevent core saturation. Traditional reset circuits use either an RCD dissipative clamp or a tertiary reset winding on the transformer. This type of circuit uses extra components and, in the case of the RCD clamp, also involves losses. The demo board for the Si9118/9119 features a self-resonant reset circuit which resets the magnetizing current and also recovers this magnetizing energy by charging it back to the input. The reset circuit consists of only parasitic elements and requires no additional external components. Detail operation of this circuit is beyond the scope of this application note. For this circuit to function properly, the primary inductance needs to satisfy the following equation:

$$LMp \le \frac{1}{C_R} \cdot \left[\left[1 - \frac{(V_o + 0.5) \cdot N_P}{V_{Im} N_S}\right] \cdot \frac{1}{Fsw \cdot \pi}\right]^2 \quad (2)$$

Where

$$C_R = C_{DS} + C_J \cdot \left(\frac{N_S}{N_P}\right)^2 \quad (3)$$

LMp is the primary winding magnetizing inductance
V_{Im} is the minimum input voltage
C_{DS} is the output capacitance of the main MOSFET switch
C_J is the junction capacitance of the output forward rectifier
C_{XFMR} is the power transformer primary winding capacitance

This equation ensures that the resonant reset circuit is fast enough to reset the core magnetizing current within the off-time of each period. The worst-case condition for reset is at low-line, light-load, and maximum switching frequency.

For high-frequency operation, the power transformer core can be gapped to obtain the required LM_p.

Example: For C_{DS} = 100 pF, C_{XFRM} = 10 pF. C_J = 200 pF, N_P = 22, N_S = 7, V_{Im} = 30 V, and F_{SW} = 500 kHz, LMp must be equal or less than 559 µH.

Selecting Core and Wire Size

Once the duty cycle range and the primary inductance values are determined, the core and wire size of the transformer should be selected to handle power and efficiency requirements.

Design example:

For this application, a Phillips EFD core in 3F3 material was chosen. The EFD core is a low-profile version of E core. It is well suited for cost conscious designs in low-profile applications. The 3F3 material, furthermore, is a good choice for a switching frequency of 500 kHz. To select the core size, an approximation can be made using the WaAc product. The equation below, provided in the Magnetics Inc. ferrite cores selection guide, can be used for this purpose:

$$WaAc = \frac{Po \cdot C \cdot 10^8}{4 \cdot E \cdot B \cdot f \cdot K} \quad (4)$$

Where:

Wa is the winding area in cm^2
Ac is the core area in cm^2
P_O is the output power in W
C is the current capacity in cm^2/A, C = 0.00507 for square wave and E core
E is transformer efficiency
B is flux density in Gauss
F is operating frequency in Hz
K is winding factor

Choosing E = 90%, B = 500 Gauss, K = 80%, results WaAc = 0.0176 cm^4, select a core with WaAc product of at least 0.0176 cm^4. Phillips EFD15, which has WaAc of 0.025 cm^4, is a good choice for this application.

Output Inductor Design

Four factors affect the design of the output inductor:

- Maximize inductor current slew rate during load transient
- Minimize amount of ripple current
- Minimize discontinuous conduction mode boundary
- Meeting current and power rating

A good compromise is to design the ripple current to be around 20% to 30% of the maximum output current. The following equation determines the inductance value to give a worst-case ripple current of 25%.

$$L_O = \left(1 - \frac{V_O \cdot N_P}{V_{IM} \cdot N_S}\right) \cdot \frac{V_O}{0.25 \cdot I_O \cdot F_{SW}} \quad (5)$$

Where:

L_O is the required output inductance at maximum load current
V_{IM} is the maximum input voltage
I_O is the maximum dc output current

Choosing a larger inductor value will result in a smaller ripple current and a lower DCM boundary, but it will also reduce the inductor current slew rate and increase the core size. The core type, size, and wire gauge can then be selected to suit current and power requirements. Most magnetics manufacturers have design guidelines for selecting core sizes, wire sizes, and core materials. To specify an inductor, the following criteria should be included:

- Minimum inductance at maximum output current, given in the above equation.
- Maximum peak current. This is the maximum output current plus one half of the peak-to-peak ripple current. The ripple current is dependent on the inductance given above, which assumes a ripple current of 25% of maximum output current. So, the peak current is 1.125 times the maximum dc output current.
- Peak-to-peak ac ripple current. This is 25% of the maximum output current if the above equation is used. The ac ripple current determines the ac flux swing in the inductor core, which causes core loss.
- Power loss. The inductor power loss has two parts. The first part is dc loss, which is the series dc resistance of the inductor winding multiplied by the square of the output current. The second part is the core loss. The total power loss cannot exceed the desired efficiency or the temperature rise limit, whichever comes first. A temperature rise limit is typically set at 50°C. There is some ac resistance loss due to the ripple current. This loss is small and is not included here for simplicity.

Design example:

V_O = 5 V, I_O max = 5A, F_{SW} = 500 kHz, V_I max = 80 V, N_S = 7, N_P = 22.

From the equation above, L_O minimum required is: 6.4 µH
Maximum peak output current is 5 A + 12.5% = 5.625 A
Peak-to-peak ac ripple current is 25% of 5 A = 1.25 A

For this output filter inductor application at high dc bias and high switching frequencies, the core material must have high-flux-saturation and low-loss characteristics. A Magnetics Inc. MPP core is suitable. A Kool-mu core would also be appropriate. The initial core size can be estimated using the LI^2 product and then comparing this with the manufacturer-recommended curve for core selection. An optimized design may require more than one iteration to satisfy each design need. For this example, a Magnetics Inc. MPP toroid, 125-µ core was chosen. The core part number is Magnetics Inc. 55030. Using 13 turns of 2 x 25 awg wire would give the desired inductance.

Inductor performance summary: Inductance at zero bias is 8.8 µH; at 5.625-A bias it is 4.8 µH. Magnetizing force at 5.625 A is 50 Oersted. Series resistance is ≈10 MΩ, which causes a dc power loss at 5 A of 250 mW. The ac magnetic flux swing is 750 Gauss, which results in core losses at 500 kHz of 166 mW. Total power loss in this inductor is 416 mW. Temperature rise, measured at room ambient, is ≈50°C.

Current Slope Compensation (Si9118 only)

Slope compensation should be added to the current sense voltage to provide optimal feedback loop compensation, to improve noise immunity, and to stabilize operation for duty cycles greater than 50%.

The Si9118 simplifies slope compensation by providing a buffered ramp signal, V_{SC}. Using V_{SC} with two external resistors accomplishes the slope compensation task. The figure below shows the recommended slope compensation configuration. R_2 can be calculated using the following equation for optimum control:

$$R_2 = \frac{N_S}{N_P} \cdot R_{IS} \cdot \frac{(V_O - 0.5)}{L_O} \cdot \frac{1}{4 \cdot F_{SW}} \cdot R_1 - R_F \quad (6)$$

Where:

L_O is the minimum output inductance at full load,

R_1 should be between 40 kΩ and 100 kΩ

This equation is designed for M_C = 2, meaning that a slope compensation of one times the inductor current down slope is being added to the current sense voltage at the Ics pin. An M_C of 2 is the critical slope compensation where peaking of the control to output gain at one half of the switching frequency is critically damped. Critical current slope compensation stablizes the current loop while while maintaining the phase lift advantage of current mode control for optimizing the voltage loop compensation.

The I_{CS} pin is used to feedback the primary current information to be used solely by the control loop. While I_{LIM} is used to detect current limit and PSM threshold.

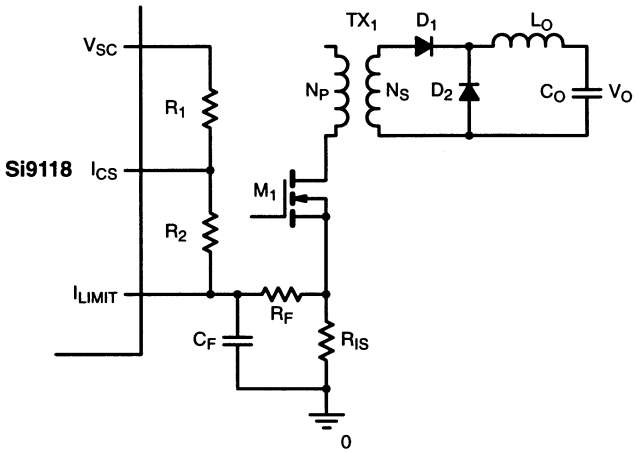


FIGURE 1.

Set Current Limit

The Si9118/9 peak current limit threshold is set internally at 600 mV. When the voltage at the I_{LIM} pin reaches this threshold, the gate drive pulse is terminated immediately until the next cycle. R_{IS} is used to set the primary pulse by pulse peak current limit. R_{IS} can be calculated using the following equation:

$$R_{IS} = \frac{N_p}{N_S} \cdot \frac{0.6}{I_{OLIM} \cdot 1.125} \quad (7)$$

Where:

I_{OLIM} is the desired output current limit threshold,

The factor 1.125 takes into account the output ripple current effect, assuming a 25% ripple current was designed. A higher value of R_{IS} reduces the output current limit and vice versa.

A low pass filter can be added to the current sense voltage to suppress high-frequency noise. To avoid an excessive phase lag on the current sense signal, the low pass filter corner frequency should be at least a decade above the switching frequency.

$$\frac{1}{2 \cdot \pi \cdot R_F \cdot C_F} \geq 10 \cdot Fsw \quad (8)$$

R_{IS} also sets the PSM threshold level as described in the PWM vs PSM section.

Synchronization (Si9119 only)

The Si9119 features a frequency synchronization pin. For synchronous operation among several Si9119 controllers, simply connect the SYNC pins together. The system switching frequency is determined by the fastest controller. The clock is synchronized with the falling edge. An unused SYNC pin should be left open.

Set Maximum Duty Cycle

The voltage on the D_{MAX} pin limits the duty cycle. The default voltage on D_{MAX} is 3.2 V which corresponds to 80%. Pulling the D_{MAX} pin to voltages larger than 3.2 V is not recommended. The maximum duty cycle can be calculated using the following equation:

$$D_{MAX} = \frac{1}{4} \cdot V_{DMAX} \quad (9)$$

Resistors R_9 and R_{10} on the demo board are provided for convenient maximum duty cycle programming. D_{MAX} can be calculated using R_9 and R_{10} ratios as follows:

$$D_{MAX} = \frac{R_9}{R_9 + R_{10}} \quad (10)$$

PWM vs. PSM

For high-efficiency operation at light load conditions, a Pulse Skipping Mode feature is included in the Si9118/9. Pulling the PWM/$\overline{\text{PSM}}$ to ground activates this feature. In PSM mode, the peak current information seen on the I_{LIM} pin for each pulse is forced to reach 100 mV during light load conditions. The excess energy forces the consecutive pulses to be skipped and results in frequency fold back operation. At lower switching frequencies, switching losses are greatly reduced and the efficiency of the converter is thus boosted. At higher load currents, the controller automatically switches back to PWM mode.

JMP1 on the demo board provides a convenient PWM/PSM configuration.

Start-up and House Keeping Supply

Start-up circuitry is integrated into the controller. When V_{IN} reaches 8.6 V, an internal depletion MOSFET charges up V_{CC}, allowing a self-start sequence. An external housekeeping source is needed to maintain V_{CC} once the converter has started running. A simple low-current housekeeping circuit is used on this demo board as shown on the schematic.

For low power and/or low frequency operation that requires V_{CC} current <8 mA, there is no need for an external housekeeping source, provided that the total power dissipation in the IC does not exceed the specification limit.

Buffer Driver

A totem pole buffer driver is included in this demo board for better switching. While this is an optional feature, buffer drivers are recommended for driving larger MOSFETs.

Control Loop Compensation

Since this design features a current mode controlled forward converter with slope compensation, a Type II compensation circuit is adequate for the feedback loop compensation. See the Control Loop section, for measured loop gain results.

DESIGN PERFORMANCE

The converter was designed on a double-sided surface-mount FR4 board. All components are surface-mount except the electrolytic capacitors. The schematic, bill of materials, and board layout artwork are included in the demonstration board data sheet (Si9118/9DB). Following are measurement results of the converter performance.

Efficiency

The Figures 2 through 7 below show the measured efficiency. Notice the extra efficiency gain at light load when the PSM mode is used. At high line voltage condition, the switching losses are higher and hence significant PSM efficiency improvement. Efficiency exceeding 80% is achieved at output loading over 1 A. Peak efficiency is 84% at ≈2.5-A loading.

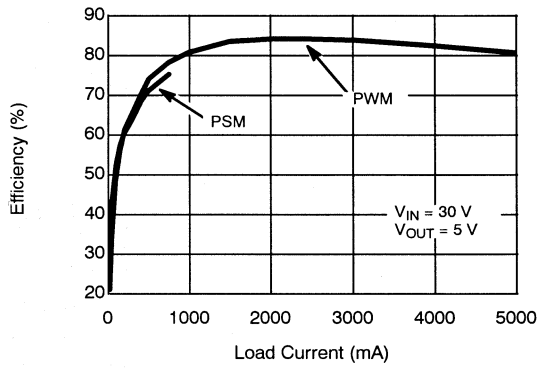


FIGURE 2. PSM and PWM Efficiency vs. Load Current

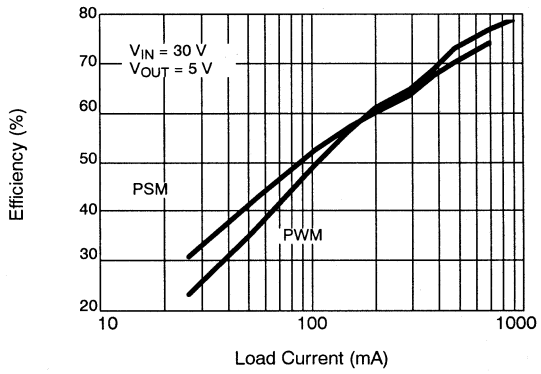


FIGURE 3. PSM and PWM Efficiency vs. Load Current

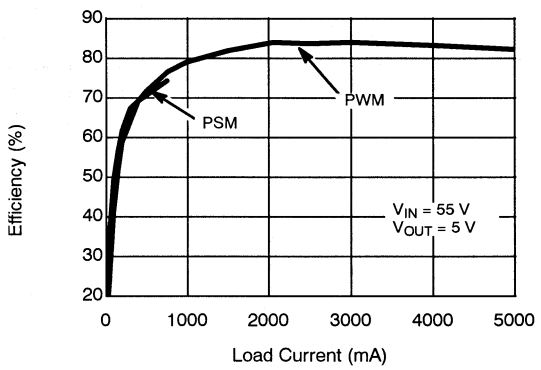


FIGURE 4. PSM and PWM Efficiency vs. Load Current

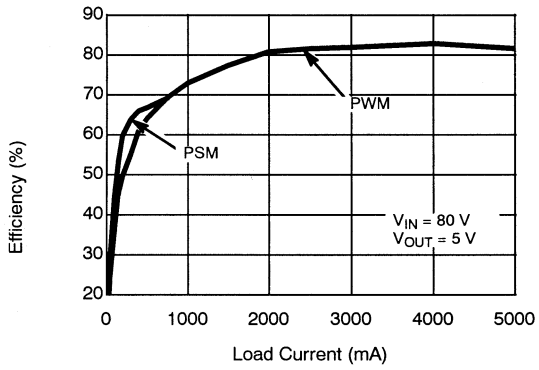


FIGURE 6. PSM and PWM Efficiency vs. Load Current

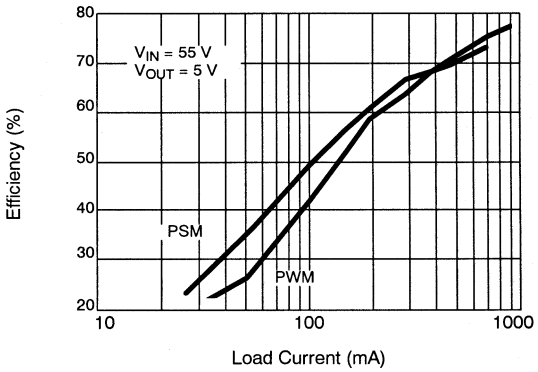


FIGURE 5. PSM and PWM Efficiency vs. Load Current

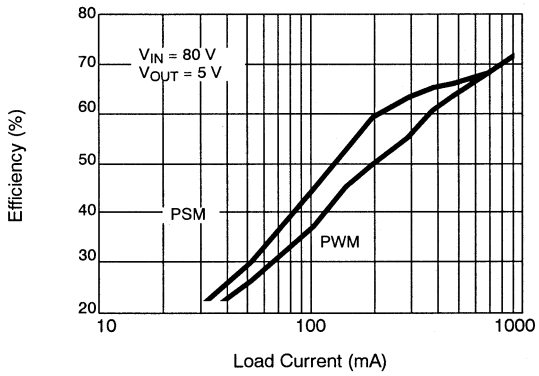


FIGURE 7. PSM and PWM Efficiency vs. Load Current

Output Regulation

Figure 8 shows the output voltage at various input voltages and load conditions in both PWM and PSM operation modes. Load and line regulation is a quarter of a percent for both modes.

V_O minimum = 5.016 V, V_O maximum = 5.041 V,
V_O mean = 5.029, V_O tolerance = ±0.25%

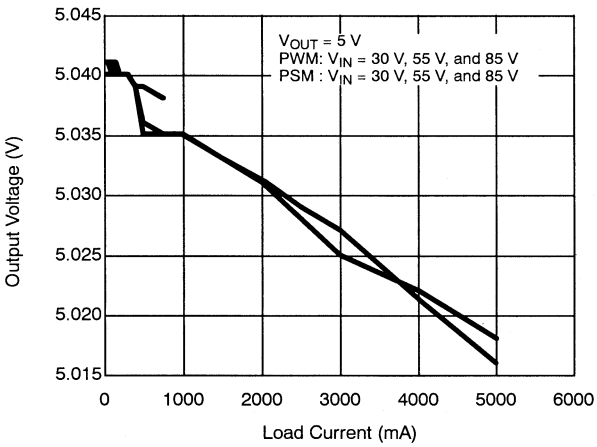
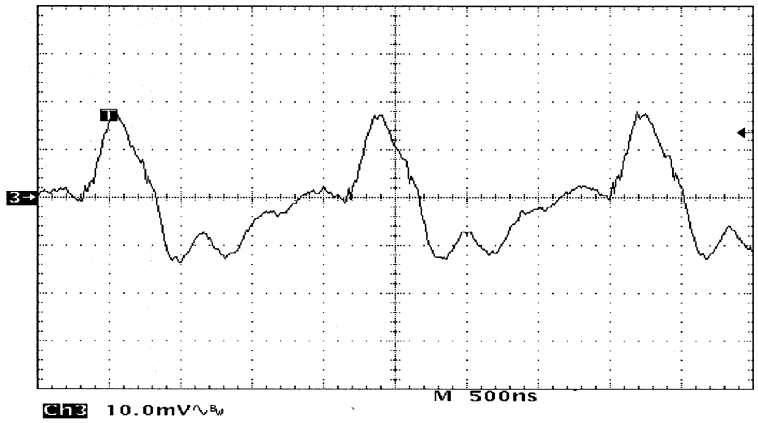


FIGURE 8. Output Regulation vs. Load Current

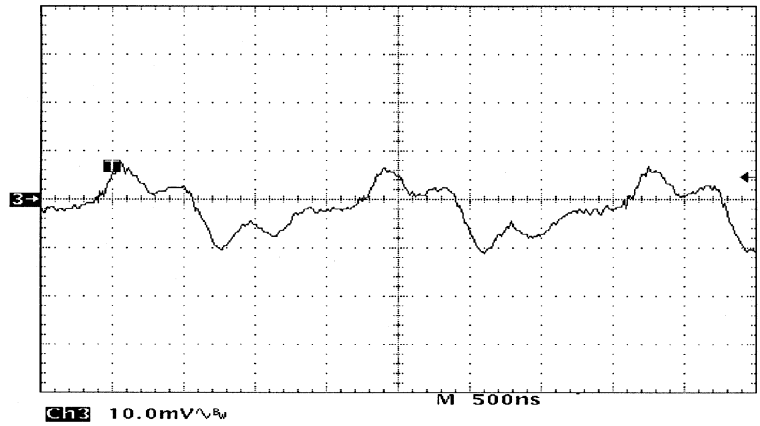
Output Ripple Voltage

Figures 9 and 10 show worst-case ripple voltage is 31.6 mV peak-to-peak at high line and maximum loads, including peak-to-peak noise voltage.



Output Ripple Voltage
Operating Condition: V_{IN} = 80 V, I_O = 5 A, 20 MHz BWL

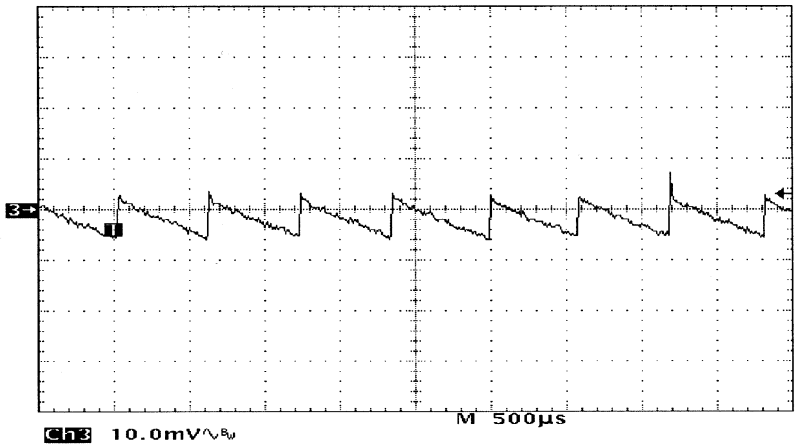
FIGURE 9.



Output Ripple Voltage
Operating Condition: V_{IN} = 48 V, I_O = 2.5 A, 20 MHz BWL

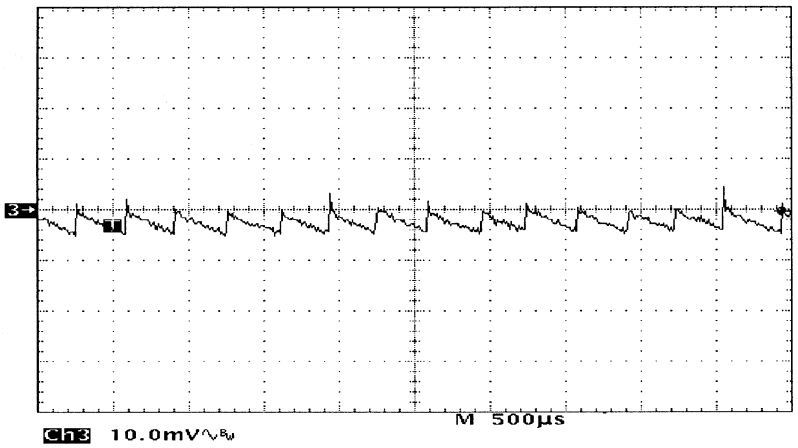
FIGURE 10.

Figures 11 and 12 show output voltage ripple during PSM operation. A worst-case output ripple voltage of 13.2 mV is seen during this condition.



Output Ripple Voltage During PSM Operation
Operating Condition: V_{IN} = 80 V, I_O = 0 A, 20 MHz BWL

FIGURE 11.

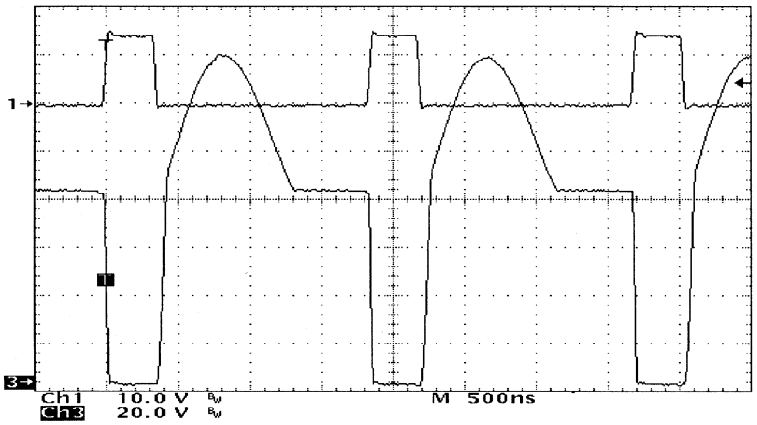


Output Ripple Voltage During PSM Operation
Operating Condition: V_{IN} = 30 V, I_O = 0 A, 20 MHz BWL

FIGURE 12.

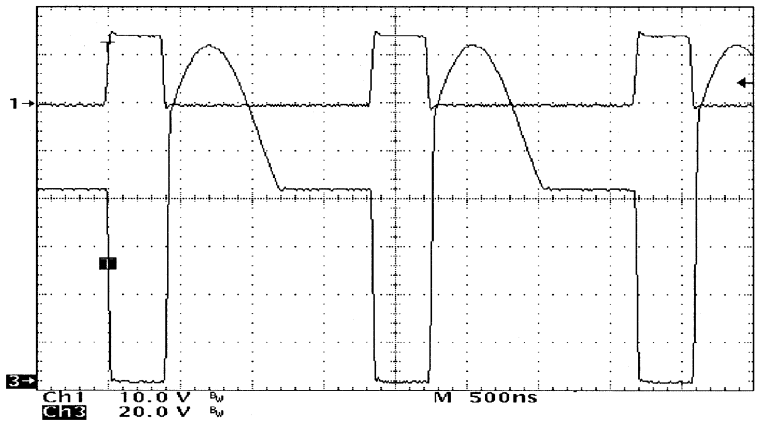
V_{DS} Resonant Voltage

Figures 13 through 21 show the drain-to-source voltage, V_{DS}, of the main power MOSFET switch. V_{DS} was measured with a TEK P5100 x 100 probe. The primary magnetizing inductance current is fully reset when V_{DS} is reset back to V_I. At this point, all of the magnetizing energy is fully recovered. At very low line and light loads, V_{DS} is not fully reset and some of the magnetizing energy will be lost. To improve this condition, a lower power transformer primary inductance is required.



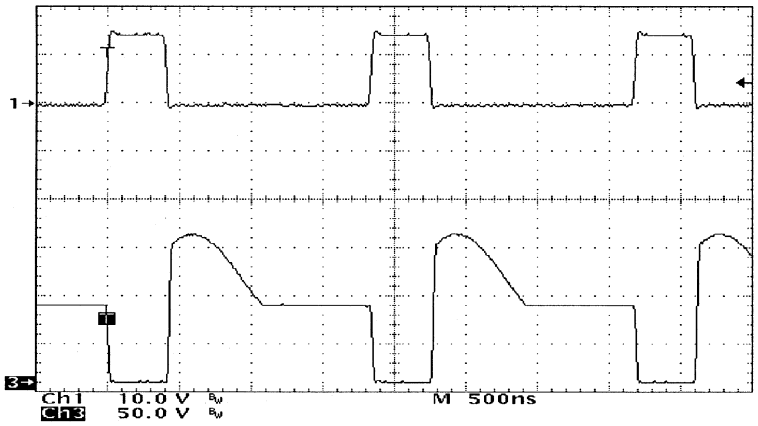
Ch1: Gate-Source Voltage
Ch3: Drain-Source Voltage
Operating Condition: V_{IN} = 80 V, I_O = 0.5 A

FIGURE 13.



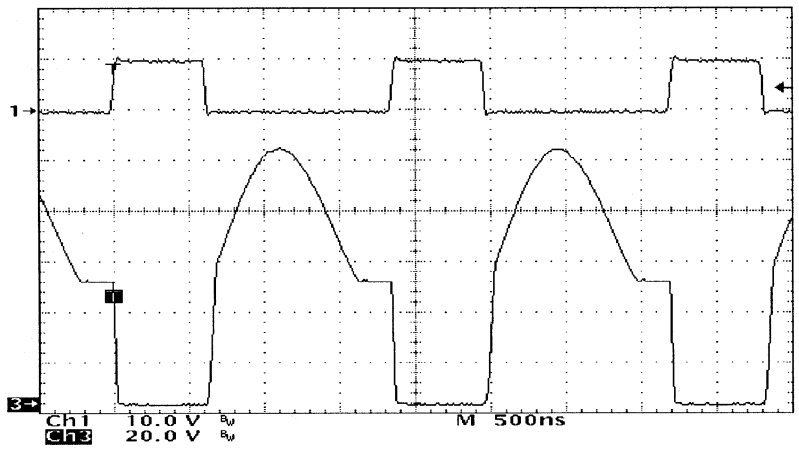
Ch1: Gate-Source Voltage
Ch3: Drain-Source Voltage
Operating Condition: V_{IN} = 80 V, I_O = 2.5 A

FIGURE 14.



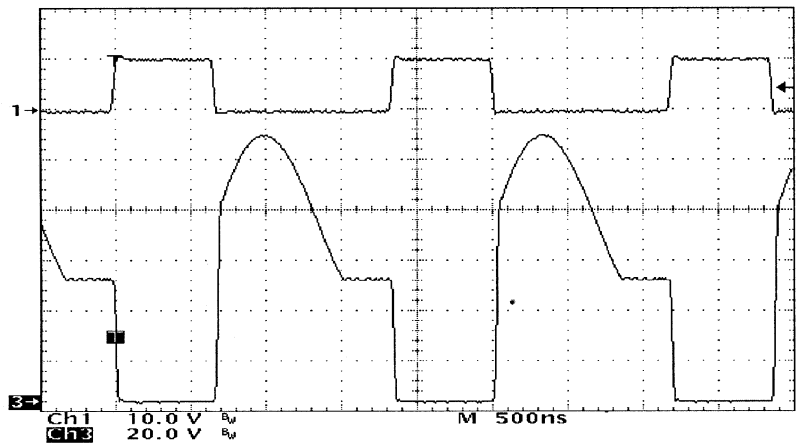
Ch1: Gate-Source Voltage
Ch3: Drain-Source Voltage
Operating Condition: V_{IN} = 80 V, I_O = 5.0 A

FIGURE 15.



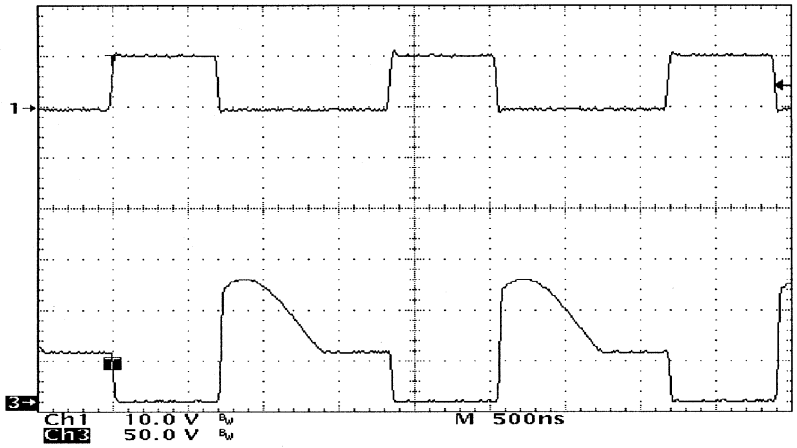
Ch1: Gate-Source Voltage
Ch3: Drain-Source Voltage
Operating Condition: V_{IN} = 48 V, I_O = 0.5 A

FIGURE 16.



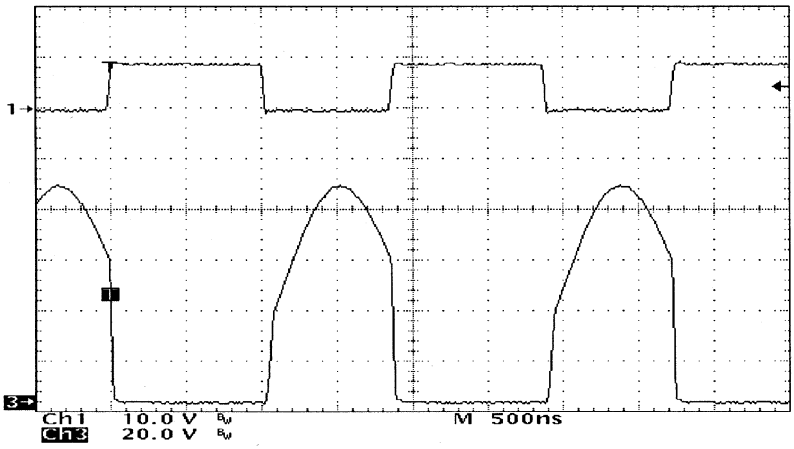
Ch1: Gate-Source Voltage
Ch3: Drain-Source Voltage
Operating Condition: V_{IN} = 48 V, I_O = 2.5 A

FIGURE 17.



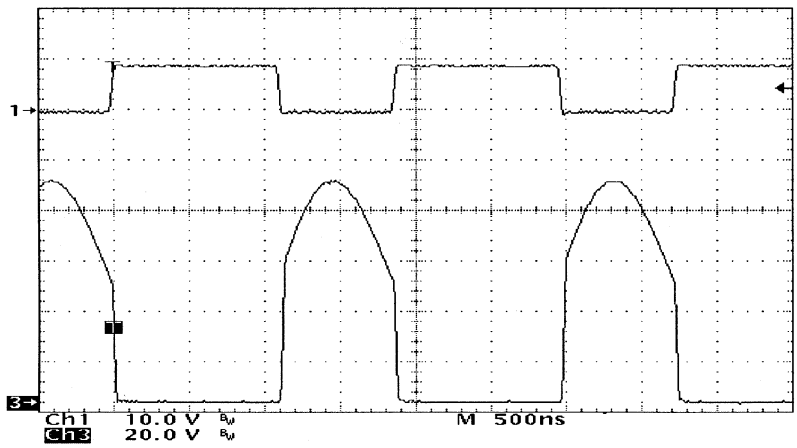
Ch1: Gate-Source Voltage
Ch3: Drain-Source Voltage
Operating Condition: V_{IN} = 48 V, I_O = 5.0 A

FIGURE 18.



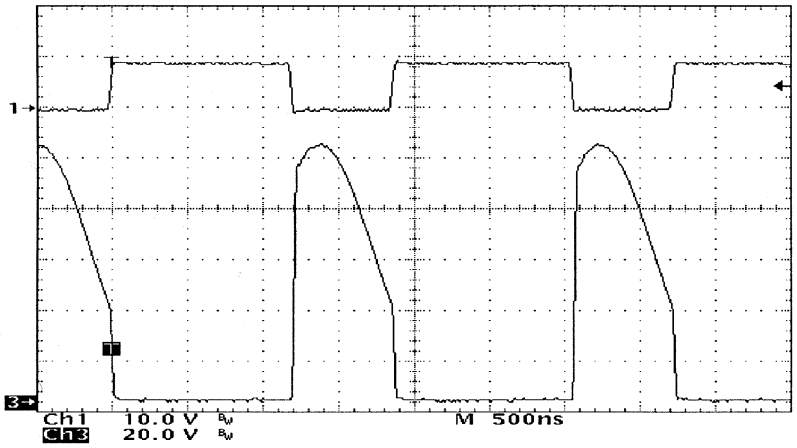
Ch1: Gate-Source Voltage
Ch3: Drain-Source Voltage
Operating Condition: V_{IN} = 30 V, I_O = 0.5 A

FIGURE 19.



Ch1: Gate-Source Voltage
Ch3: Drain-Source Voltage
Operating Condition: V_{IN} = 30 V, I_O = 2.5 A

FIGURE 20.



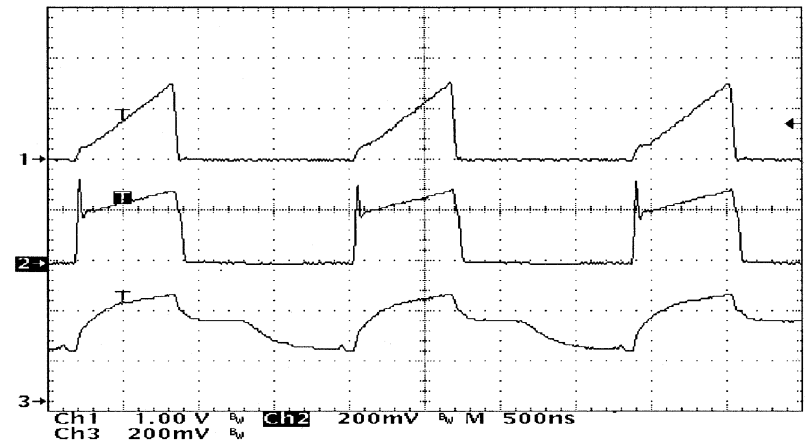
Ch1: Gate-Source Voltage
Ch3: Drain-Source Voltage
Operating Condition: V_{IN} = 30 V, I_O = 5.0 A

FIGURE 21.

Miscellaneous Waveforms

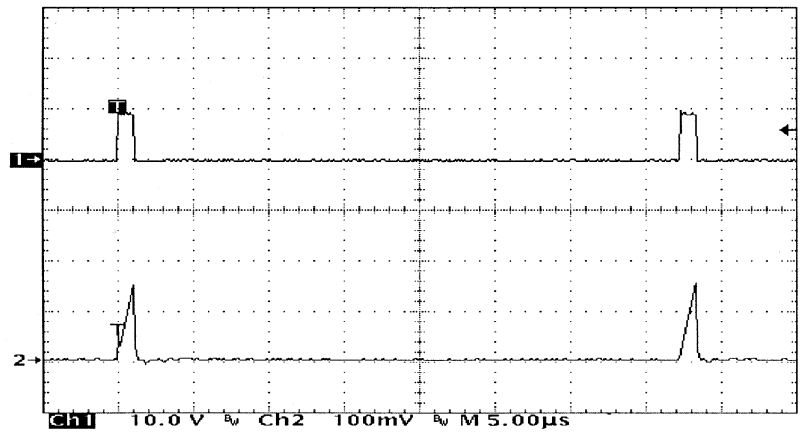
Figure 22 shows typical voltage waveforms at the V_{SC}, LIM, and I_{CS} pins. Notice that I_{CS} voltage is not a direct addition of I_{LIM} and V_{SC}. I_{CS} is an input of a high-speed current comparator. This comparator sources a non linear current through the I_{CS} pin. To provide an optimum slope compensation value for the current signal, the equation mentioned in the slope compensation section must be used.

Figures 23 and 24 demonstrate the operation of PSM versus PWM mode. During PSM mode, at V_I = 48 V, I_O = 50 mA, the frequency is folded back to 26.8 kHz from 526 kHz. Switching losses are reduced to $^1/_{20}$ of that in PWM operation.



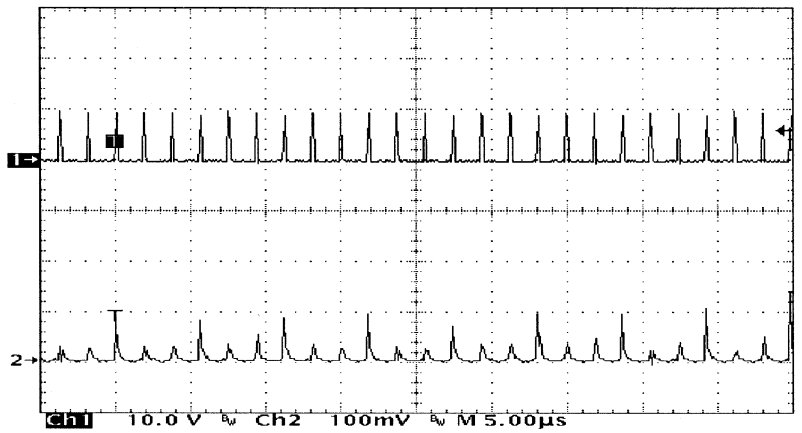
Ch1: V_{SC}
Ch2: I_{LIM}
Ch3: I_{CS}
Operating Condition: V_{IN} = 48 V, I_O = 2.5 A

FIGURE 22.



Ch1: Gate-Drive Voltage
Ch2: I_{LIM}
Operating Condition:
PSM Mode, V_{IN} = 48 V, I_O = 50 mA

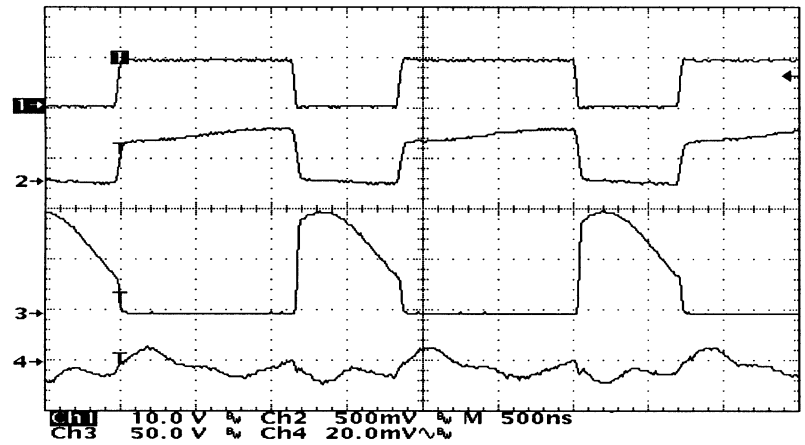
FIGURE 23.



Ch1: Gate-Drive Voltage
Ch2: I_{LIM}
Operating Condition:
PWM Mode, V_{IN} = 48 V, I_O = 50 mA

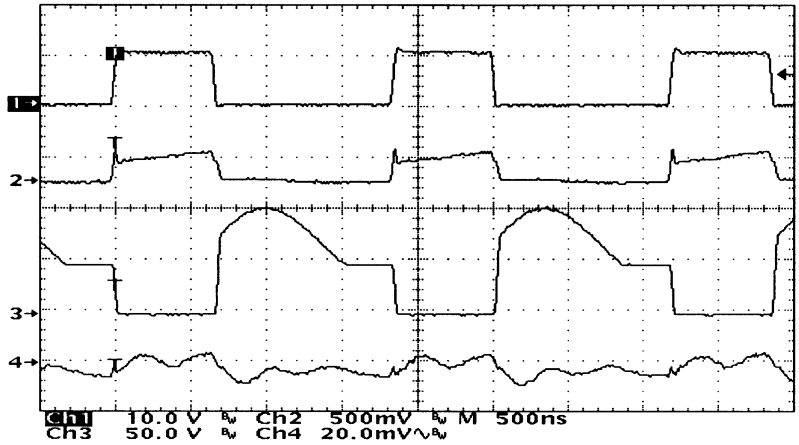
FIGURE 24.

Figures 25 and 26 show typical gate drive, output voltage ripple, primary current, and power switch drain-to-source voltage:



Ch1: Gate-Drive
Ch2: I_{LIM}
Ch3: Power Switch Drain-Source Voltage
Ch4: Output Ripple Voltage
V_{IN} = 30 V, I_O = 5 A, D = 62.8%

FIGURE 25.



Ch1: Gate-Drive
Ch2: I_{LIM}
Ch3: Power Switch Drain-Source Voltage
Ch4: Output Ripple Voltage
V_{IN} = 48 V, I_O = 2.5 A, D = 36%

FIGURE 26.

Control Loop

The following figures shows the control to output and loop gain bode plots of the converter. Figure 27 indicates a current-controlled buck converter with current slope compensation characteristics. The converter is stable with adequate gain and phase margins as shown on Figure 28. Due to the speed of the optocoupler used in this demo board, the loop crossover frequency is reduced to around 8 kHz. The low gain at low frequencies is also caused by the optocoupler's low frequency gain. For non-isolated design or with faster optocoupler, the crossover frequency can be optimized exceeding 40 kHz, as shown on Figure 29.

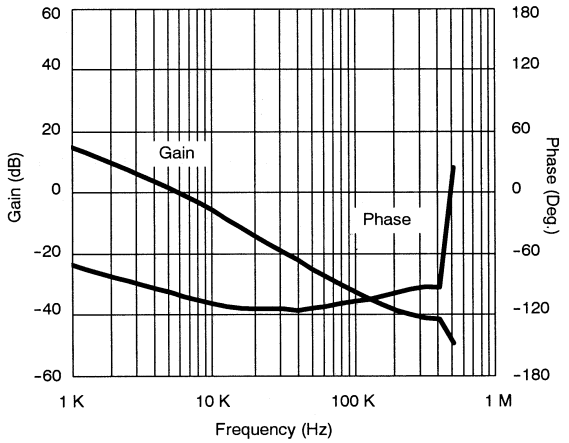


FIGURE 27. Control to Output, 50 V, 2.5 A

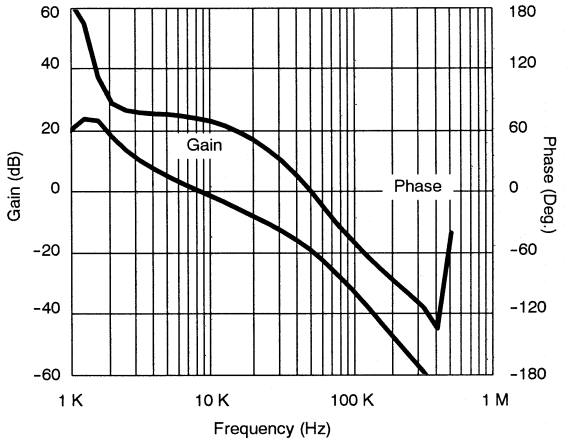


FIGURE 28. Loop Gain, 50 V, 2.5 A

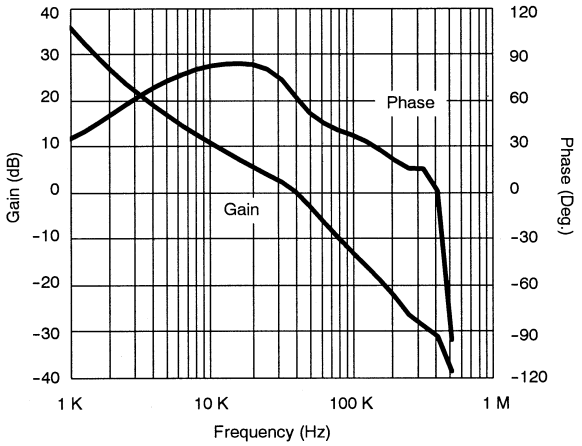
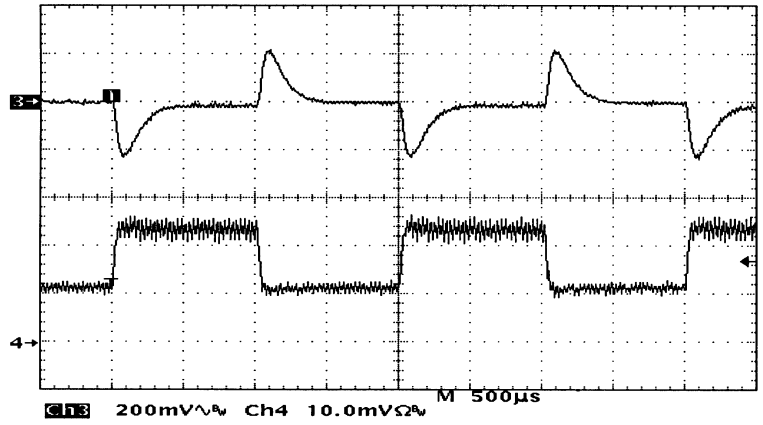


FIGURE 29. Loop Gain for Non-Isolated Version

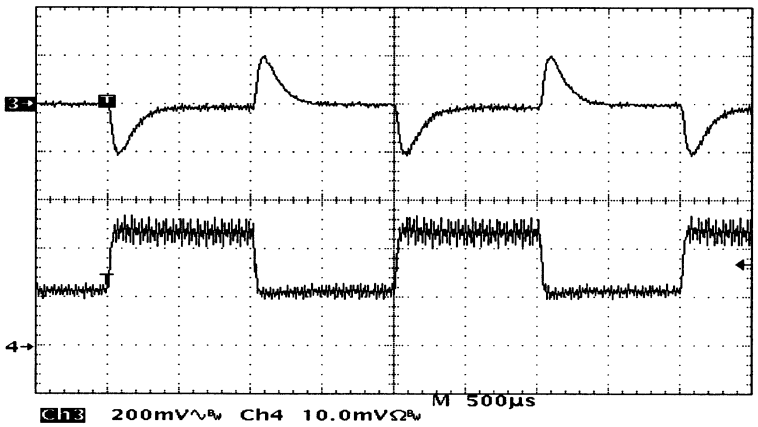
Load Step Response

Figures 30 through 32 show the output voltage response to a load step condition. With a crossover frequency of 8 kHz, the worst-case output voltage deviation is 228 mV nominal-to-peak, a 4.6% deviation from nominal output voltage. The voltage recovers nicely within 300 µs. The load step response performance can be further improved with a higher loop gain crossover frequency. As mentioned earlier, higher crossover frequencies are possible with faster optocouplers or when no input/output isolation is required. With very fast crossover frequency at 40.2 kHz, the load step response performance improves dramatically. Figure 33 shows only 35-mV peak voltage deviation and recovery time is only 150 µS.



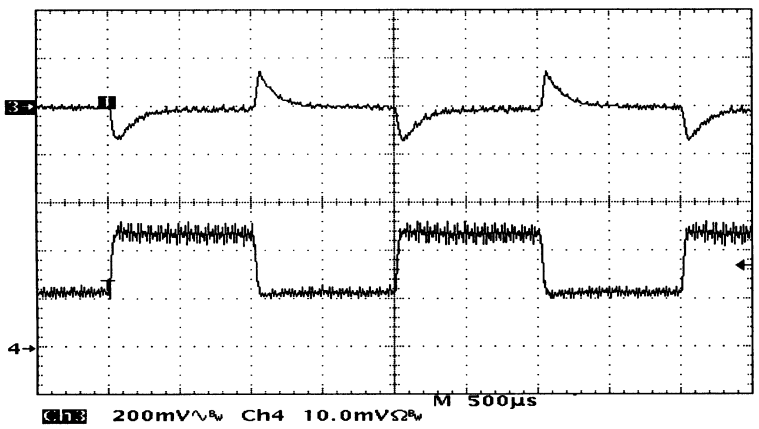
Ch3: Output Voltage Load Step Response
Ch4: Load Step Current, 2 A/div
Operating condition: V_{IN} = 30 V
I_O steps between 2.5 A – 5.0, $t_r = t_f$ = 50 µS
f_c = 8 kHz

FIGURE 30.



Ch3: Output Voltage Load Step Response
Ch4: Load Step Current, 2 A/div
Operating condition: V_{IN} = 48 V
I_O steps between 2.5 A – 5.0, $t_r = t_f$ = 50 µS
f_c = 8 kHz

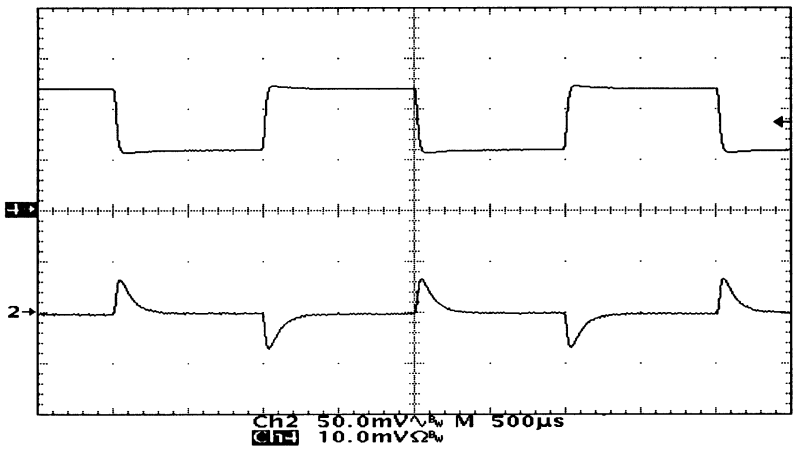
FIGURE 31.



Ch3: Output Voltage Load Step Response
Ch4: Load Step Current, 2 A/div
Operating condition: V_{IN} = 80 V
I_O steps between 2.5 A – 5.0, $t_r = t_f$ = 50 µS
f_c = 8 kHz

FIGURE 32.

Load step response with optimized loop gain cross over frequency of 40.2 kHz:



Ch2: Output Voltage Load Step Response
Ch4: Load Step Current, 2 A/div
Operating condition: V_{IN} = 48 V
I_O steps between 2.5 A – 5.0, $t_r = t_f$ = 50 µS
f_c = 40.2 kHz
Non-isolated

FIGURE 33.

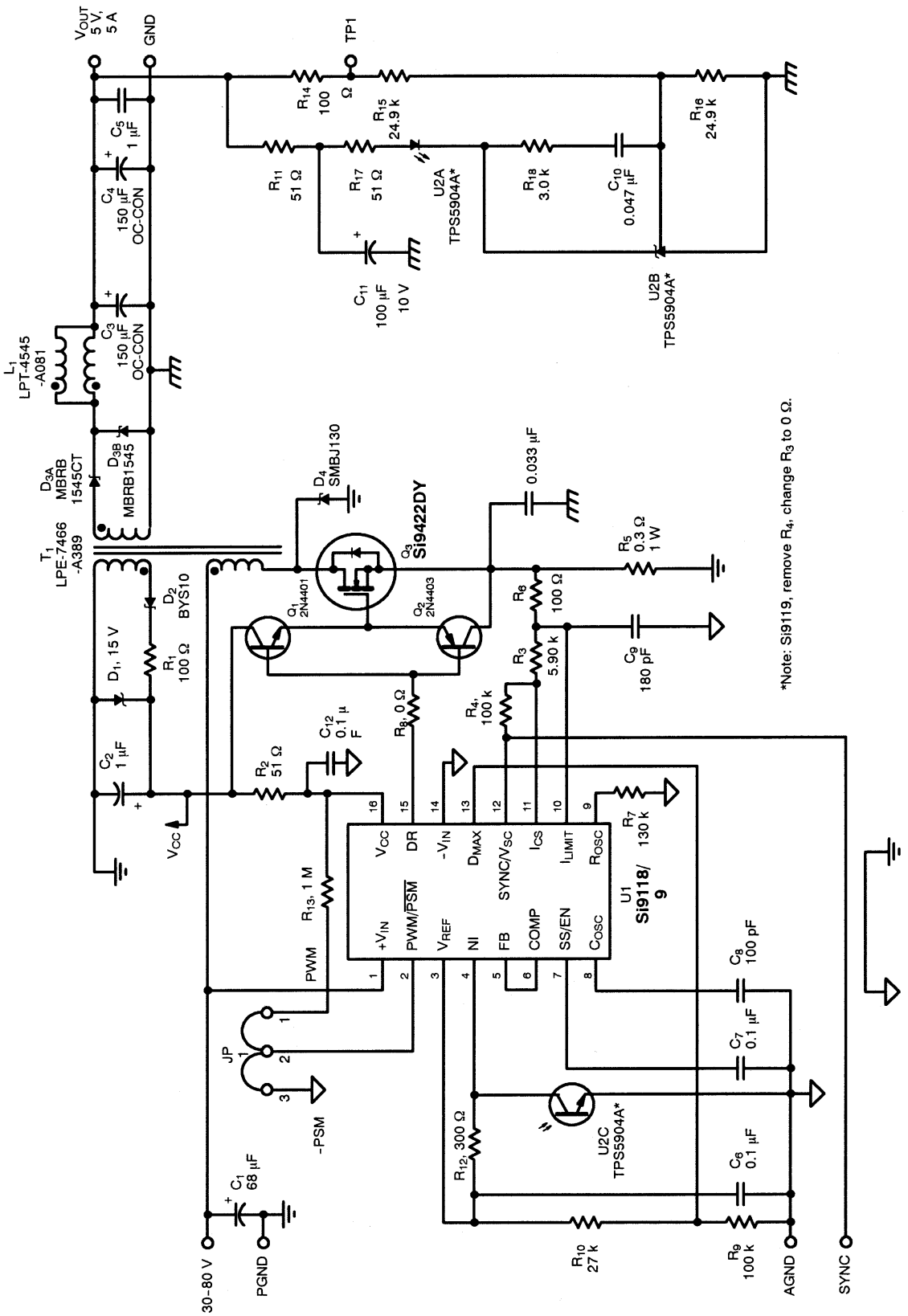


FIGURE 34. Application Circuit Schematic