PSM Buck Converter with Dynamic Adjustable Output and Bypass Capability

FEATURES

- 2.7-V to 6-V Input Voltage Range
- Dynamic Adjustable 1.5-V to 3.6-V Output.
- Power Conversion Efficiency of 95% at 170-mA Load
- Selectable Pulse Skipping Modulation (PSM) or Bypass Mode (BP) Operation
- Bypass for up to 800-mA Load
- Integrated MOSFET with Low External Part Count
- Low Quiescent Current–110 μA/250 μA (BP/$\overline{\text{PSM}}$)
- Shutdown Current <1 μA
- Integrated UVLO and POR
- Integrated Soft-Start
- Over Temperature Protection
- MSOP-10 Package

APPLICATIONS

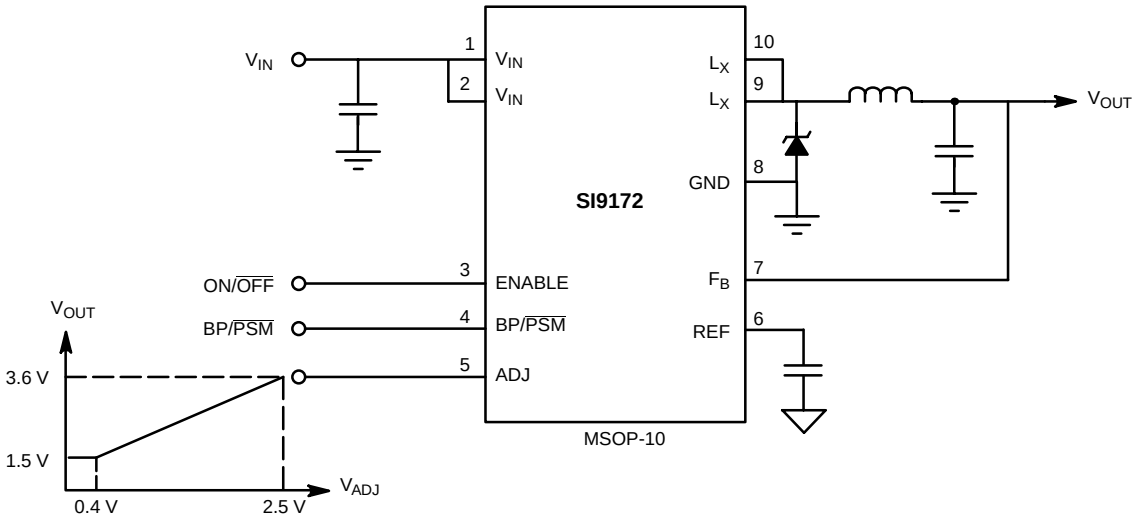
- Cellular Phones, Cordless Phones
- Computer Point of Use, Notebook
- PDAs
- Battery Powered Devices

DESCRIPTION

The Si9172 is a dual-mode power adjustable output converter. When it is set to PSM mode, the Si9172 operates as a pulse-skipping-modulation controlled step-down (buck) converter with a dynamically adjustable output of 1.5 V to 3.6 V. It has an integrated MOSFET, capable of supplying a minimum 170-mA load current with a 1.5-μH inductor. The output voltage is adjusted by the analog dc signal at the ADJ pin. The typical conversion efficiency is above 90%. A logic high at the BP/$\overline{\text{PSM}}$ pin puts the Si9172 in bypass mode. The main PMOS buck switch is forced to turn on at 100% duty cycle, overriding the FB signal. The voltage differential between input and output is the resistive voltage drop on the internal PMOS and the inductor. The Si9172 guarantees to deliver 800-mA load in bypass mode with a typical 95% efficiency.

The Si9172 is available in MSOP-10 package. In order to satisfy the stringent ambient temperature requirements, the Si9172 is rated to handle the industrial temperature range of –25°C to 85°C.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

V_{IN} . . . . . 6.5 V
BP/$\overline{PSM}$, ENABLE, F_B, L_X . . . . . –0.3 V to V_{IN} + 0.3 V
ADJ . . . . . V_{IN}
Peak Output Current . . . . . 1.5 A (1 ms)
Continuous Output Current . . . . . 1 A
Storage Temperature . . . . . –55 to 150°C
Operating Junction Temperature . . . . . 150°C

Power Dissipation (Package)[a]
10-Pin MSOP (Q Suffix)[b] . . . . . 825 mW
Thermal Impedance (Θ_{JA})
10-Pin MSOP . . . . . 150°C/W
Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6.6 mW/ °C above 25°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

V_{IN} . . . . . 2.7 V to 6 V
BP/PSM, ENABLE . . . . . 0 V to V_{IN}
REF Capacitor . . . . . 0.1 µF
Output Capacitor . . . . . 10 µF

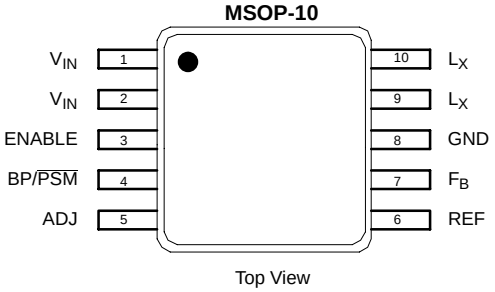
Inductor . . . . . 1.5 µH
PSM Load . . . . . 0 to 170 mA
Bypass Load . . . . . 0 to 800 mA

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified –25°C to 85°C 2.7 V ≤ V_{IN} ≤ 6 V	Limits Min[a]	Limits Typ[b]	Limits Max[a]	Unit
Output						
FB Threshold	V_{FB}	ADJ = 0.4 V	1.440	1.5	1.560	V
		ADJ = 2.5 V, V_{IN} ≥ V_{FB}	3.492	3.6	3.708	
Reference						
Output Voltage	V_{REF}	I_{REF} = 0	1.175	1.215	1.255	V
		I_{REF} = 0, T_A = 25°C	1.195	1.215	1.235	
Power Supply Rejection[c]	PSRR			60		dB
UVLO						
Under Voltage Lockout (turn-on)	V_{UVLD}		2.3	2.4	2.5	V
Hysteresis	$UVLD_{HYST}$			0.1		
Start-Up						
Start-Up Delay Time	t_{DELAY}			3		ms
Soft Start Time[c]	t_{ss}			100		µs
ENABLE, BP/$\overline{PSM}$						
Logic High	V_{IH}		1.5			V
Logic Low	V_{IL}				0.4	
Output Capability/MOSFET						
Maximum Bypass Output Current	I_{OUT}		800			mA
Maximum PSM Output Current		L = 1.5 µH	170			
MOSFET On-resistance	$r_{DS(on)}$	V_{IN} ≥ 3.3 V		150	300	mΩ
Supply Current						
BP Mode	I_{IN}	V_{IN} = 3.3 V		75	110	µA
PSM Mode[d]				190	250	
Shutdown Mode		V_{IN} = 3.3 V, ENABLE = 0 V			1	
Thermal Shutdown						
Threshold	$T_{S/D}$	Up-Rising		165		°C
Hysteresis	T_{HYST}	V_{IN} = 3.3 V		25		

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
c. Guaranteed by design and characterization, not subject to production testing.
d. For operation involving L_X frequency faster than 1-Hz the supply current may be higher.

PIN CONFIGURATION



ORDERING INFORMATION		
Part Number	**Temperature Range**	**Package**
Si9172BH-TI	–25°C to 85°C	Tape and Reel

Eval Kit	**Temperature Range**	**Board Type**
Si9172DB	–25°C to 85°C	Surface Mount

PIN DESCRIPTION

Pin No.	Name	Function
1, 2	V_{IN}	Input voltage source for buck converter, MOSFET driver, and IC control circuits.
3	ENABLE	Logic high enables the converter. Logic low shuts down the IC and decreases current consumed to <1 μA.
4	BP/$\overline{PSM}$	Logic high = Bypass mode, logic low = PSM mode.
5	ADJ	Analog voltage input to control output voltage
6	REF	1.215-V reference. Decouple with 0.1-μF capacitor.
7	F_B	Direct output voltage sense feedback
8	GND	IC ground
9, 10	L_X	Inductor connection node

TIMING WAVEFORMS

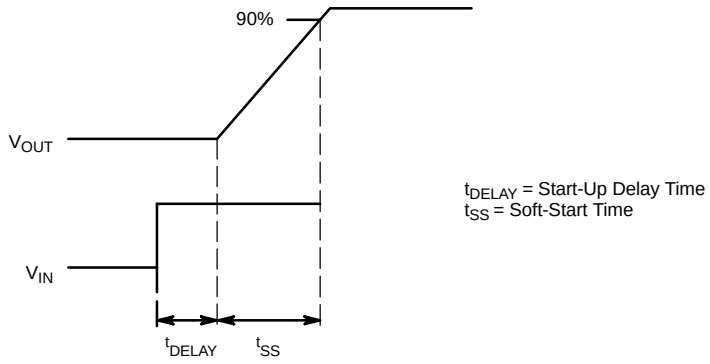
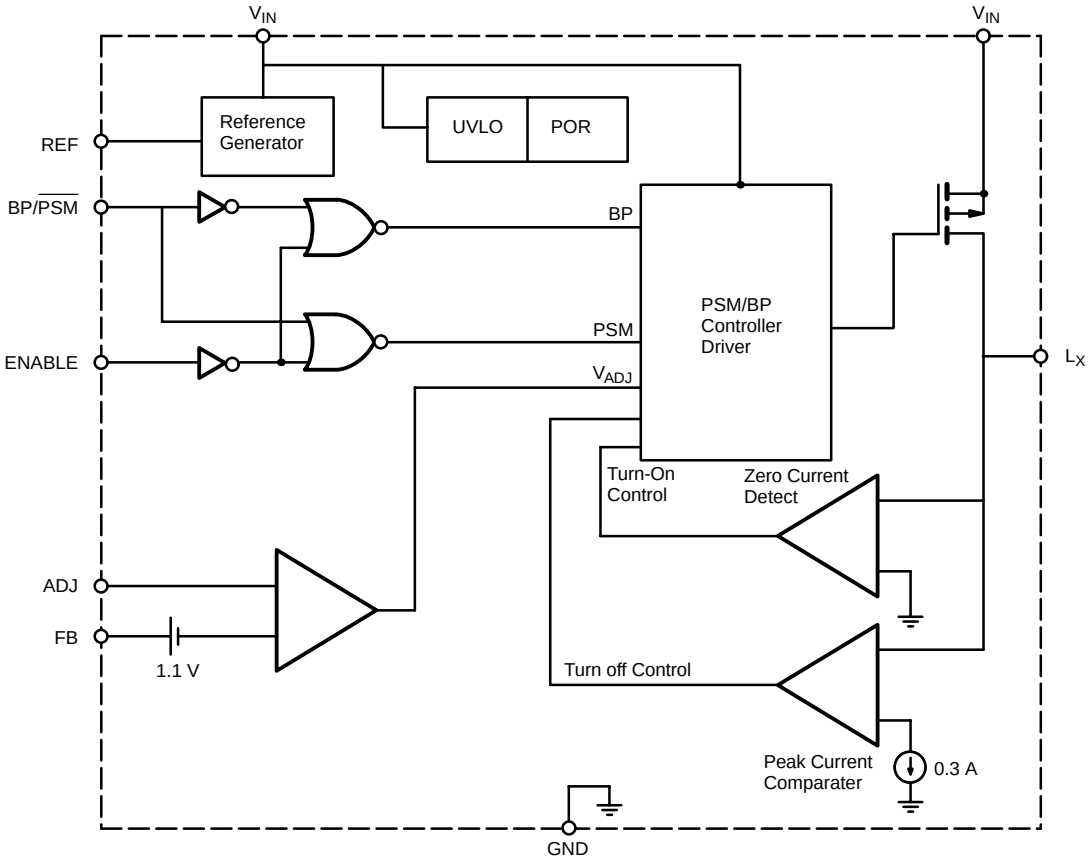


FIGURE 1.

FUNCTIONAL BLOCK DIAGRAM



DETAIL OPERATIONAL DESCRIPTION

Start-Up

The built-in UVLO circuit in the Si9172 prevents the internal MOSFET from turning on if the voltage on the V_{IN} pin is less than 2.4 V. With typical UVLO hysteresis of 0.1 V, the controller is continuously powered ON until the V_{IN} voltage drops below 2.3 V. This hysteresis prevents the converter from oscillating during the start-up phase and unintentionally locking up the system. Once the V_{IN} voltage exceeds the UVLO threshold, and with no other shutdown condition detected, an internal power-on-reset timer is activated. The circuitry, except the output driver, is turned on. After the POR time-out of about 3 ms, the soft-start begins. If pin 4 is in BP mode, the high side PMOS will turn on gradually in about 100 μs to avoid any inrush current. If pin 4 is in PSM mode, the converter will soft-start in PSM operation, forcing the output voltage to rise smoothly with minimum overshoot. The rise time is approximatly 100-μs. In order to start-up properly in PSM mode, the load current has to be 170 mA or less.

Pulse Skipping Mode

The gate charge losses produced from the Miller capacitance of the MOSFET are the dominant power dissipation parameter during light load. Therefore, reduced gate switching frequency improves overall converter efficiency. This is exactly why the Si9172 is designed to operate in pulse-skipping mode rather than PWM mode. If the BP/$\overline{\text{PSM}}$ pin is connected to logic low level, the converter runs in pulse skipping modulation mode. In this mode, the internal MOSFET operates with a constant on-time. The on-time is reduced if necessary by the peak current detector circuitry. There is an enforced minimum off-time acting as the feedback comparator blanking time. If the output voltage drops below the desired level, the main switch is first turned on and then off. If the applied on-time did not deliver enough energy to keep the output at the desired voltage level, the controller will force another on and off sequence, until the desired voltage is accomplished. If the applied on-time forces the output to exceed the desired level, the converter stays off. The excess energy is delivered to the output slowly, forcing the converter to skip pulses as needed to maintain regulation. The on-time and off-time are set internally based on the inductor value (1.5 μH Typical) and maximum load current. With a 1.5-μH inductor, the Si9172 guarantees to deliver minimum of 170-mA load current. This current capability decreases as the inductance increases. In pulse-skipping mode, the switching frequency, f_{sw}, varies with load current. When the load increases, f_{sw} increases as well. The typical conversion efficiency in PSM mode is 90%. Efficiency is higher at high output voltage and decreases with the output voltage.

Adjustable Output

In PSM mode, the output voltage regulation point can be adjusted by an external analog voltage signal at the ADJ pin. When this voltage varies from 0.4 V to 2.5 V, the output voltage also increases linearly from 1.5 V to 3.6 V. When the programmed output voltage is higher than the input voltage can support, the converter will be in drop out mode and the output voltage will be the input voltage minus the resistive drop of the MOSFET and inductor.

BYPASS Mode

The Si9172 can also operate in Bypass mode to handle heavy load current. In this mode the IC ignores the feedback signal at the FB pin, forcing the internal PMOS to turn on at 100% duty cycle. The input-output voltage differential is merely the resistive voltage drop on the MOSFET and the inductor. The Si9172 can bypass at least 800mA at 95% typical efficiency. Whenever the converter enters BP mode, regardless switching from PSM or starting up, the PMOS turns on gradually within 100 μs.

Shutdown

The Si9172 is designed to conserve as much battery life as possible by decreasing current consumption of the IC during normal operation as well as the shutdown mode. With logic low level on the ENABLE pin, the current consumption of the IC is decreased to less than 1 μA by shutting off most of the circuits. A logic high enables the controller and starts up as described in the “Start-Up” section above.

Reference

The reference voltage of the Si9172 is set to 1.215 V. It is internally connected to the non-inverting inputs of the error amplifier. A 0.1-μF decoupling capacitor is required at the V_{REF} pin.

Power Switches

The main MOSFET switch is integrated in the Si9172 for optimum performance and minimum overall converter size. The internal MOSFET is designed to minimize the gate charge loss as well as the conduction loss. The typical on-resistance of the PMOS is 150 mΩ with a minimum V_{IN} pin voltage of 3.3 V.

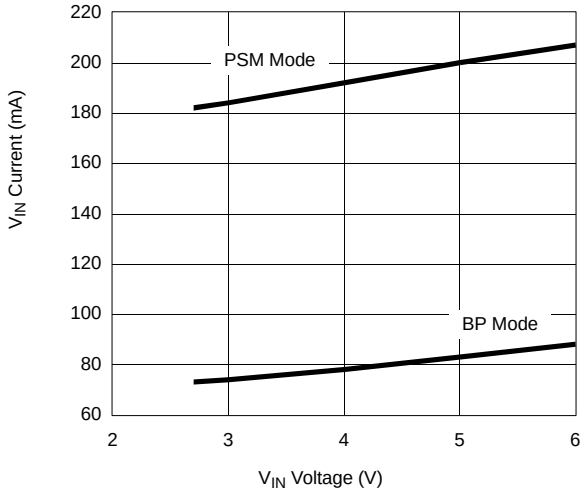
An external Schottky diode is mandatory for PSM mode operation. It freewheels the inductor current after the main switch is turned off, which is typical in basic non-synchronous buck converter operation. It must be rated at 800 mA or higher, with low forward drop to minimize power loss. The diode has to be connected at PGND with the cathode connected to the L_X pin.

Over Temperature Protection

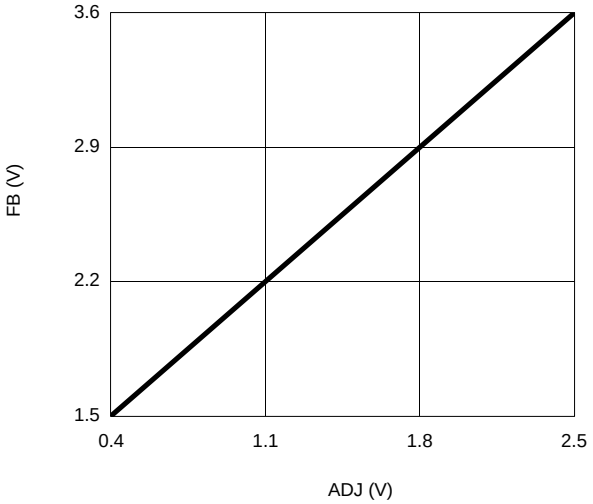
The Si9172 includes an over temperature protection circuit to prevent thermal runaway in the MOSFET switch. If the temperature reaches 165°C, an internal soft-start capacitor is discharged, shutting down the output stage. The converter remains in the disabled mode until the temperature in the IC decreases below 140°C.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

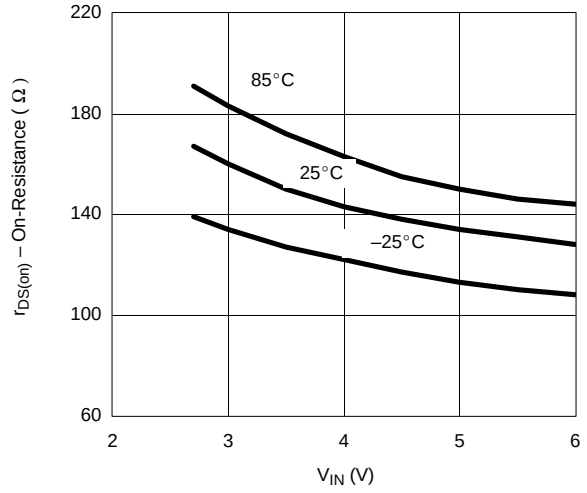
V_{IN} Current vs. V_{IN} Voltage



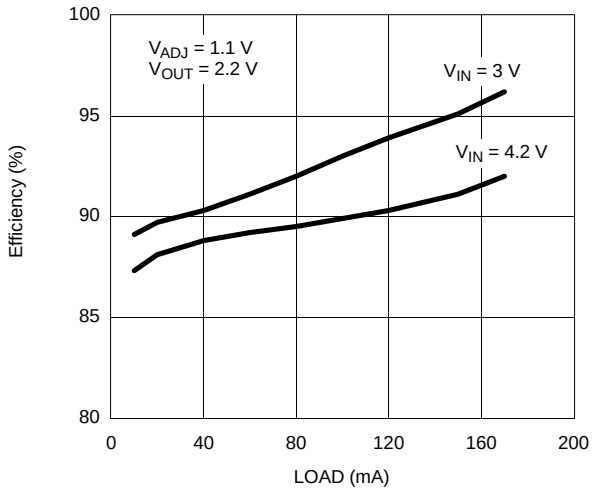
FB Threshold vs. ADJ Voltage



$r_{DS(on)}$ vs. V_{IN}



PSM Mode Efficiency vs. Load



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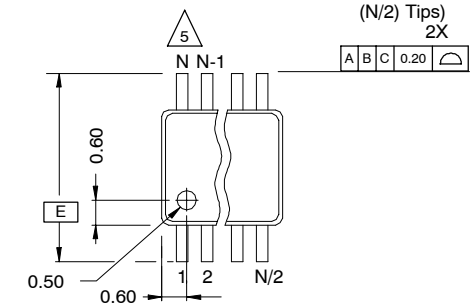
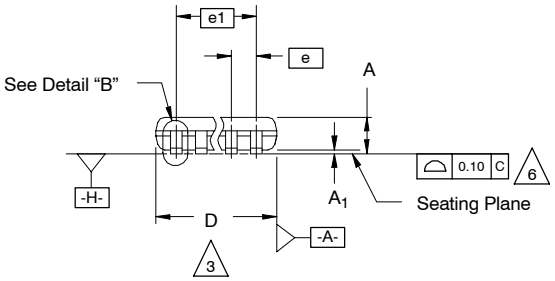
MSOP: 10-LEADS (POWER IC ONLY)

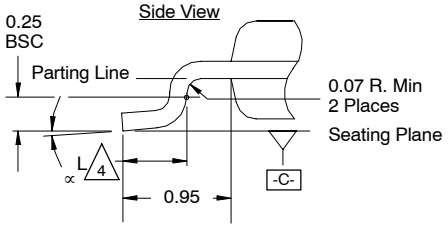
JEDEC Part Number: MO-187, (Variation AA and BA)



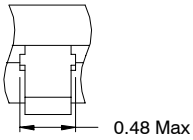
Top View



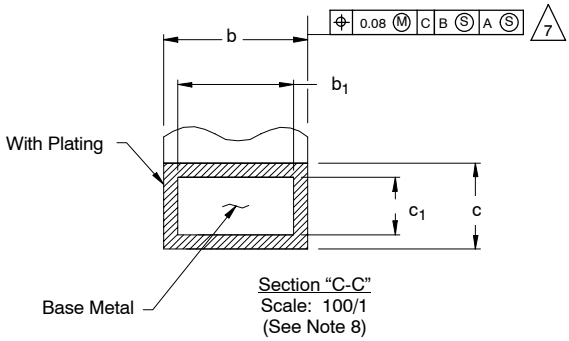
Side View



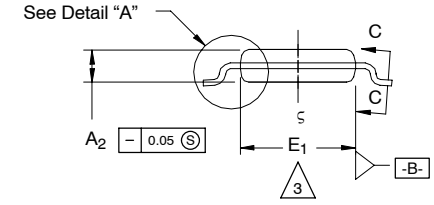
Detail "A"
(Scale: 30/1)



Detail "B"
(Scale: 30/1)
Dambar Protrusion



Section "C-C"
Scale: 100/1
(See Note 8)



End View

NOTES:

1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 10L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	–	–	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.17	–	0.27	8
b_1	0.17	0.20	0.23	8
c	0.13	–	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.50 BSC			
e_1	2.00 BSC			
L	0.40	0.55	0.70	4
N	10			5
∝	0°	4°	6°	

ECN: S-40082—Rev. A, 02-Feb-04
DWG: 5922

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