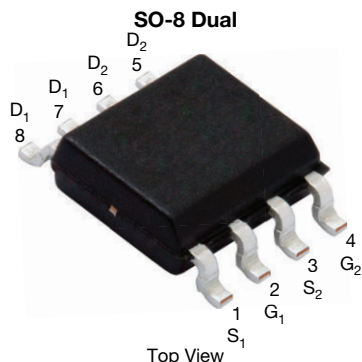
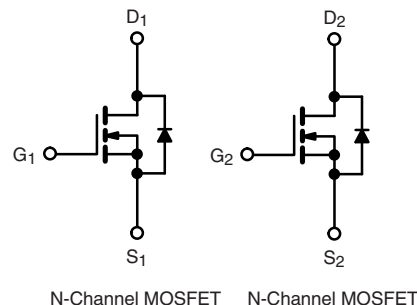


# Automotive Dual N-Channel 60 V (D-S) 175 °C MOSFET



## FEATURES

- TrenchFET® power MOSFET
- 100 %  $R_g$  and UIS tested
- AEC-Q101 qualified
- Material categorization:  
for definitions of compliance please  
see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



PRODUCT SUMMARY	
$V_{DS}$ (V)	60
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.040
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.055
$I_D$ (A) per leg	7
Configuration	Dual

ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free and halogen-free	SQ4946AEY (for detailed order number please see <a href="http://www.vishay.com/doc?79771">www.vishay.com/doc?79771</a> )

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	60	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current	$T_C = 25$ °C	$I_D$	7	A
	$T_C = 125$ °C		4	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	3.6	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	28	
Single Pulse Avalanche Current		$I_{AS}$	18	
Single Pulse Avalanche Energy		$E_{AS}$	16.2	mJ
Maximum Power Dissipation <sup>b</sup>	$T_C = 25$ °C	$P_D$	4	W
	$T_C = 125$ °C		1.3	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	110	°C/W
Junction-to-Foot (Drain)		$R_{thJF}$	34	

## Notes

- Package limited
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- When mounted on 1" square PCB (FR4 material)

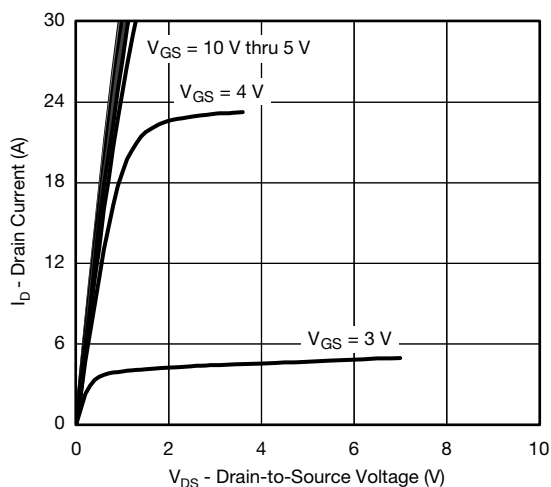
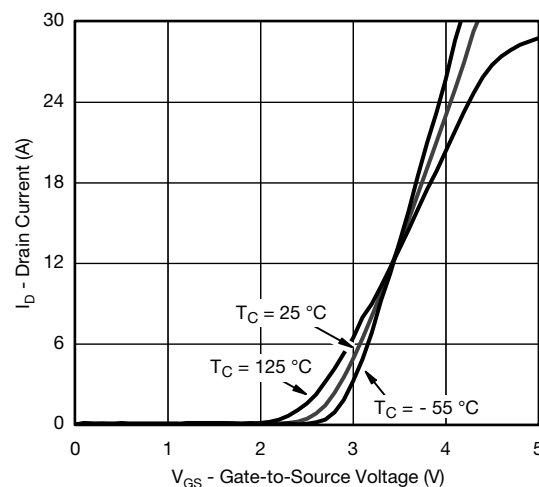
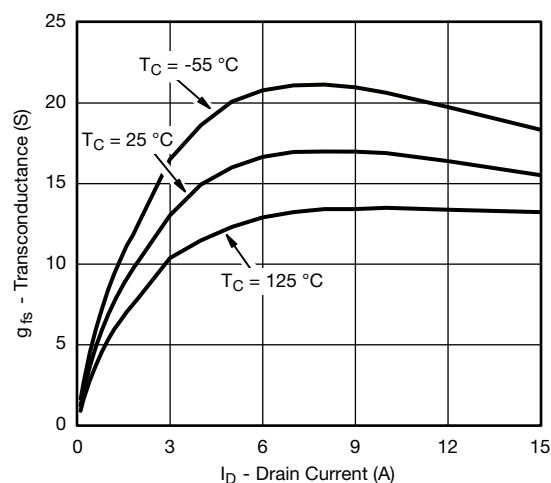
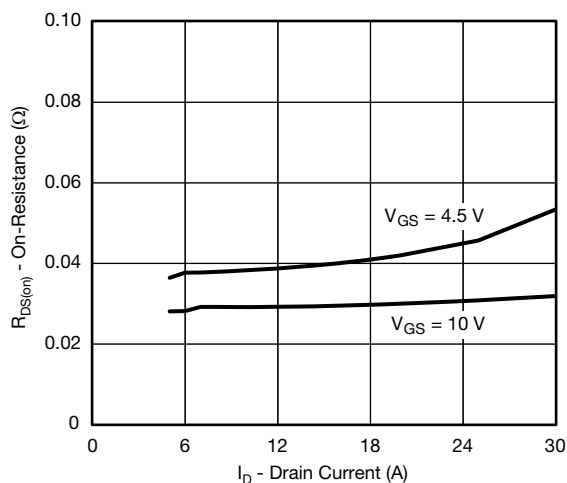
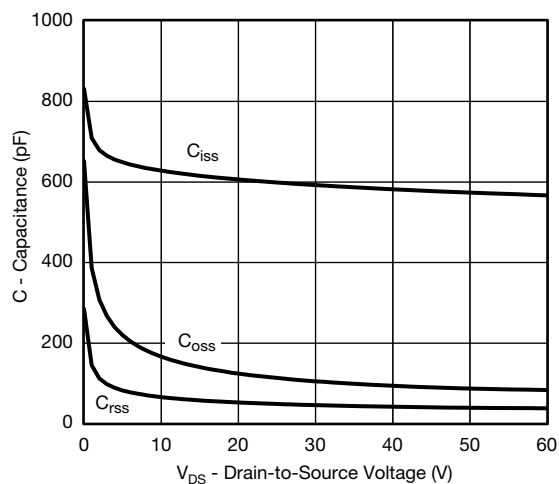
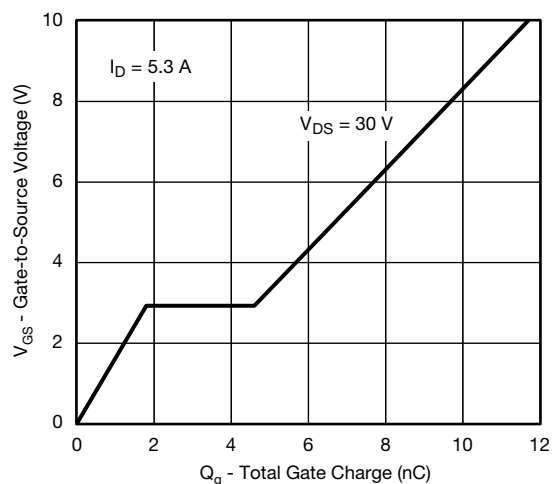


SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		60	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.5	2.0	2.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	20	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.5 A	-	0.033	0.040	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.5 A, T <sub>J</sub> = 125 °C	-	-	0.066	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.5 A, T <sub>J</sub> = 175 °C	-	-	0.081	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 4 A	-	0.045	0.055	
Forward Transconductance <sup>f</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4.5 A		-	15	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	600	750	pF
Output Capacitance	C <sub>oss</sub>			-	110	140	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	50	62	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 5.3 A	-	11.7	18	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			-	1.8	2.7	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	2.8	4.2	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.3	-	6	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 6.8 Ω I <sub>D</sub> ≡ 4.4 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	7	11	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			-	3.3	5	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	22.4	33.5	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	2.1	3.2	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	28	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 2 A, V <sub>GS</sub> = 0 V		-	0.75	1.1	V

**Notes**

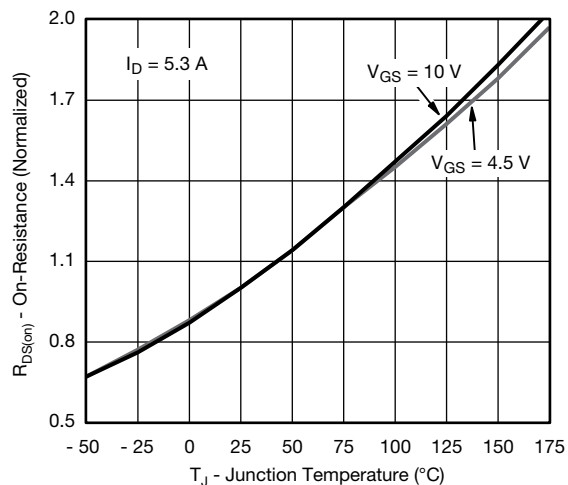
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

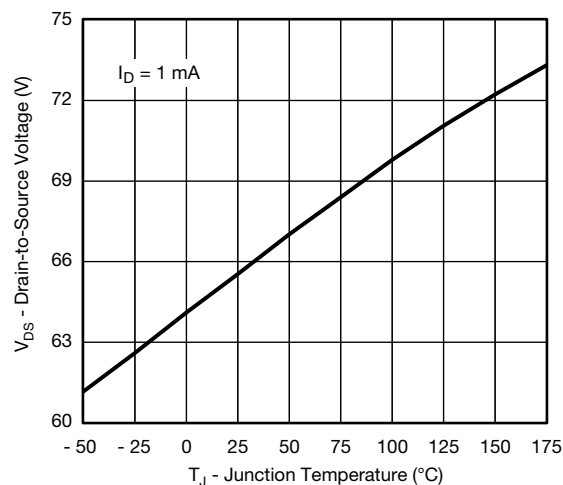
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**



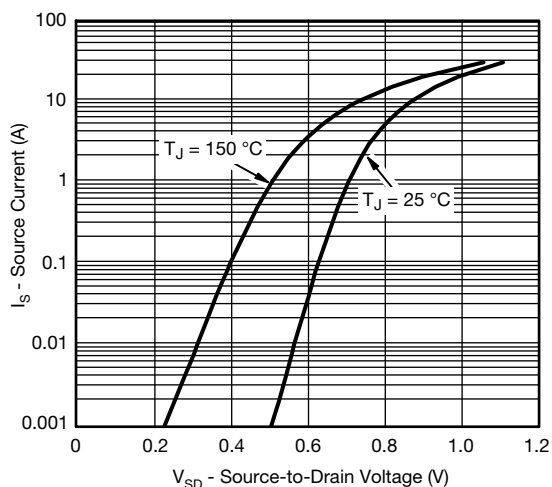
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



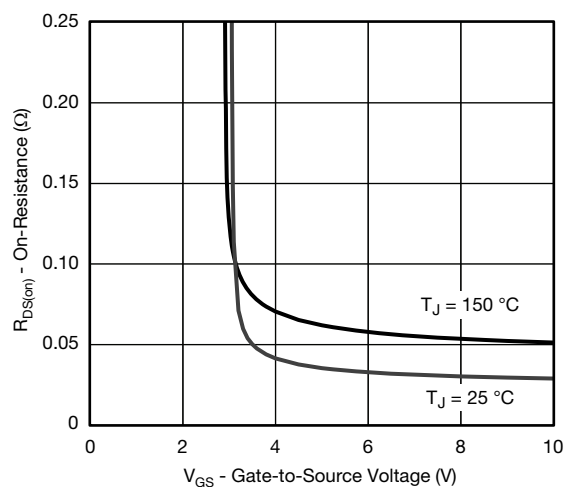
**On-Resistance vs. Junction Temperature**



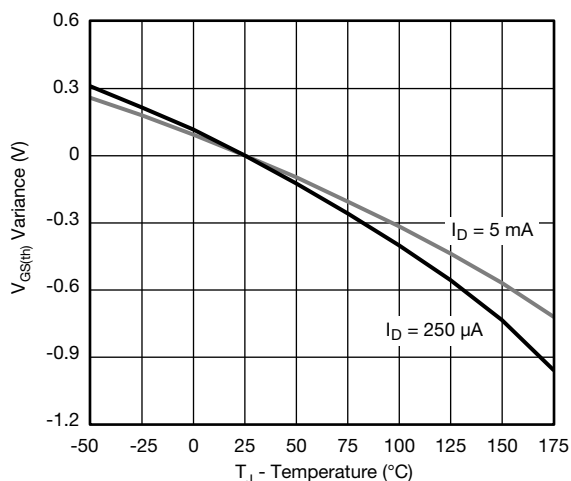
**Drain Source Breakdown vs. Junction Temperature**



**Source Drain Diode Forward Voltage**

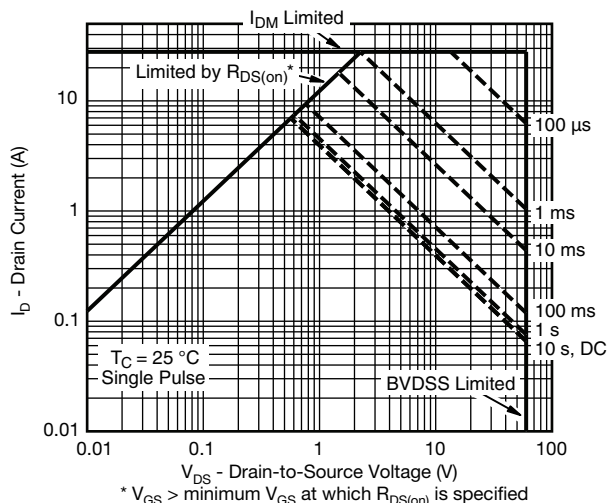


**On-Resistance vs. Gate-to-Source Voltage**

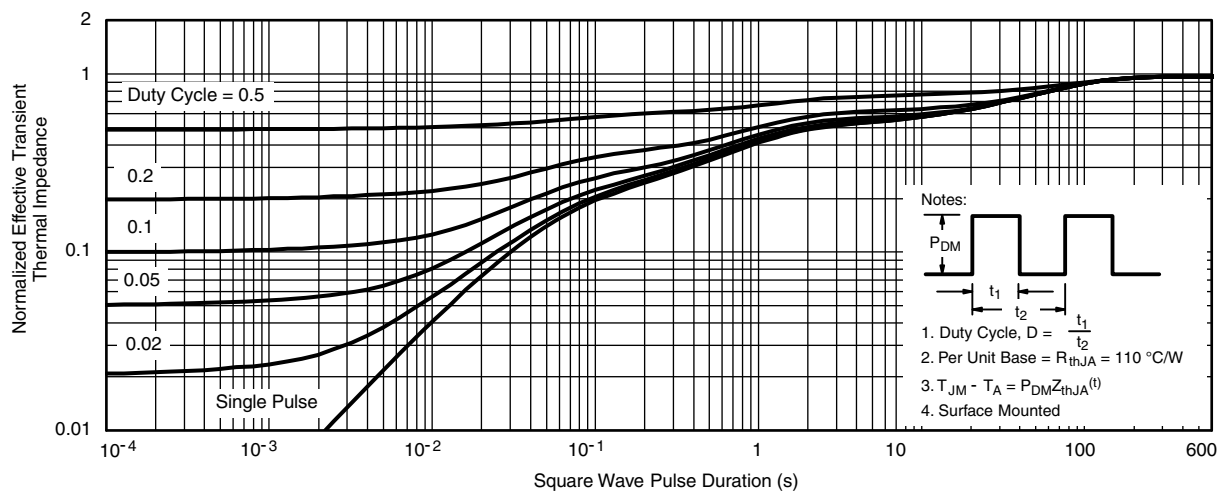


### Threshold Voltage

**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



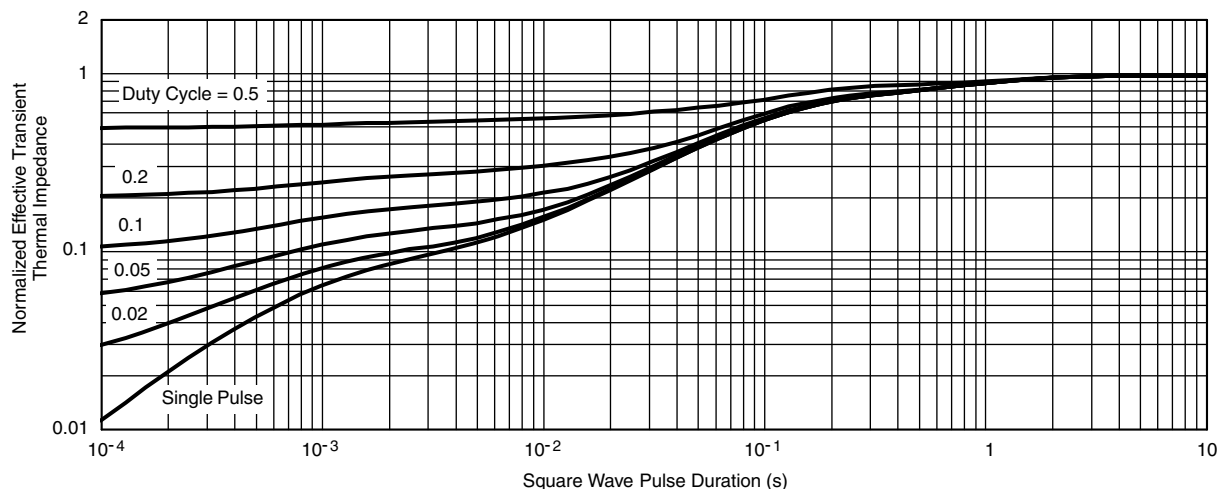
### Safe Operating Area



### Normalized Thermal Transient Impedance, Junction-to-Ambient



**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Foot**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^{\circ}\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Foot ( $25\text{ }^{\circ}\text{C}$ )are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?71506](http://www.vishay.com/ppg?71506).

## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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