

Low-Voltage Single Asymmetrical SPDT Analog Switch

DESCRIPTION

The DG2020 is a single-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed, low on-resistance and small physical size, the DG2020 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2020 is built on Vishay Siliconix's low voltage J12 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FEATURES

- Low voltage operation (2.7 V to 5.5 V)
- Low on-resistance - R_{ON}
 - NO = $0.8\ \Omega$
 - NC = $1.2\ \Omega$
- Low power consumption
- TTL/CMOS compatible
- TSOP-6 package

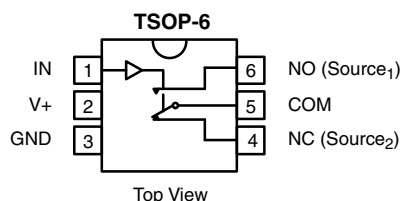
BENEFITS

- Reduced power consumption
- Simple logic interface
- High accuracy
- Reduce board space

APPLICATIONS

- Cellular phones
- Communication systems
- Portable test equipment
- Battery operated systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: E3xxx

TRUTH TABLE

LOGIC	NC	NO
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

TEMP. RANGE	PACKAGE	PART NUMBER
- 40 °C to 85 °C	TSOP-6	DG2020DV

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	CONDITIONS	LIMITS	UNIT
V+	Reference to GND	- 0.3 to 6	V
IN, COM, NC, NO ^a	Reference to GND	- 0.3 to (V+ + 0.3 V)	
Continuous Current (any terminal)	Reference to GND	± 50	mA
Peak Current (pulsed at 1 ms, 10 % duty cycle)	Reference to GND	± 200	
Storage Temperature (D suffix)	Reference to GND	- 65 to + 125	°C
TSOP-6 ^c	Power Dissipation (packages) ^b	570	mW

Notes

- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC board.
- Derate 7 mW/°C above 25 °C.



SPECIFICATION (V ₊ = 3 V)							
PARAMETER	SYMBOL	TEST CONDITION	TEMP. ^a	LIMITS (- 40 °C TO 85 °C)			UNIT
		UNLESS OTHERWISE SPECIFIED, V ₊ = 3 V, ± 10 %, V _{IN} = 0.4 V or 2 V ^e		MIN. ^b	TYP. ^c	MAX. ^b	
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0	-	V ₊	V
On-Resistance	R _{ON(NO)}	V ₊ = 2.7 V, V _{COM} = 1.5 V, I _{NO} , I _{NC} = 100 mA	Room	-	1.4	2	Ω
			Full	-	1.5	2.1	
	R _{ON(NC)}		Room	-	2.2	3.2	
			Full	-	2.3	3.3	
R _{ON} Flatness ^d	R _{ON(NO)} Flatness	V ₊ = 2.7 V, V _{COM} = 0 V to V ₊ , I _{NO} , I _{NC} = 100 mA	Room	-	0.42	-	
Switch Off Leakage Current ^f	I _{NO(off)} , I _{NC(off)}	V ₊ = 3.3 V, V _{NO} , V _{NC} = 1 V/3 V, V _{COM} = 3 V/1 V	Room	- 2.3	-	2.3	nA
			Full	- 60	-	60	
	I _{COM (off)}		Room	- 2.3	-	2.3	
			Full	- 60	-	60	
Channel-On Leakage Current ^f	I _{COM(on)}	V ₊ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 1 V/3 V	Room	- 2.3	-	2.3	
			Full	- 60	-	60	
Digital Control							
Input High Voltage	V _{INH}		Full	2	-	-	V
Input Low Voltage	V _{INL}		Full	-	-	0.4	
Input Capacitance	C _{IN}		Full	-	3.7	-	pF
Input Current	I _{NL} or I _{NH}	V _{IN} = 0 or V ₊	Full	1	-	1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON(NO)}	V _{NO} or V _{NC} = 2 V, R _L = 300 Ω, C _L = 35 pF	Room	-	6	10	μs
			Full	-	-	11	
	t _{ON(NC)}		Room	-	5	7	
			Full	-	-	8	
Turn-Off Time	t _{OFF(NO)}		Room	-	2	5	
			Full	-	-	5.5	
	t _{OFF(NC)}		Room	-	2	4	
			Full	-	-	4.5	
Break-Before-Make Time	t _d	V _{NO} or V _{NC} = 2 V, R _L = 300 Ω, C _L = 35 pF	Full	1	3	-	
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω	Room	-	1	-	pC
Off-Isolation ^d	Q _{IRR}	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room	-	- 52	-	dB
Crosstalk ^d	X _{TALK}		Room	-	- 53	-	
NO, NC Off Capacitance ^d	t _{ON(NO)}	V _{IN} = 0 or V ₊ , f = 1 MHz	Room	-	75	-	pF
	t _{ON(NC)}		Room	-	34	-	
Channel-On Capacitance ^d	t _{OFF(NO)}		Room	-	88	-	
	t _{OFF(NC)}		Room	-	95	-	
Power Supply							
Power Supply Range	V ₊		-	2.7	-	3.3	V
Power Supply Current	I ₊	V _{IN} = 0 or V ₊	Full	-	0.2	1	μA
Power Consumption	P _C		Full	-	-	3.3	μW

Notes

- a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.



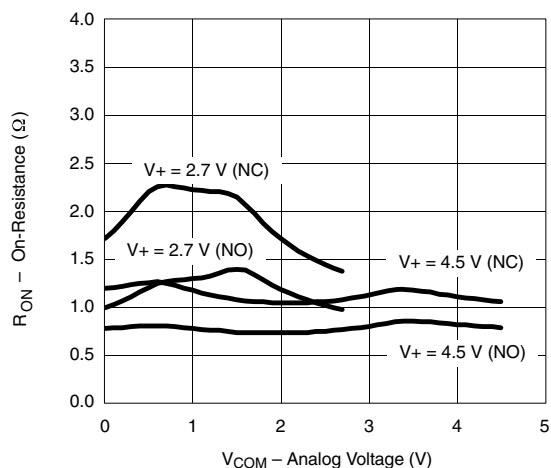
SPECIFICATION (V+ = 5 V)								
PARAMETER	SYMBOL	TEST CONDITION	TEMP. ^a	LIMITS (- 40 °C TO 85 °C)			UNIT	
		UNLESS OTHERWISE SPECIFIED, V+ = 5 V, ± 10 %, VIN = 0.8 V or 2.4 V ^e		MIN. ^b	TYP. ^c	MAX. ^b		
Analog Signal Range ^d	VNO, VNC, VCOM		Full	0	-	V+	V	
On-Resistance	RON(NO)	V+ = 4.5 V, VCOM = 3 V, INO, INC = 100 mA	Room	-	0.8	1.1	Ω	
			Full	-	0.9	1.2		
	RON(NC)		Room	-	1.2	1.6		
			Full	-	1.3	1.7		
RON Flatness ^d	RON(NO) Flatness	V+ = 4.5 V, VCOM = 0 V to V+, INO, INC = 100 mA	Room	-	0.13	-		
Switch Off Leakage Current	INO(off), INC(off)	V+ = 5.5 V, VNO, VNC = 1 V/4.5 V, VCOM = 4.5 V/1 V	Room	- 5.3	-	5.3	nA	
			Full	- 98	-	98		
	ICOM (off)		Room	- 5.3	-	5.3		
			Full	- 98	-	98		
Channel-On Leakage Current	ICOM(on)	V+ = 5.5 V, VNO, VNC = VCOM = 1 V/4.5 V	Room	- 5.3	-	5.3		
			Full	- 98	-	98		
Digital Control								
Input High Voltage	VINH		Full	2.4	-	-	V	
Input Low Voltage	VINL		Full	-	-	0.8		
Input Capacitance	CIN		Full	-	3.5	-	pF	
Input Current	INL or INH	VIN = 0 or V+	Full	1	-	1	μA	
Dynamic Characteristics								
Turn-On Time	tON(NO)	VNO or VNC = 3 V, RL = 300 Ω, CL = 35 pF	Room	-	3	6	μs	
			Full	-	-	6.5		
	tON(NC)		Room	-	2	5		
			Full	-	-	5.5		
Turn-Off Time	tOFF(NO)		Room	-	1	4		
			Full	-	-	4.5		
	tOFF(NC)		Room	-	1	3		
			Full	-	-	3.5		
Break-Before-Make Time	td	VNO or VNC = 3 V, RL = 300 Ω, CL = 35 pF	Full	0.3	1.5	-		
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω	Room	-	5	-	pC	
Off-Isolation ^d	QIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room	-	- 53	-	dB	
Crosstalk ^d	XTALK		Room	-	- 54	-		
NO, NC Off Capacitance ^d	tON(NO)	VIN = 0 or V+, f = 1 MHz	Room	-	65	-	pF	
	tON(NC)		Room	-	32	-		
Channel-On Capacitance ^d	tOFF(NO)		Room	-	90	-		
	tOFF(NC)		Room	-	95	-		
Power Supply								
Power Supply Range	V+			4.5	-	5.5	V	
Power Supply Current	I+	VIN = 0 or V+	Full	-	0.2	1	μA	
Power Consumption	PC		Full	-	-	5.5	μW	

Notes

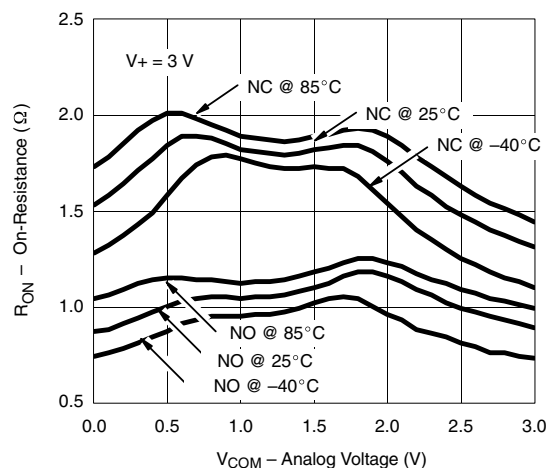
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e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested..



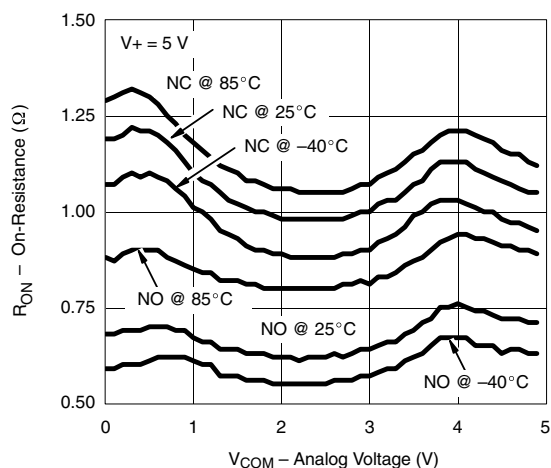
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



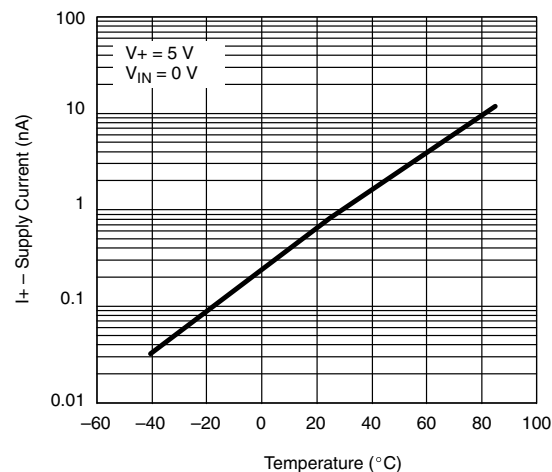
R_{ON} vs. V_{COM} and Supply Voltage



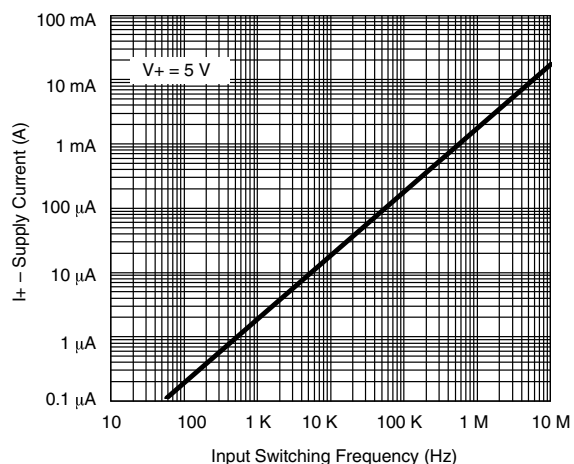
R_{ON} vs. Analog Voltage and Temperature



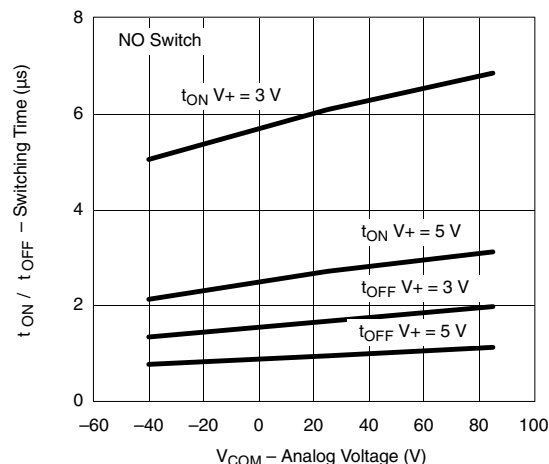
R_{ON} vs. Analog Voltage and Temperature



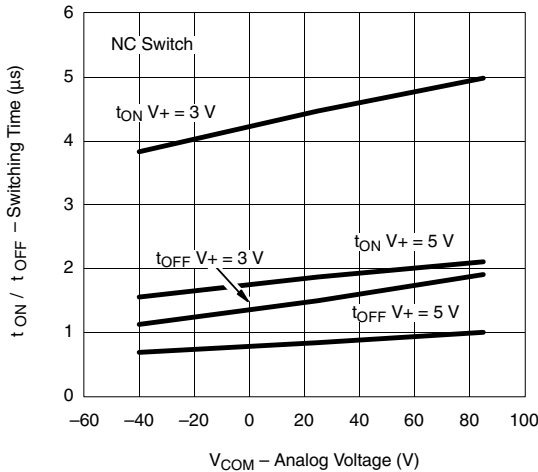
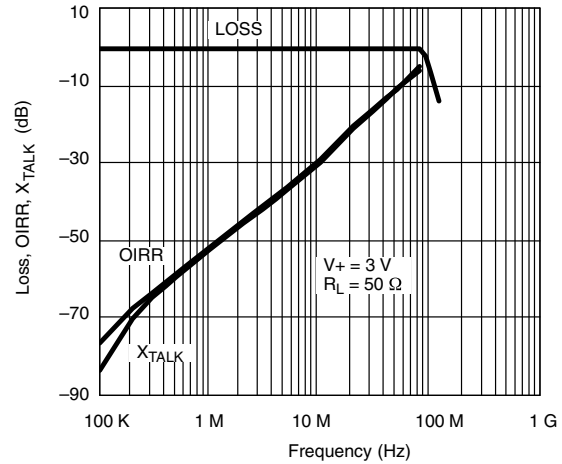
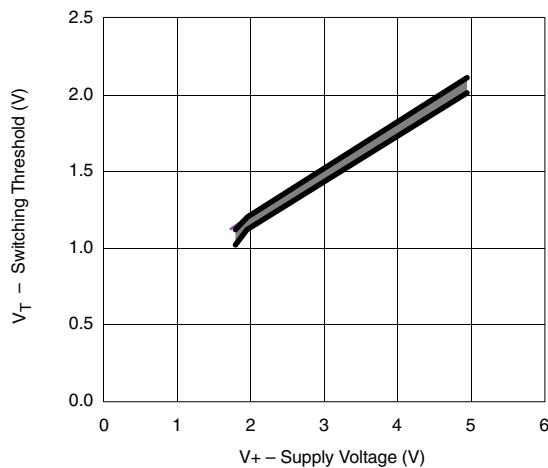
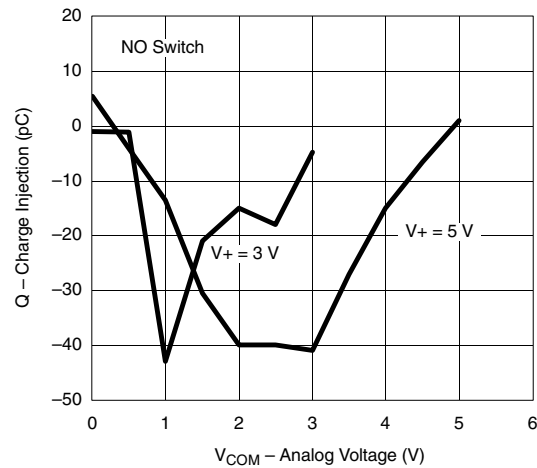
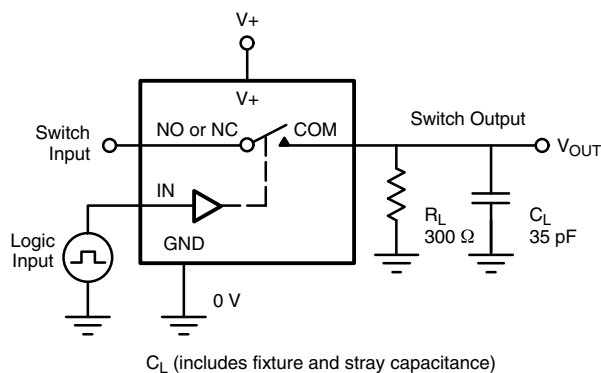
Supply Current vs. Temperature



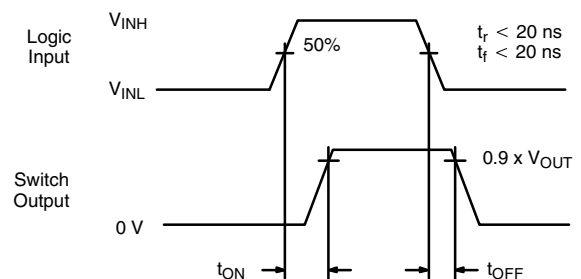
Supply Current vs. Input Switching Frequency



Switching Time vs. Temperature and Supply Voltage

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Switching Time vs. Temperature and Supply Voltage

Insertion Loss, Off-Isolation Crosstalk vs. Frequency

Switching Threshold vs. Supply Voltage

Charge Injection vs. Analog Voltage
TEST CIRCUITS

 C_L (includes fixture and stray capacitance)

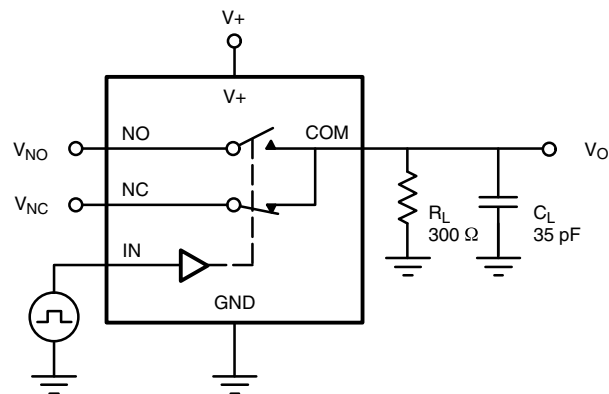
$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

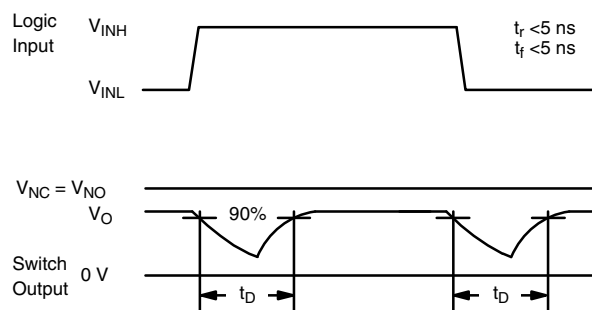
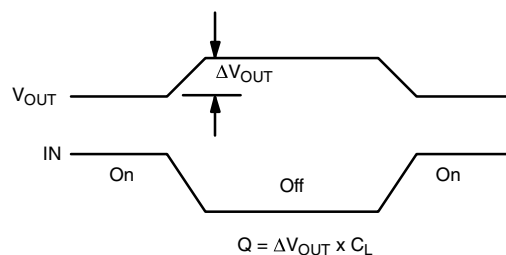
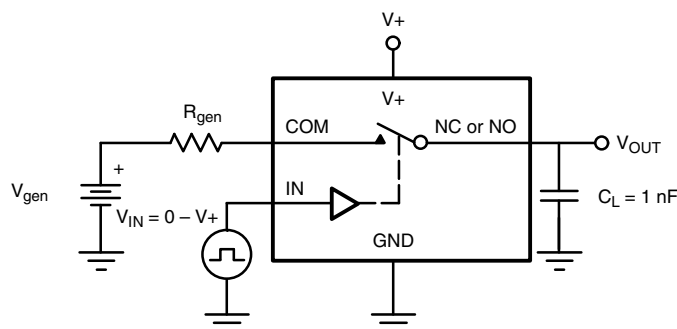


Fig. 2 - Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 3 - Charge Injection

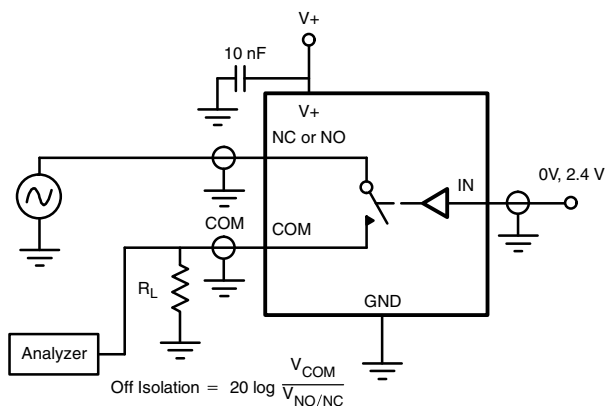


Fig. 4 - Off-Isolation

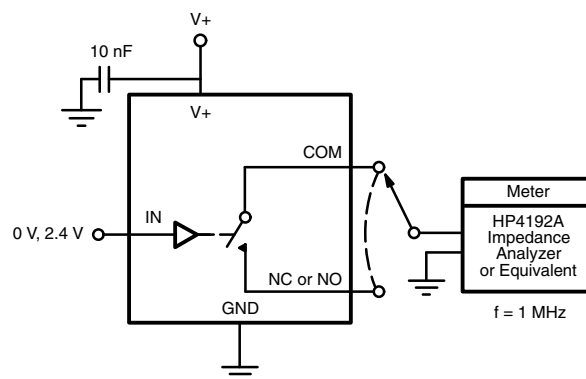


Fig. 5 - Channel off/on Capacitance

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TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C



5-LEAD TSOP



6-LEAD TSOP



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

Recommended Land Pattern For TSOP-5L / TSOP-6L



TSOP 5L



TSOP 6L


Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022
DWG: 3010



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