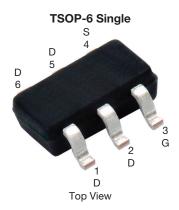




N-Channel 150 V (D-S) MOSFET



PRODUCT SUMMARY						
V _{DS} (V)	150					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.375					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 6 \text{ V}$	0.400					
Q _g typ. (nC)	5.4					
I _D (A)	1.5					
Configuration	Single					

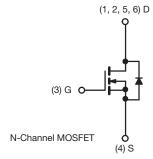
FEATURES

- TrenchFET® power MOSFET
- PWM optimized for fast switching in small footprint
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

• Primary side switch for low power DC/DC converters



ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free	Si3440DV-T1-E3
Lead (Pb)-free and halogen-free	Si3440DV-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage	V _{DS}	150	V		
Gate-source voltage	V_{GS}	V _{GS} ± 20			
Continuous drain current (T, I = 175 °C) a	T _A = 25 °C	I _D	1.2	A	
Continuous drain current (1 _J = 175 °C) ^a	T _A = 85 °C		0.8		
Pulsed drain current		I _{DM}	6	A	
Single avalanche current	L = 0.1 mH	I _{AS}	4		
Single avalanche energy (duty cycle ≤ 1 %)	L=U.IIIII	E _{AS}	0.8	mJ	
Continuous source current (diode conduction) a	I _S	1	Α		
Maximum power dissipation ^a	T _A = 25 °C	D.	1.14	W	
Maximum power dissipation "	T _A = 85 °C	P _D	0.59		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^a	t ≤ 5 s	R_{thJA}	45	62.5		
	Steady state		90	110	°C/W	
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	25	30		

Notes

a. Surface mounted on 1" x 1" FR4 board



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	OL TEST CONDITIONS		TYP.	MAX.	UNIT	
Static							
Gate threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	2	-	4	V	
Gate-body leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
Zero gate voltage drain current	la a a	$V_{DS} = 150 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μА	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 150 V, V _{GS} = 0 V, T _J = 85 °C	-	-	5		
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	4	-	-	Α	
Drain-source on-state resistance ^a	В	V _{GS} = 10 V, I _D = 1.5 A	-	0.310	0.375	0	
Drain-Source on-State resistance "	R _{DS(on)}	V _{GS} = 6 V, I _D = 1.4 A - 0.330			0.400	Ω	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 1.5 A	-	4.1	-	S	
Diode forward voltage ^a	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	-	0.8	1.2	V	
Dynamic ^b							
Total gate charge	Qg		-	5.4	8		
Gate-source charge	Q _{gs}	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 1.5 \text{ A}$	-	1.1	-	nC	
Gate-drain charge	Q _{gd}		-	1.9	-		
Gate resistance	R_g	f = 1 MHz	4	9	15	Ω	
Turn-on delay time	t _{d(on)}		-	8	15		
Rise time	t _r	$V_{DD} = 75 \text{ V}, \ R_L = 75 \ \Omega$ $I_D \cong 1 \text{ A}, \ V_{GEN} = 10 \text{ V}, \ R_g = 6 \ \Omega$	-	10	15		
Turn-off delay time	t _{d(off)}		-	20	30	ns	
Fall time	t _f		-	15	25		
Source-drain reverse recovery time	t _{rr}	I _F = 1.7 A, dI/dt = 100 A/μs	-	40	60]	

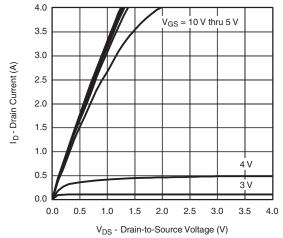
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

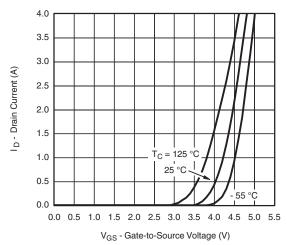
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



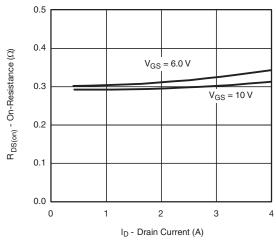
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



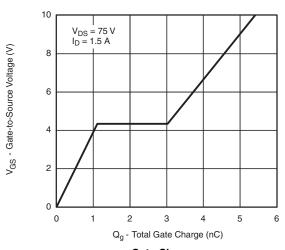




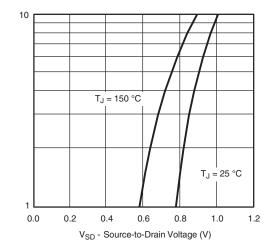
Transfer Characteristics



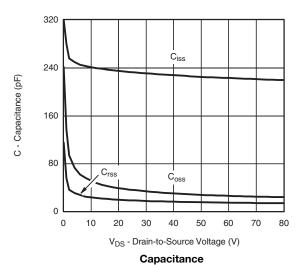
On-Resistance vs. Drain Current



Gate Charge



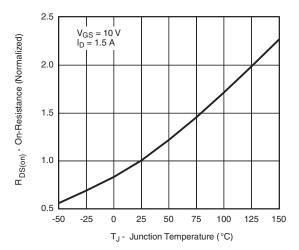
Source-Drain Diode Forward Voltage



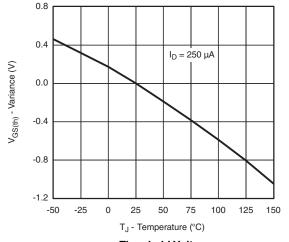
Is - Source Current (A)



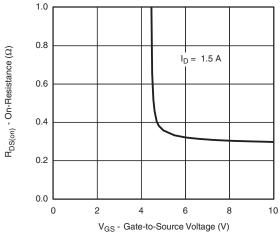
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



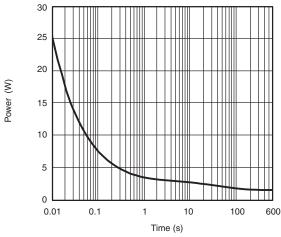
On-Resistance vs. Junction Temperature



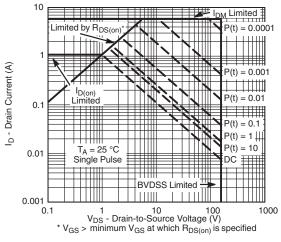
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



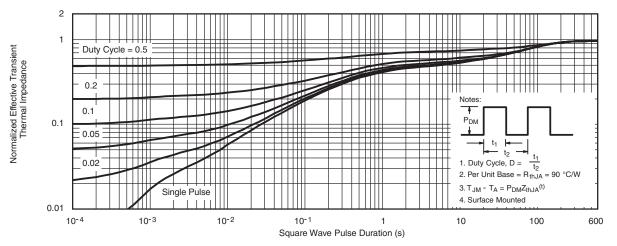
Single Pulse Power



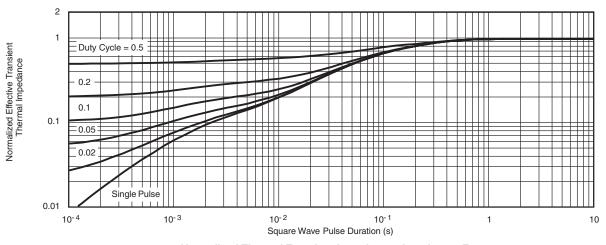
Safe Operating Area



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

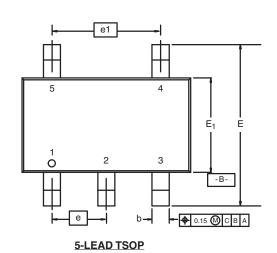
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg272380.

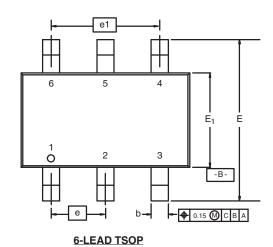


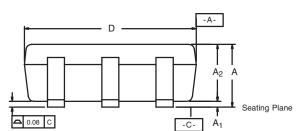


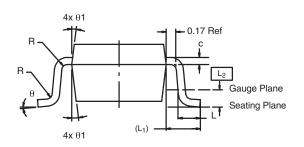
TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C









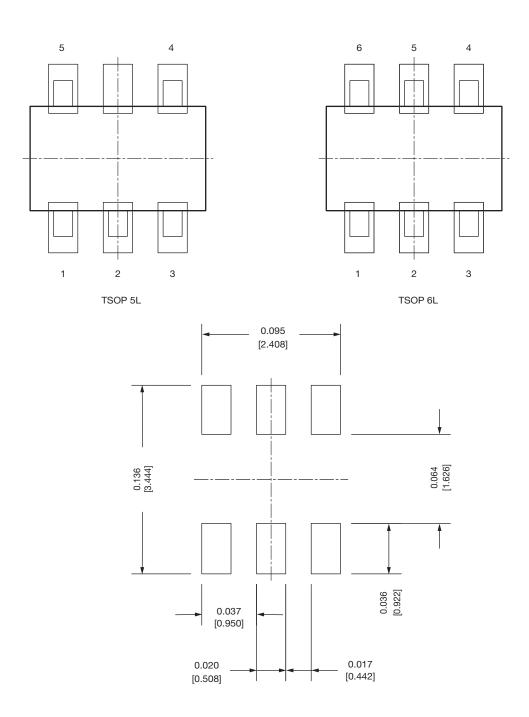
	MILLIMETERS			ı	NCHES	
Dim	Min	Nom	Max	Min	Nom	Max
Α	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
С	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
Е	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
е		0.95 BSC		0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁		0.60 Ref			0.024 Ref	
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ_1	7° Nom				7° Nom	
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540						

Document Number: 71200 18-Dec-06

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Recommended Land Pattern For TSOP-5L / TSOP-6L



Note

• All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022 DWG: 3010



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