Dual Output Power Switch

FEATURES

- Two Output Power Switches
- Total Output Drive — 200 mA Continuous
- 9-V to 35-V Supply Voltage Range
- Low Side or High Side Switch Configuration
- Internal Output Over Voltage Clamp For Driving Inductive Loads
- Current Limit Protection
- Thermal Shutdown Protection
- UVLO With User Programmable Time Delay

Pb-free Available

APPLICATIONS

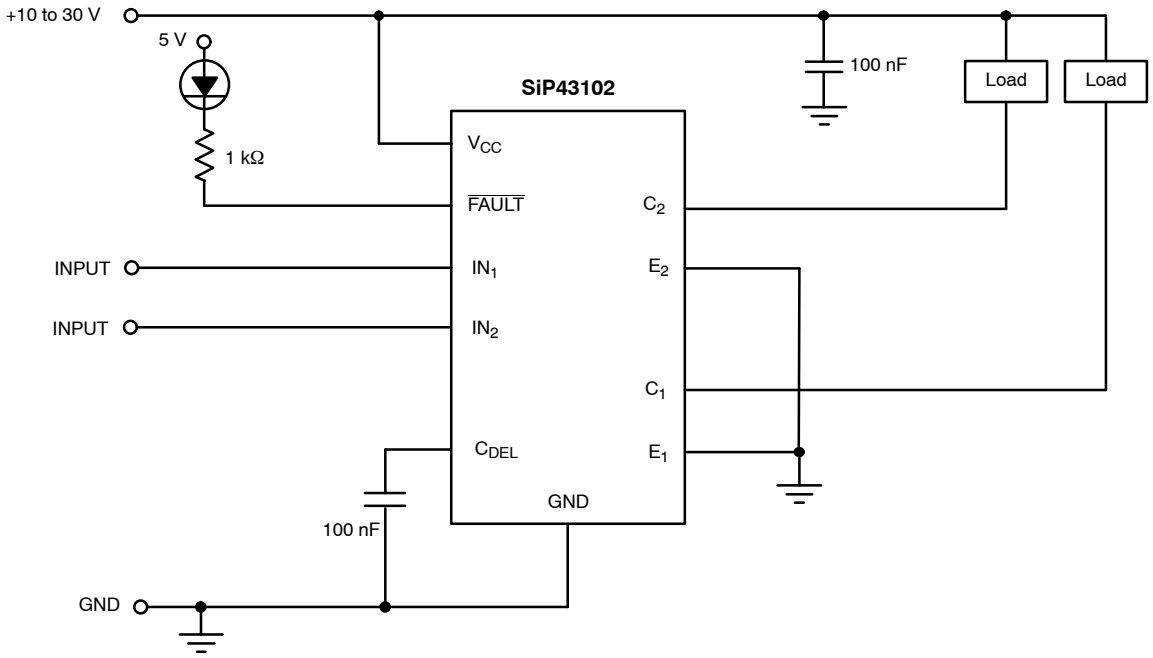
- Optical Detectors for Factory Automation

DESCRIPTION

SiP43102 is a dual power switch IC which contains all control and power switching circuitry required to drive resistive and inductive loads in industrial applications. The output switches are NPN power transistors which can be configured as either high-side or low-side switches. These switches can operate from voltages as high as 35 V and have a continuous output current rating of 200 mA, combined or individually. Internal zener diodes are provided to clamp the power switch voltages to safe levels when driving inductive loads. The IN_1 and IN_2 pins are non-inverting inputs which control the output of switch 1 and switch 2 respectively. SiP43102 contains under voltage lockout, UVLO, a user definable turn on delay, current limit, short circuit protection, and thermal shutdown.

The SiP43102 is available in 16-pin TSSOP and PowerPAK® MLP-44 packages, which are specified over the industrial, D suffix (–40 to 85°C) temperature range. Both standard and lead (Pb)-free options are available in the 16-pin TSSOP package.

TYPICAL APPLICATION CIRCUIT



Both Switches Configured as Low-Side

ABSOLUTE MAXIMUM RATINGS

V_{CC} . . . . . 35 V
C1, E1, C2, E2 . . . . . 35 V
C1-E1, C2-E2 (clamped by internal circuitry) . . . . . 52 V
Output Current
Continuous for one Output . . . . . 200 mA
Peak for one Output . . . . . 1.3 A
$\overline{FAULT}$ Output Current . . . . . 10 mA
$\overline{FAULT}$ Output Voltage . . . . . −0.3 V t0 V_{CC} + 0.3 V
IN_1, IN_{2A}, IN_{2B} . . . . . −0.3 V t0 V_{CC} + 0.3 V
Storage Temperature . . . . . −65 to 150°C
Operating Junction Temperature . . . . . 125°C

Power Dissipation
TSSOP-16[a] @ 85°C . . . . . 440 mW
PowerPAK MLP44-16[b] @ 85°C . . . . . 850 mW
Thermal Impedance (Θ_{JA})
TSSOP-16[c] . . . . . 90°C/W
PowerPAK MLP44-16[d] . . . . . 47°C/W

Notes
a. Derate 11.1 mW/°C
b. Derate 21.3 mW/°C
c. Device mounted on JEDEC compliant two layer test board.
d. Device mounted on JEDEC compliant four layer test board.

Currents are positive into, negative out of the specificed terminal.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

V_{CC} . . . . . 9 to 32 V
Operating Temperature Range . . . . . −40 to 85°C

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified V_{CC} = 25 V,IN1, IN2 = 0 V, IN1, IN2, INV2 = 5 V C_{DEL} = 10 nF, $T_A = T_J$		Limits Min[a]	Typ[b]	Max[a]	Unit
Power Supply							
Supply Voltage	V_{CC}			9		32	V
Supply Current	I_{CC}	−40 to 85°C, Both Inputs Enabled			6	9	mA
Logic Inputs (IN_1, IN_2)							
Digital Input High Level	V_{IH}			3.5			V
Digital Input Low Level	V_{IL}					1.5	
Input Bias Current, Low Level	I_{IL}	IN_1, IN_{2A}, IN_{2B} = 0 V			−0.40		µA
Input Bias Current, High Level	I_{IH}	IN_1, IN_{2A}, IN_{2B} = 5 V			0.02		
Switches 1&2 – High Side Configuration							
Rise Time (Off to On)	t_r	R_{LOAD} = 250 Ω to GND, C_1 , C_2 = 25 V			300		ns
Rise Tiem (On to Off)	t_f				300		
Saturation Voltage	V_{SATHS}	R_{LOAD} = 125 Ω to GND	T_A = 25 °C			1.3	V
			T_A = −40 °C			1.5	
Current Limit	I_{LIMHS}	R_{LOAD} = 0.25 Ω to GND, T_A = 25 °C			1.1		A
Leakage Current	I_{LHS}	E_1, E_2 = GND, C_1 , C_2 = 25 V,IN_1, IN_{2A}, IN_{2B} = 0 V				5	µA
Voltabe Clamp	V_{CLHS}	Measure ($V_{C1} - V_{E1}$) or ($V_{C2} - V_{E2}$)			52		V
Switches 1&2 – Low Side Configuration							
Rise Time (On to Off)	t_r	R_{LOAD} = 250 Ω to V_{CC}, L_{OAD} = 25 V to C_1 , C_2			400		ns
Rise Tiem (Off to On)	t_f				350		
Saturation Voltage	V_{SATLS}	R_{LOAD} = 125 Ω to V_{CC}	T_A = 25 °C			1.3	V
			T_A = −40 °C			1.5	
Current Limit	I_{LIMLS}	R_{LOAD} = 0.25 Ω to V_{CC}, T_A = 25 °C			1.1		A
Leakage Current	I_{LLS}	E_1, E_2 = GND, C_1 , C_2 = 25 V,IN_1, IN_{2A}, IN_{2B} = 0 V				5	µA
Voltabe Clamp	V_{CLLS}	Measure ($V_{C1} - V_{E1}$) or ($V_{C2} - V_{E2}$)			52		V

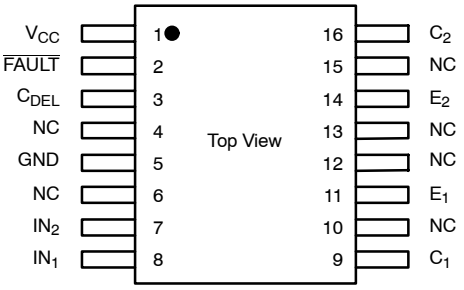
SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified V_{CC} = 25 V,IN1, IN2 = 0 V, IN1, IN2, INV2 = 5 V C_{DEL} = 10 nF, $T_A = T_J$	Limits Min[a]	Limits Typ[b]	Limits Max[a]	Unit
Turn-On Delay						
C_{DEL} Maximum Voltage	V_{DEL}			4.7		V
C_{DEL} Threshold	V_{DELTH}			4		
I_{CDEL}	I_{CDEL}			2.5		µA
$\overline{FAULT}$ Output						
V_{CESAT} Conducting State (On)	V_{SDON}	Load on $\overline{FAULT}$ ≤ 10 mA		0.4		V
Operating Frequency						
Switching Frequency	f_{SW}				25	kHz
Under Voltage Lockout						
UVLO Threshold	V_{UVLO}		7.5	8	8.5	V
UVLO Hysteresis	V_{HYS}		0.4	0.5	0.6	
Thermal Shutdown						
Thermal Shutdown Threshold	T			160		°C
Hysteresis	T_{HYS}			20		

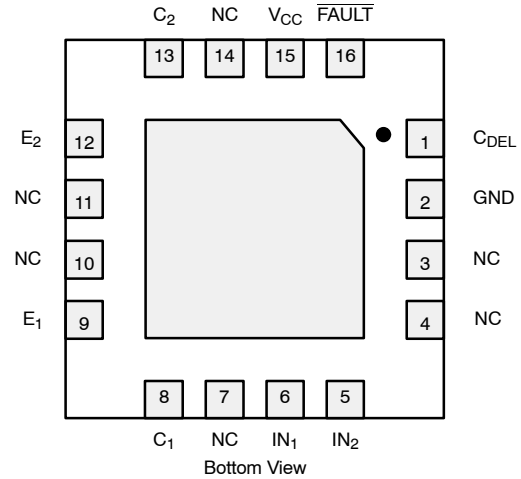
Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (−40° to 85°C).
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at V_{CC} = 12 V unless otherwise noted.

PIN CONFIGURATION

TSSOP-16



PowerPAK MLP-44



TSSOP-16 ORDERING INFORMATION

Standard-Part Number	Lead (Pb)-Free Part Number	Temperature Range	Marking
SiP43102DQ-T1	SiP43102DQ-T1—E3	−40 to 85°C	43102

PowerPAK MLP-44 ORDERING INFORMATION

Standard Part Number	Temperature Range	Marking
SiP43102DLP-T1	−40 to 85°C	43102

PIN DESCRIPTION			
Pin Number		Name	Function
TSSOP–16	MLP44–16		
1	15	V_{CC}	Positive Supply Voltage
2	16	$\overline{FAULT}$	Open collector output that is switched low on in the event of Short Circuit or Thermal Shut Down.
3	1	C_{DEL}	Connection for the external capacitor controlling the turn on delay.
4, 6, 10, 12, 13, 15	3, 4, 7, 10, 11, 14	NC	No connection
5	2	GND	Ground Pin.
7	5	IN_2	Input to the Exclusive OR controlling power switch 2.
8	6	IN_1	Input controlling power switch 1.
9	8	C_1	Collector of power switch 1.
11	9	E_1	Emitter of power switch 1.
14	12	E_2	Emitter of power switch 2.
16	13	C_2	Collector of power switch 2.

DETAILED PIN DESCRIPTION

C_{DEL}

A capacitor connected to this pin is used to set the duration the turn on delay. The delay starts after the UVLO threshold has been reached.

IN_1

This pin controls the state of the output NPN switch 1. A Logic 0 holds the switch off while a Logic 1 turns the switch on.

IN_2

This pin controls the state of the output NPN switch 2. A Logic 0 holds the switch off while a Logic 1 turns the switch on.

E_1

This pin is the emitter of switch 1. This pin is connected to the load in the High-Side switch configuration, and is connected to Ground in the Low-Side configuration.

E_2

This pin is the emitter of switch 2. This pin is connected to the load in the High-Side switch configuration, and is connected to Ground in the Low-Side configuration.

C_1

This pin is the collector of switch 1. This pin is connected to the V_{CC} in the High-Side switch configuration, and is connected to the load in the Low-Side configuration.

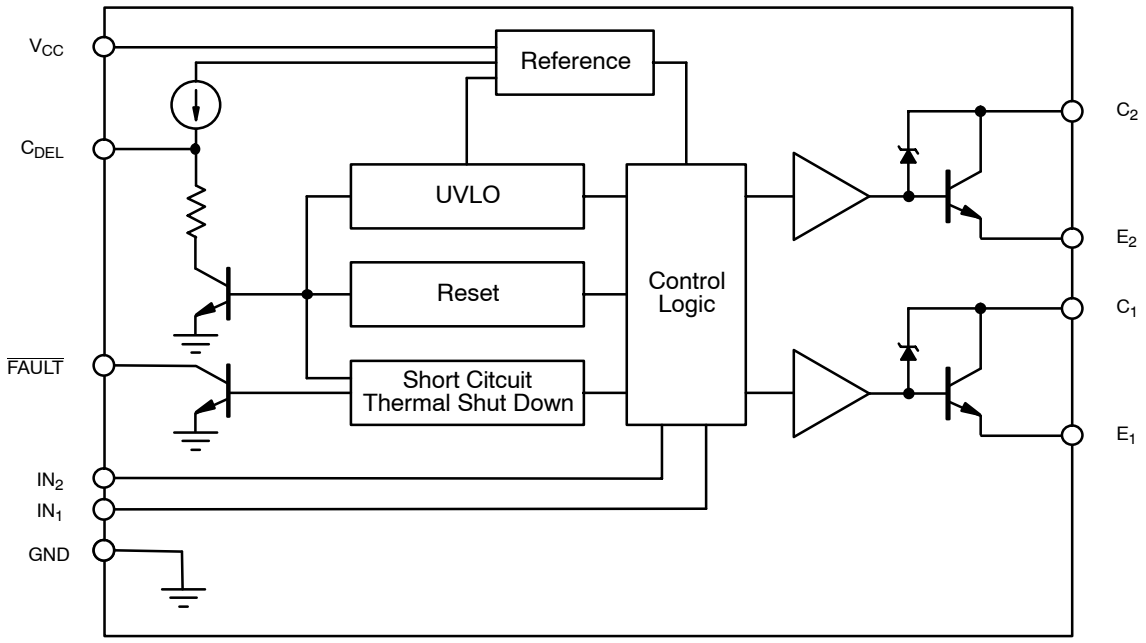
C_2

This pin is the collector of switch 2. This pin is connected to the V_{CC} in the High-Side switch configuration, and is connected to the load in the Low-Side configuration.

$\overline{FAULT}$

This pin is an open collector output that is pulled to Ground in the event of a short circuit, an overcurrent, or a thermal shut down.

FUNCTIONAL BLOCK DIAGRAM



DETAILED OPERATION

Turn On Delay

The turn on delay prohibits the output switches from being turned on for a period of time after V_{CC} has passed through 8 V and the undervoltage condition no longer exists. The UVLO function keeps the external C_{DEL} capacitor discharged until V_{CC} is greater than 8 V. After that occurs, internal 2.5-μA current source charges the capacitor from GND to 4.7 V. A comparator detects when the voltage on C_{DEL} passes through 4 V and enables the output switches. The delay time is a function of the capacitor value and is defined as 1.6 ms/nF.

An external switch can be connected across the capacitor to disable the output switches and reset the time delay.

Short Circuit and Overcurrent indication

When an overcurrent or short circuit condition occurs on either switch, the SiP43102enters a hiccup current limiting mode. In this mode, the capacitor on C_{DEL} is discharged down to 3 V, thus turning off the output switches, and then is charged up to 4 V by a 2.5-μA internal current source, thus turning the switches on again. If the overcurrent or short circuit condition remains this cycle will continue. The switches are enabled at a very low duty cycle, minimizing the power dissipation and protecting the switches from damage.

The FAULT output will switch to GND, indicating that an overload condition or short circuit condition exists.

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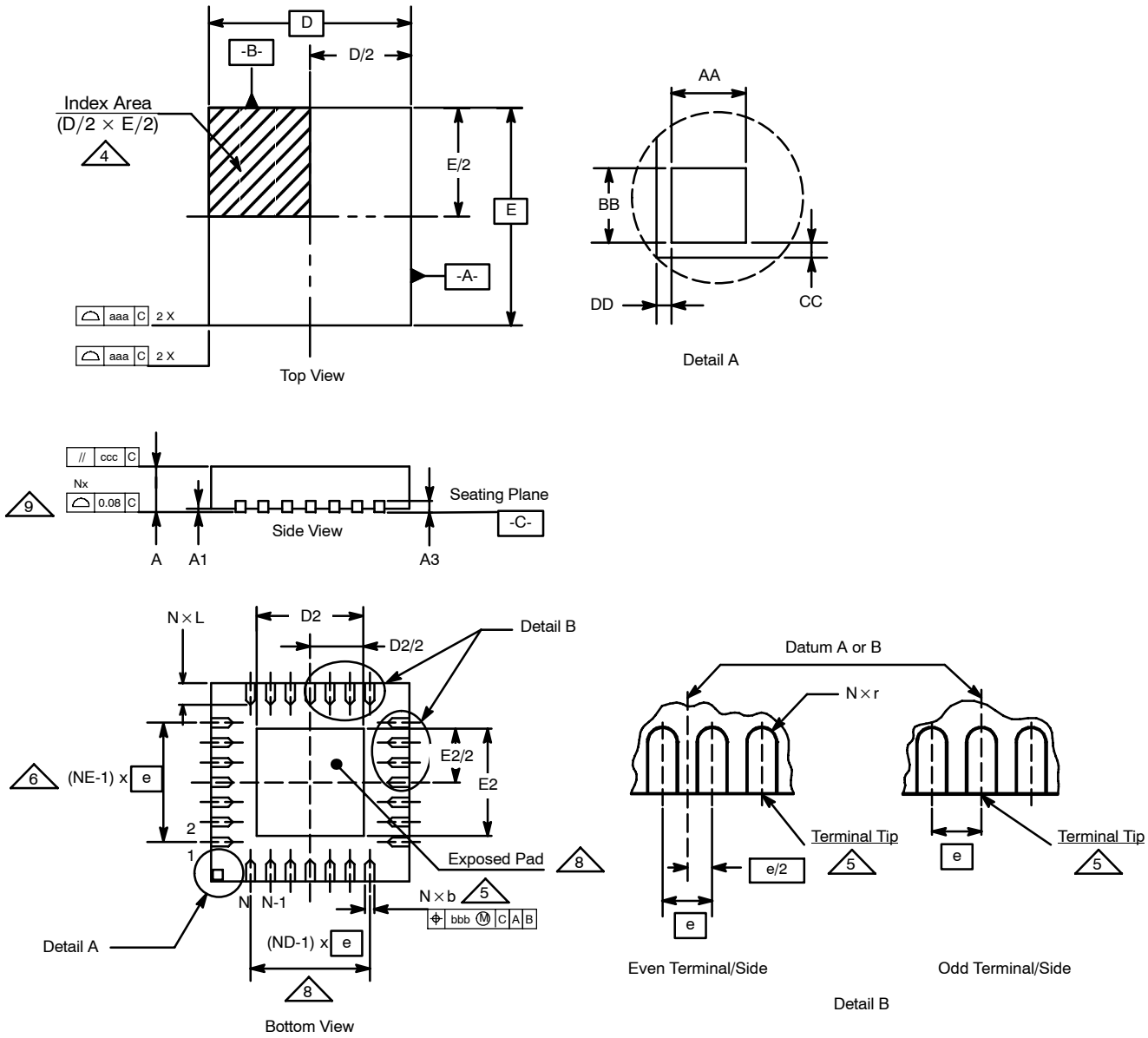
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PowerPAK® MLP44-16 (POWER IC ONLY)

JEDEC Part Number: MO-220



PowerPAK® MLP44-16 (Power IC Only)

JEDEC Part Number: MO-220

Dim	MILLIMETERS*			INCHES			Notes
	Min	Nom	Max	Min	Nom	Max	
A	0.80	0.90	1.00	0.0315	0.0354	0.0394	
A1	0	0.02	0.05	0	0.0008	0.0020	
A3	–	0.20 Ref	–	–	0.0079	–	
AA	–	0.345	–	–	0.0136	–	
aaa	–	0.15	–	–	0.0059	–	
BB	–	0.345	–	–	0.0136	–	
b	0.25	0.30	0.35	0.0098	0.0118	0.138	5
bbb	–	0.10	–	–	0.0039	–	
CC	–	0.18	–	–	0.0071	–	
ccc	–	0.10	–	–	0.0039	–	
D		4.00 BSC			0.1575 BSC		
D2	2.55	2.7	2.8	0.1004	0.1063	0.1102	
DD	–	0.18	–	–	0.0071	–	
E		4.00 BSC			0.1575 BSC		
E2	2.55	2.7	2.8	0.1004	0.1063	0.1102	
e		0.65 BSC			0.0256 BSC		
L	0.3	0.4	0.5	0.0118	0.0157	0.0197	
N		16			16		3, 7
ND	–	4	–	–	4	–	6
NE	–	4	–	–	4	–	6
r	b(min)/2	–	–	b(min)/2	–	–	

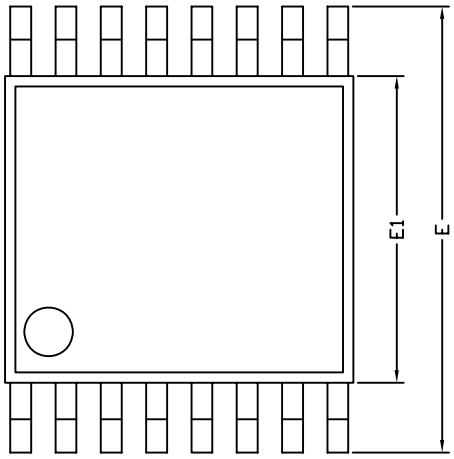
* Use millimeters as the primary measurement.

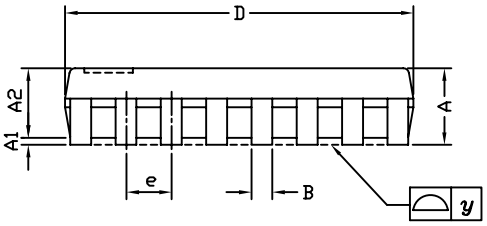
ECN: S-50794—Rev. B, 16-May-05
DWG: 5905

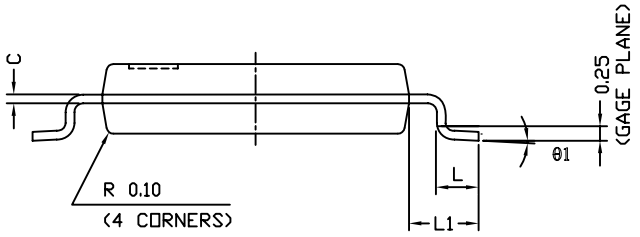
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angels are in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a molded or marked feature. The X and Y dimension will vary according to lead counts.
5. Dimension b applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip.
6. ND and NE refer to the number of terminals on the D and E side respectively.
7. Depopulation is possible in a symmetrical fashion.
8. Variation HHD is shown for illustration only.
9. Coplanarity applies to the exposed heat sink slug as well as the terminals.

TSSOP: 16-LEAD

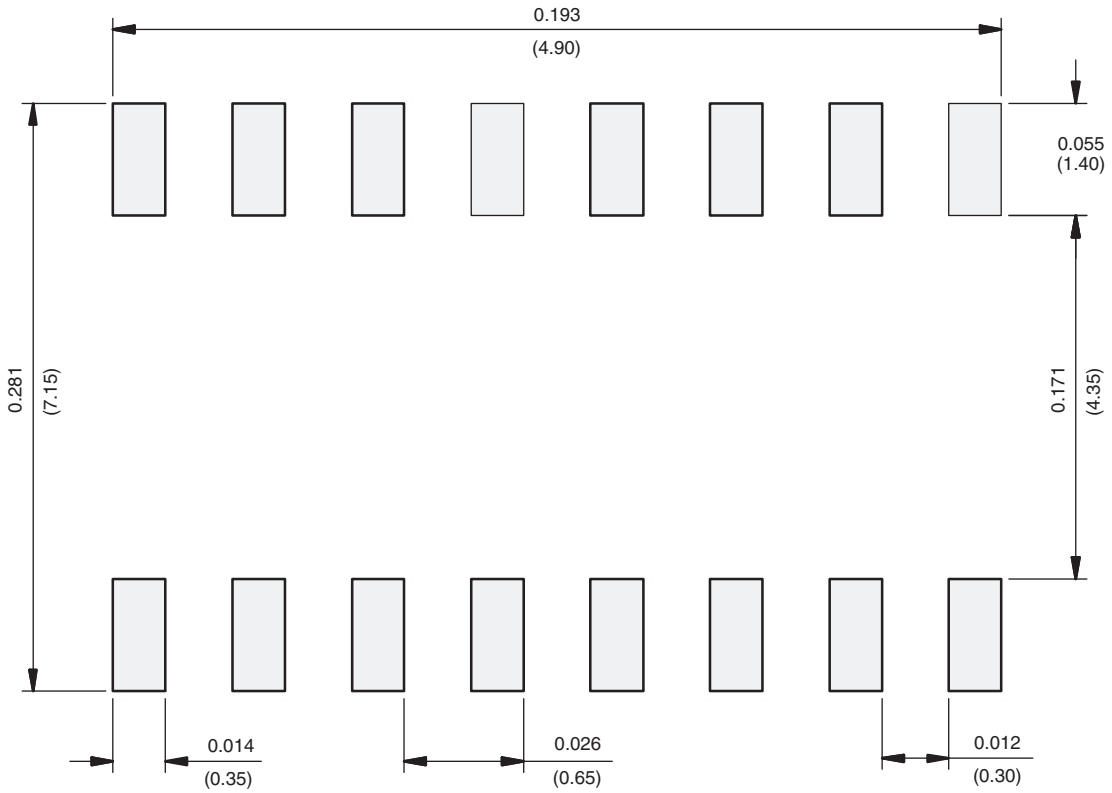






Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

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