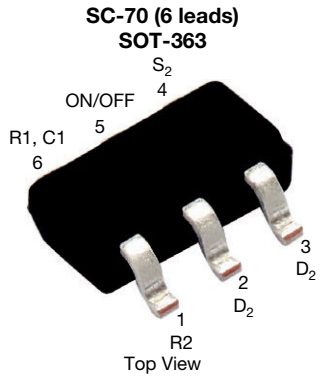
Load Switch with Level-Shift



Marking code: VC

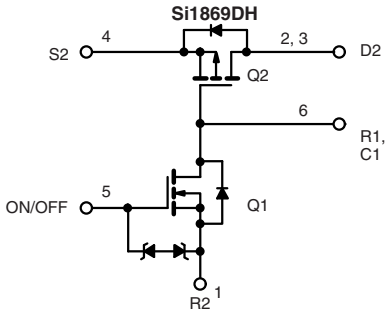
FEATURES

- TrenchFET® power MOSFETs: 1.8 V rated
- ESD protected: 2000 V on input switch, $V_{ON/OFF}$
- 165 mΩ low $R_{DS(on)}$
- 1.8 V to 20 V input
- 1.5 V to 8 V logic level control
- Low profile, small footprint SC-70-6 package
- Adjustable slew-rate
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- Level-shift for portable devices



PRODUCT SUMMARY	
V_{D2S2} (V)	-20
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.165
$R_{DS(on)}$ max. (Ω) at V_{GS} = 2.5 V	0.222
$R_{DS(on)}$ max. (Ω) at V_{GS} = 1.8 V	0.303
I_D (A)	± 1.2
Configuration	Level-Shift

ORDERING INFORMATION	
Package	SC-70
Lead (Pb)-free	Si1869DH-T1-E3
Lead (Pb)-free and halogen-free	Si1869DH-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage (D2-S2)		V_{DS}	-20	V
Input voltage		V_{IN}	20	
ON/OFF voltage		$V_{ON/OFF}$	8	
Load current	Continuous [a, b]	I_L	± 1.2	A
	Pulsed [b, c]		± 3	
Continuous intrinsic diode conduction [a]		I_S	-0.4	
Maximum power dissipation [a]		P_D	1	W
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
ESD rating, MIL-STD-883D human body model (100 pF, 1500 Ω)		ESD	2	kV

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient (continuous current) [a]	R_{thJA}	100	125	°C/W
Maximum junction-to-foot (Q2)	R_{thJF}	44	55	

Notes

a. Surface mounted on FR4 board
b. V_{IN} = 20 V, $V_{ON/OFF}$ = 8 V, T_A = 25 °C
c. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2 %

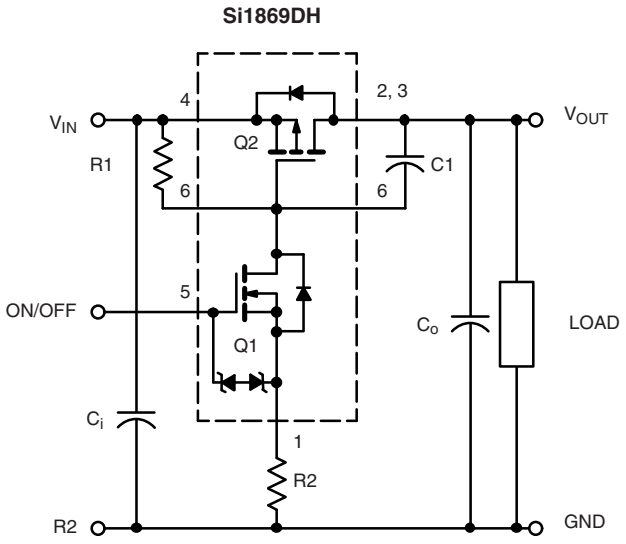
SPECIFICATIONS (T_A = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
OFF Characteristics						
Reverse leakage current	I_{FL}	V_{IN} = 8 V, $V_{ON/OFF}$ = 0 V	-	-	1	µA
Diode forward voltage	V_{SD}	I_S = -0.4 A	0.4	0.6	1.1	V
ON Characteristics						
Input voltage range [a]	V_{IN}		1.8	-	20	V
Drain to source breakdown voltage (p-channel)	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-20	-	-	
On-resistance (p-channel) at 1 A	$R_{DS(on)}$	$V_{ON/OFF}$ = 1.5 V, V_{IN} = 4.5 V, I_D = 1.2 A	-	0.132	0.165	Ω
		$V_{ON/OFF}$ = 1.5 V, V_{IN} = 2.5 V, I_D = 1 A	-	0.177	0.222	
		$V_{ON/OFF}$ = 1.5 V, V_{IN} = 1.8 V, I_D = 0.7 A	-	0.242	0.303	
On-state (p-channel) drain-current	$I_{D(on)}$	$V_{IN-OUT} \leq$ 0.2 V, V_{IN} = 5 V, $V_{ON/OFF}$ = 1.5 V	1	-	-	A
		$V_{IN-OUT} \leq$ 0.3 V, V_{IN} = 3 V, $V_{ON/OFF}$ = 1.5 V	1	-	-	

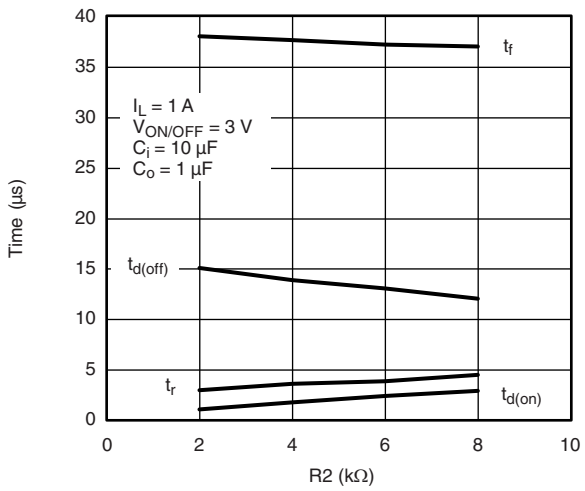
Note

a. V_{IN} = < 12 V, $V_{ON/OFF}$ = 8 V, T_A = 25 °C; recommended application specifications

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

APPLICATION CIRCUITS





Note: For R2 switching variations with other V_{IN}/R1 combinations see Typical Characteristics

Switching Variation
R2 at V_{IN} = 2.5 V, R1 = 20 kΩ

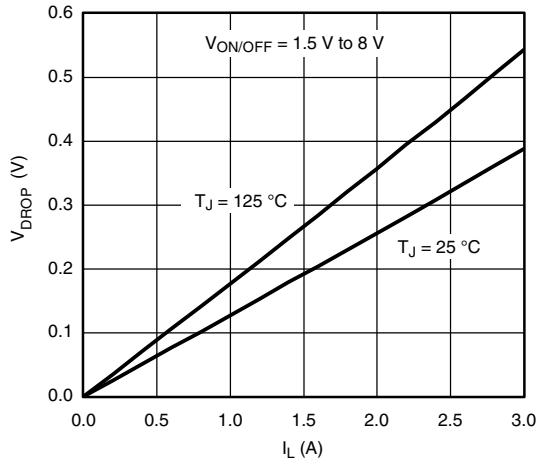
COMPONENTS		
R1	Pull-Up Resistor	Typical 10 kΩ to 1 MΩ [a]
R2	Optional Slew-Rate Control	Typical 0 to 100 kΩ [a]
C1	Optional Slew-Rate Control	Typical 1000 pF

Note

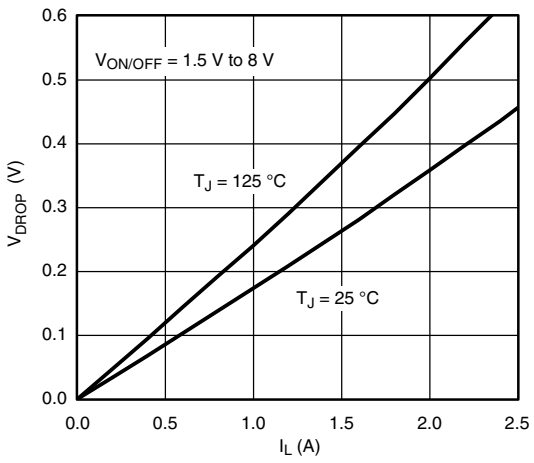
a. Minimum R1 value should be at least 10 x R2 to ensure Q1 turn-on

The Si1869DH is ideally suited for high side load switching in portable applications. The integrated n-channel level-shift device saves space by reducing external components. The slew rate is set externally so that rise-times can be tailored to different load types.

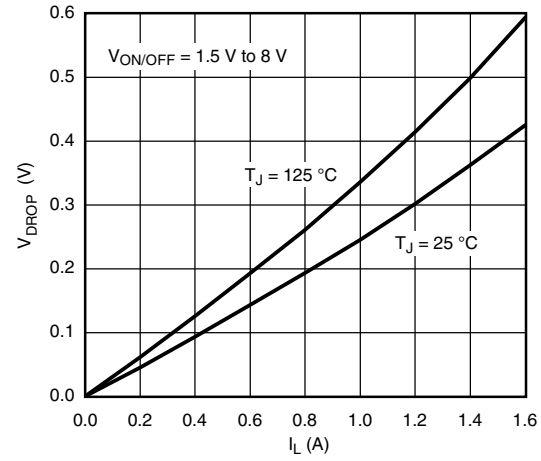
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



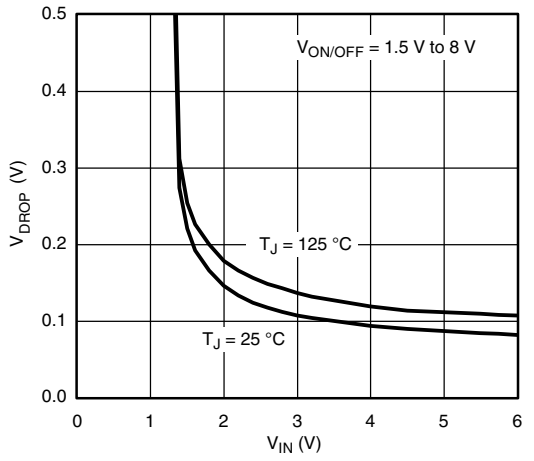
V_{DROP} vs. I_L at V_{IN} = 4.5 V



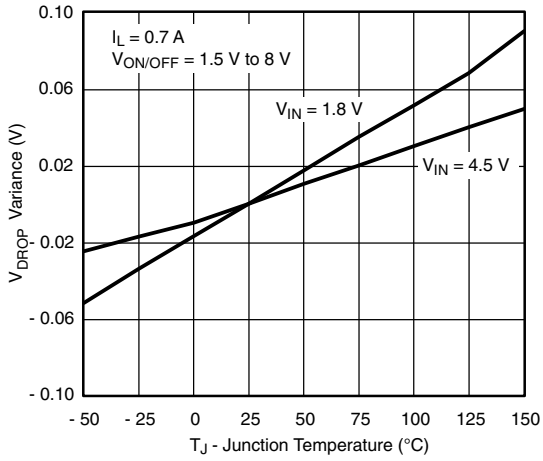
V_{DROP} vs. I_L at V_{IN} = 2.5 V



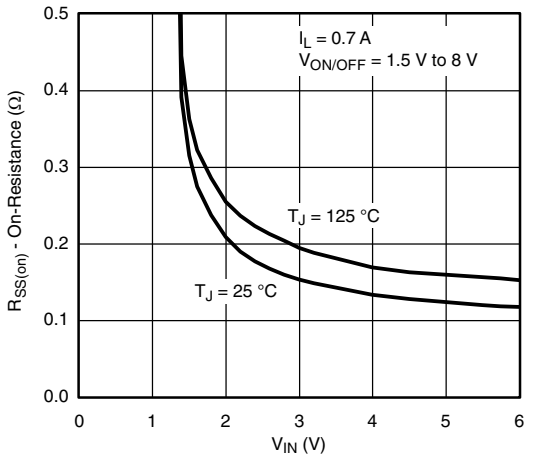
V_{DROP} vs. I_L at V_{IN} = 1.8 V



V_{DROP} vs. V_{IN} at I_L = 0.7 A

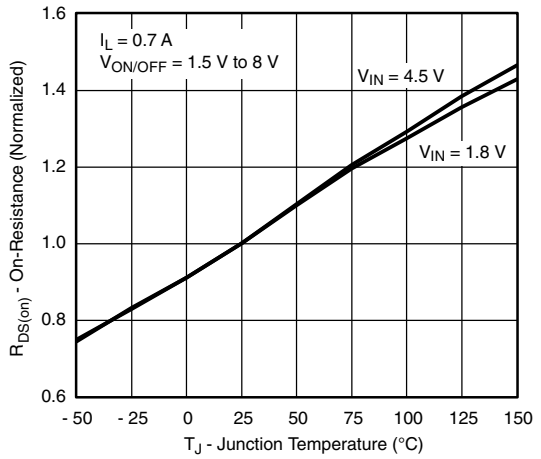


V_{DROP} Variance vs. Junction Temperature

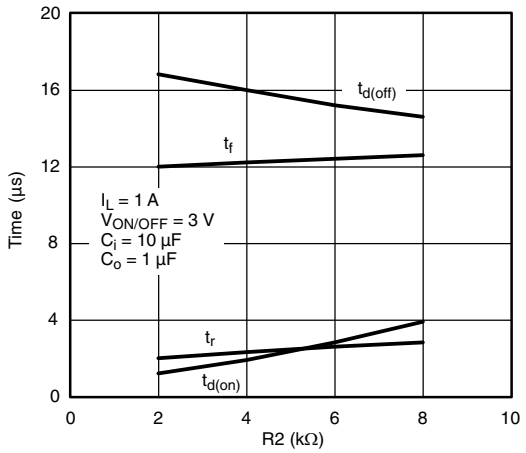


On-Resistance vs. Input Voltage

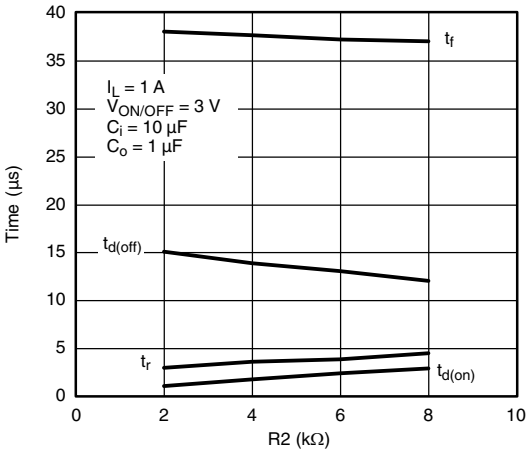
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



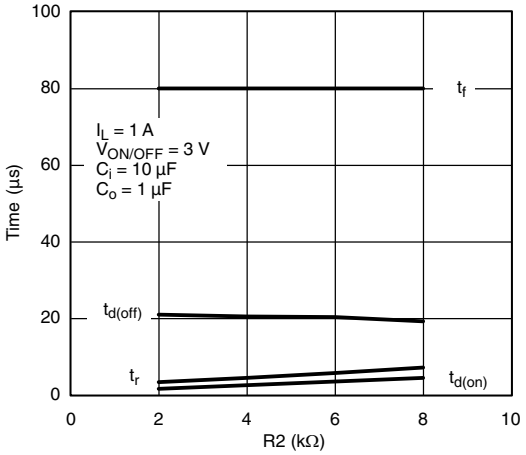
Normalized On-Resistance vs. Junction Temperature



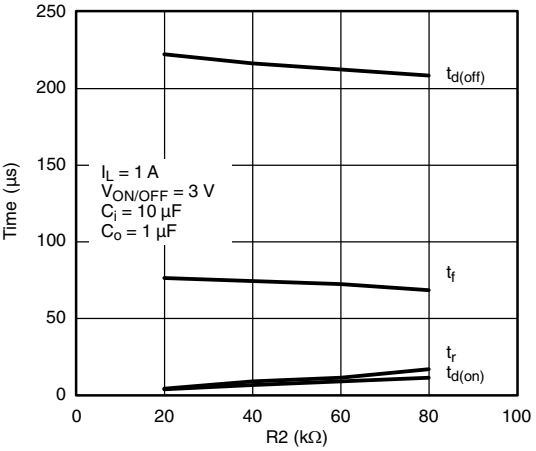
Switching Variation R2 at V_{IN} = 4.5 V, R1 = 20 kΩ



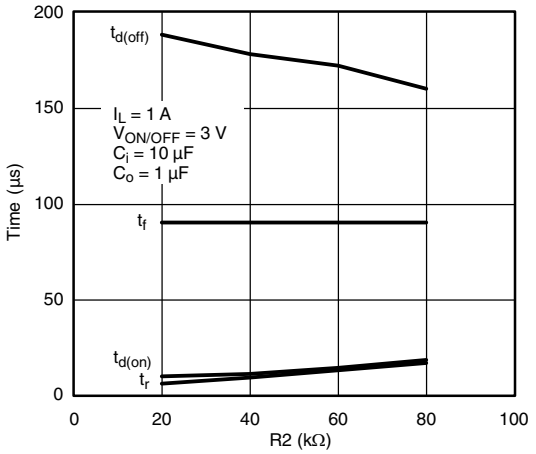
Switching Variation R2 at V_{IN} = 2.5 V, R1 = 20 kΩ



Switching Variation R2 at V_{IN} = 1.8 V, R1 = 20 kΩ

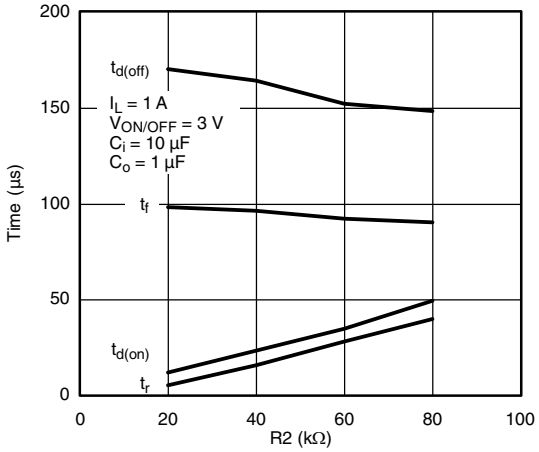


Switching Variation R2 at V_{IN} = 4.5 V, R1 = 300 kΩ

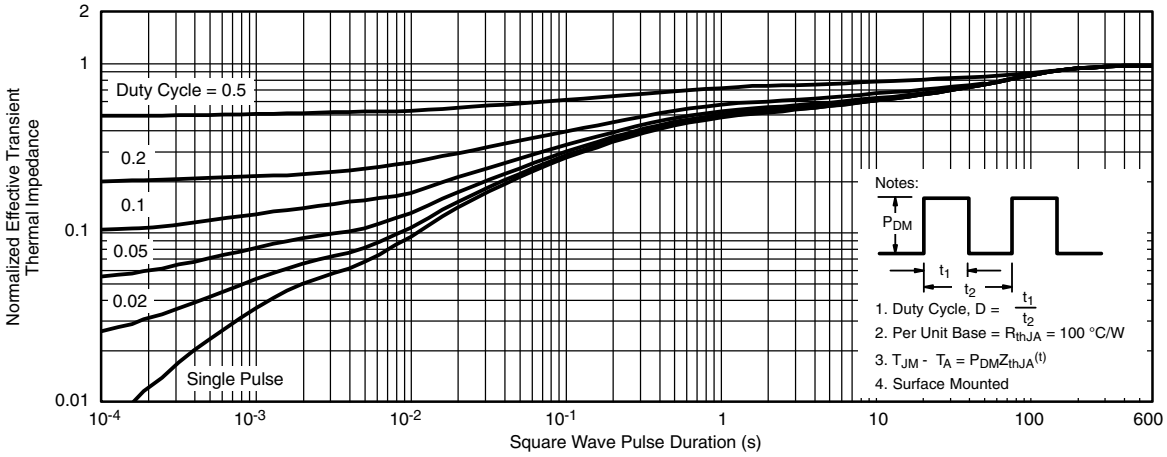


Switching Variation R2 at V_{IN} = 2.5 V, R1 = 300 kΩ

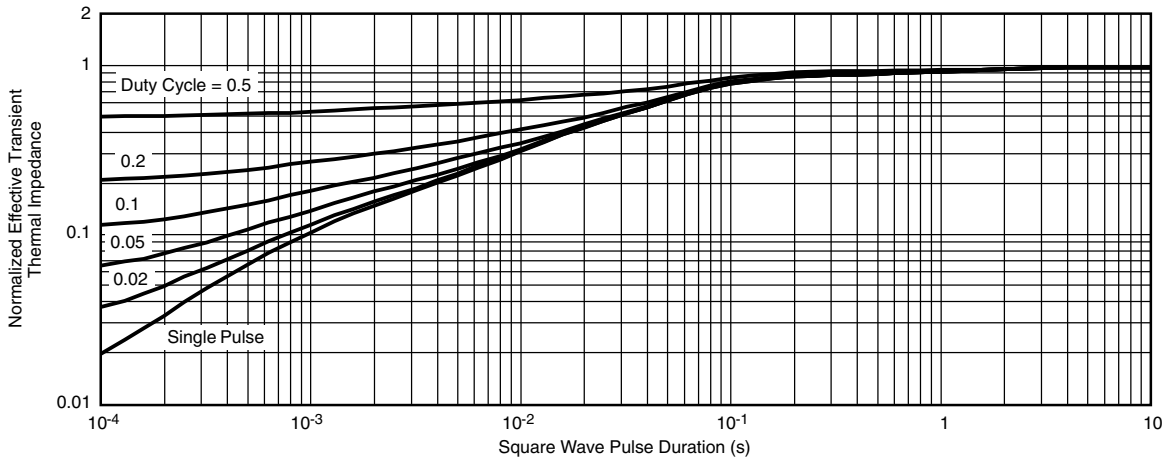
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Switching Variation R2 at V_{IN} = 1.8 V, R1 = 300 kΩ



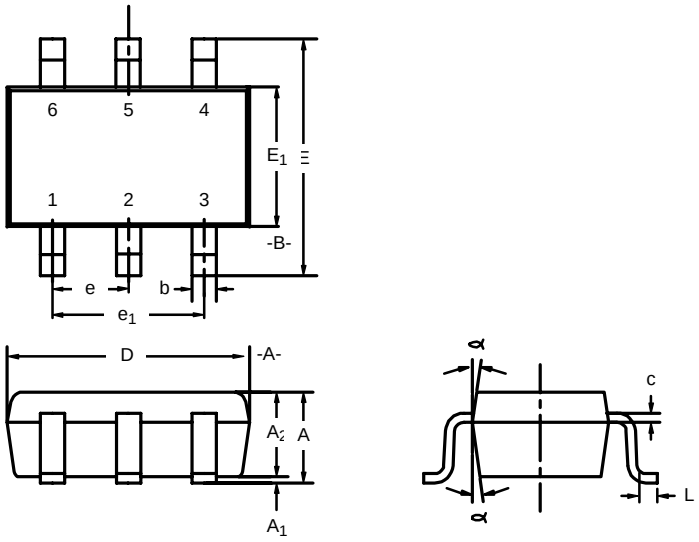
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73449.

SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	–	1.10	0.035	–	0.043
A_1	–	–	0.10	–	–	0.004
A_2	0.80	–	1.00	0.031	–	0.039
b	0.15	–	0.30	0.006	–	0.012
c	0.10	–	0.25	0.004	–	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E_1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e_1	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance

INTRODUCTION

The new dual 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the dual-channel version.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration. Both n-and p-channel devices are available in this package – the drawing example below illustrates the p-channel device.

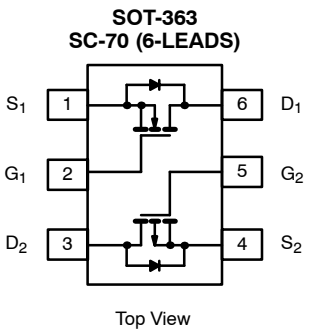


FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286) for the SC-70 6-pin basic pad layout and dimensions. This pad pattern is sufficient for the low-power applications for which this package is intended. Increasing the drain pad pattern (Figure 2) yields a reduction in thermal resistance and is a preferred footprint.

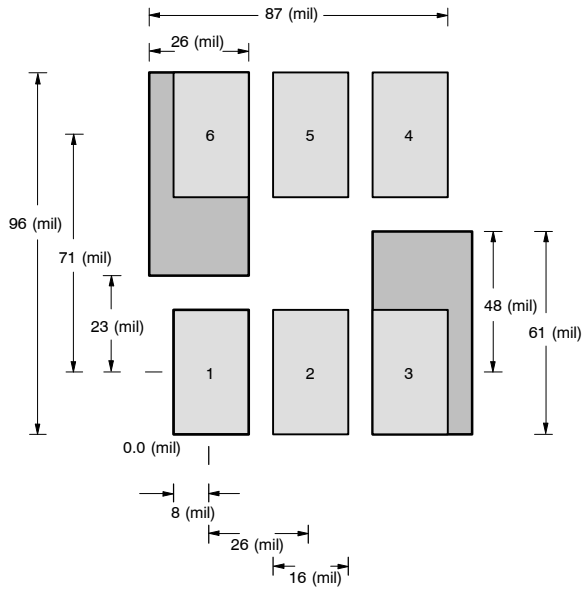


FIGURE 2. SC-70 (6 leads) Dual

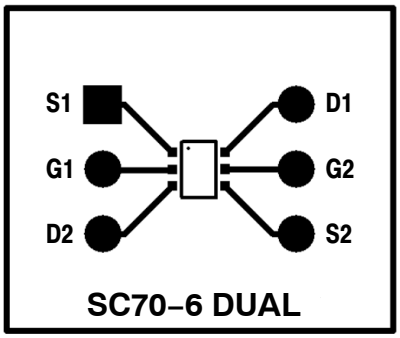
EVALUATION BOARD FOR THE DUAL-CHANNEL SC70-6

The 6-pin SC-70 evaluation board (EVB) shown in Figure 3 measures 0.6 in. by 0.5 in. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows for examination from the outer pins to the 6-pin DIP connections, permitting test sockets to be used in evaluation testing.

The thermal performance of the dual 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was then repeated using the 1-inch^2 PCB with dual-side copper coating.

A helpful way of displaying the thermal performance of the 6-pin SC-70 dual copper leadframe is to compare it to the traditional Alloy 42 version.

Front of Board SC70-6



Back of Board SC70-6

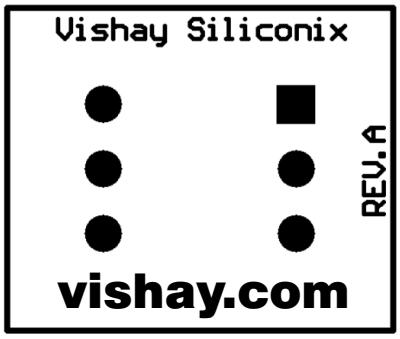


FIGURE 3.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package is measured as junction-to-foot thermal resistance, in which the "foot" is the drain lead of the device as it connects with the body. The junction-to-foot thermal resistance for this device is typically 80°C/W, with a maximum thermal resistance of approximately 100°C/W. This data compares favorably with another compact, dual-channel package – the dual TSOP-6 – which features a typical thermal resistance of 75°C/W and a maximum of 90°C/W.

Power Dissipation

The typical $R\theta_{JA}$ for the dual-channel 6-pin SC-70 with a copper leadframe is 224°C/W steady-state, compared to 413°C/W for the Alloy 42 version. All figures are based on the 1-inch^2 FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at varying ambient temperatures.

Alloy 42 Leadframe

ALLOY 42 LEADFRAME	
Room Ambient 25 °C	**Elevated Ambient 60 °C**
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^oC - 25^oC}{413^oC/W}$	$P_D = \frac{150^oC - 60^oC}{413^oC/W}$
P_D = 303 mW	P_D = 218 mW

COOPER LEADFRAME	
Room Ambient 25 °C	**Elevated Ambient 60 °C**
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^oC - 25^oC}{224^oC/W}$	$P_D = \frac{150^oC - 60^oC}{224^oC/W}$
P_D = 558 mW	P_D = 402 mW

Although they are intended for low-power applications, devices in the 6-pin SC-70 dual-channel configuration will handle power dissipation in excess of 0.5 W.

TESTING

To further aid the comparison of copper and Alloy 42 leadframes, Figures 4 and 5 illustrate the dual-channel 6-pin SC-70 thermal performance on two different board sizes and pad patterns. The measured steady-state values of $R\theta_{JA}$ for the dual 6-pin SC-70 with varying leadframes are as follows:

LITTLE FOOT 6-PIN SC-70		
	Alloy 42	**Copper**
1) Minimum recommended pad pattern on the EVB board (see Figure 3).	518°C/W	344°C/W
2) Industry standard 1-inch^2 PCB with maximum copper both sides.	413°C/W	224°C/W

The results indicate that designers can reduce thermal resistance (θJA) by 34% simply by using the copper leadframe device as opposed to the Alloy 42 version. In this example, a 174°C/W reduction was achieved without an increase in board area. If an increase in board size is feasible, a further 120°C/W reduction can be obtained by utilizing a 1-inch^2. PCB area.

The Dual copper leadframe versions have the following suffix:

Dual:	Si19xxEDH
Compl.:	Si15xxEDH

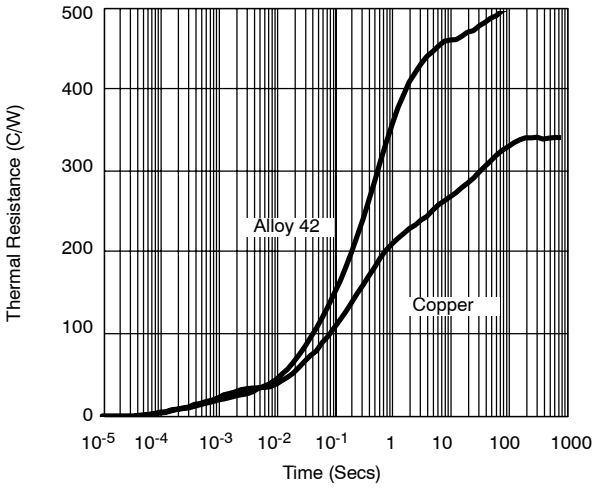


FIGURE 4. Dual SC70-6 Thermal Performance on EVB

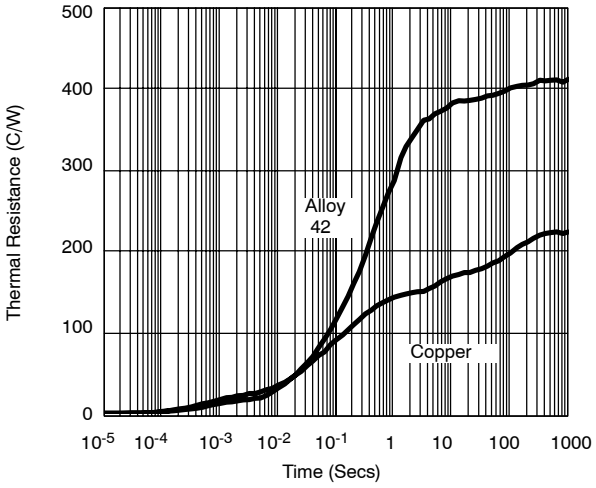
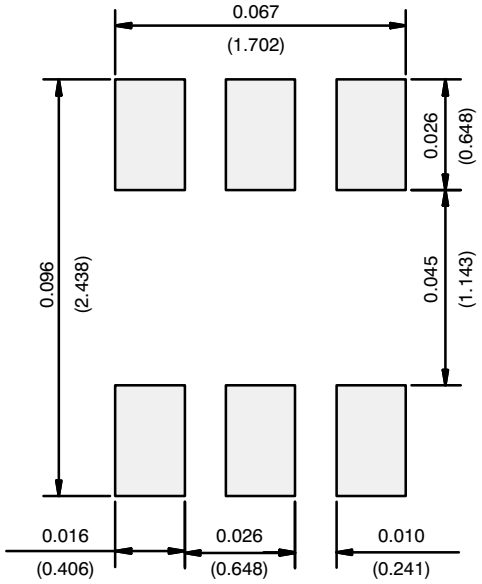


FIGURE 5. Dual SC70-6 Comparison on 1-inch^2 PCB

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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