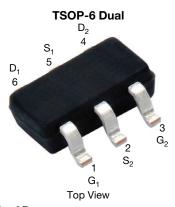


Vishay Siliconix

Automotive Dual P-Channel 30 V (D-S) 175 °C MOSFET



Marking code: 9B

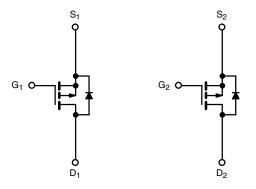
PRODUCT SUMMARY					
V _{DS} (V)	-30				
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	-0.155				
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5 \text{ V}$	-0.300				
I _D (A)	-2.32				
Configuration	Dual				

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_q and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912







P-Channel MOSFET

ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free and halogen-free	SQ3989EV (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (IA = 23 C, unless c			
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V _{DS}	-30	V	
Gate-source voltage		V _{GS}	± 20	v
Continuous drain current (T _J = 150 °C) ^a	T _C = 25 °C		-2.5	
	T _C = 125 °C	I _D	-1.5	^
Pulsed drain current		I _{DM}	-10.2	A
Continuous source current (diode conduction) a	I _S	-2.1		
Maximum power dissipation ^a	T _C = 25 °C	Б	1.67	w
	T _C = 125 °C	P _D	0.56	VV
Unclamped inductive surge UIS	<u>.</u>	I _{AV}	-7	A
Operating junction and storage temperature range	ge	T _J , T _{sta}	-55 to +175	°C

THERMAL RESISTANCE RATING	S			
PARAMETER		SYMBOL	LIMIT	UNIT
Maximum junction-to-ambient ^a	Steady state	R _{thJA}	150	°C/W
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	90	C/VV

Note

a. Surface mounted on 1" x 1" FR4 board



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SPECIFICATIONS (T _J = 25°C, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Gate threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$		-0.6	-	-1.5	V	
Gate-body leakage	I _{GSS}	V_{DS}	$_{S} = 0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
Zero gate voltage drain		$V_{GS} = 0 V$	V _{DS} = -30 V	-	-	-1	μΑ	
current	I _{DSS}	$V_{GS} = 0 V$	$V_{DS} = -30 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$	-	-	-5		
On-state drain current a	I _{D(on)}	V _{GS} = -10 V	V _{DS} ≤ -5 V	-4	-	-	Α	
Drain-source on-state		V _{GS} = -10 V	I _D = -0.4 A	-	0.140	0.155	Ω	
resistance ^a	R _{DS(on)}	V _{GS} = -4.5 V	I _D = -0.2 A	-	0.265	0.300	Ω	
Forward transconductance ^a	9 _{fs}	V _{DS} = -5 V, I _D = -1 A		-	2.2	-	S	
Diode forward voltage a	V _{SD}	I _S = -0.5 A, V _{GS} = 0 V		-	-0.83	-1.1	V	
Dynamic ^b								
Total gate charge	Q_g			-	8.6	11.1		
Gate-source charge	Q _{gs}	$V_{GS} = -10 \text{ V}$	$V_{DS} = -15 \text{ V}, I_D = -3 \text{ A}$	-	1.2	-	nC	
Gate-drain charge	Q_{gd}			-	3	-		
Gate resistance	R_g	f = 1 MHz		2.5	-	7.2	Ω	
Turn-on delay time	t _{d(on)}			-	5.7	8		
Rise time	t _r	V_{DD} = -10 V, R_L = 10 Ω $I_D \cong$ -1 A, V_{GEN} = -10 V, R_g = 1 Ω		-	3	4	ns	
Turn-off delay time	t _{d(off)}			-	13.8	18		
Fall time	t _f			-	2	3		

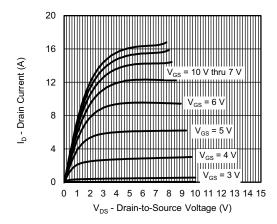
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

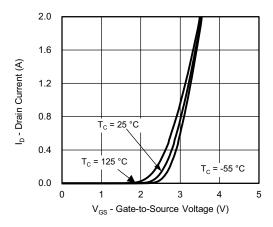
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



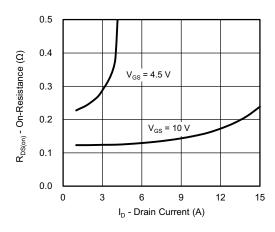
TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



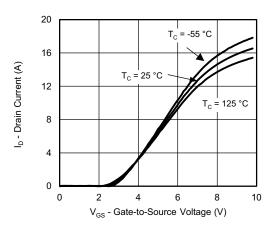
Output Characteristics



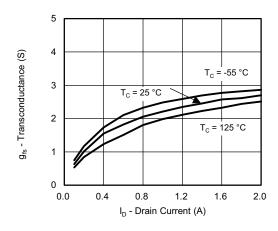
Transfer Characteristics



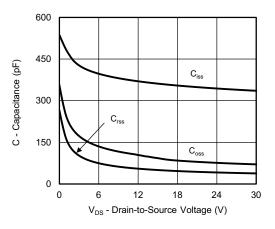
On-Resistance vs. Drain Current



Transfer Characteristics



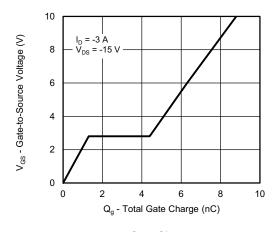
Transconductance



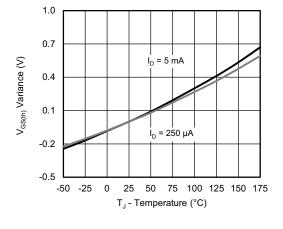
Capacitance



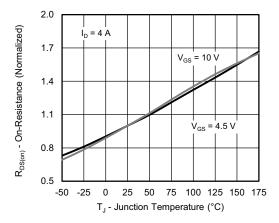
TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



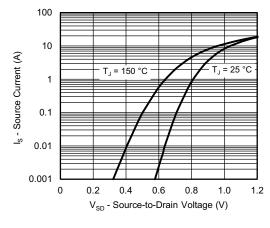
Gate Charge



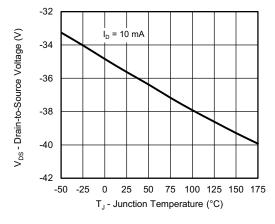
Threshold Voltage



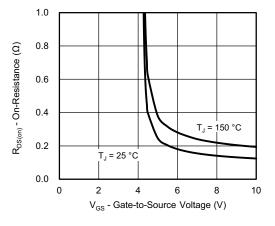
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



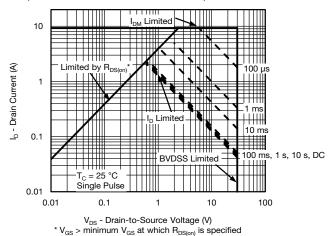
Drain Source Breakdown vs. Junction Temperature



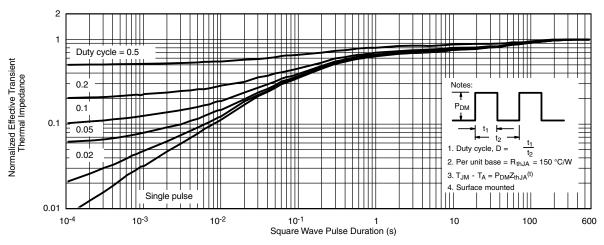
On-Resistance vs. Gate-to-Source Voltage



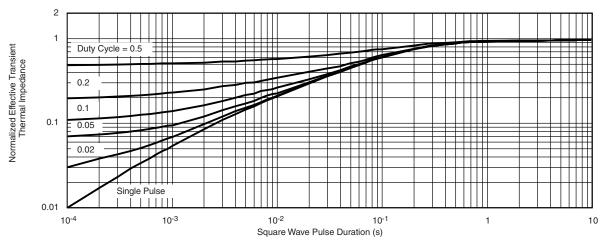
TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

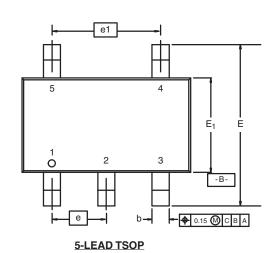
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg275059.

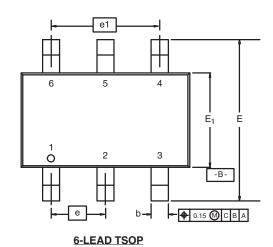


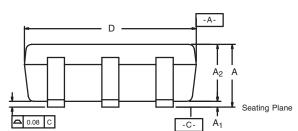


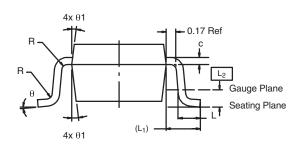
TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C









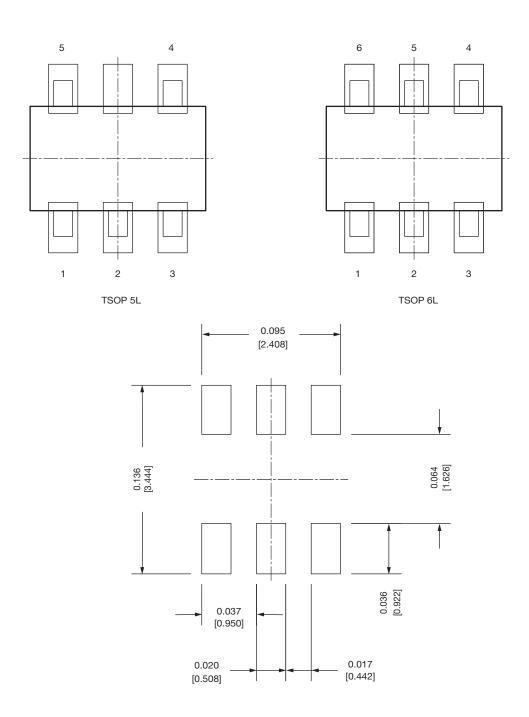
	MILLIMETERS			INCHES			
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.91	-	1.10	0.036	-	0.043	
A ₁	0.01	-	0.10	0.0004	-	0.004	
A ₂	0.90	-	1.00	0.035	0.038	0.039	
b	0.30	0.32	0.45	0.012	0.013	0.018	
С	0.10	0.15	0.20	0.004	0.006	0.008	
D	2.95	3.05	3.10	0.116	0.120	0.122	
Е	2.70	2.85	2.98	0.106	0.112	0.117	
E ₁	1.55	1.65	1.70	0.061	0.065	0.067	
е		0.95 BSC		0.0374 BSC			
e ₁	1.80	1.90	2.00	0.071	0.075	0.079	
L	0.32	-	0.50	0.012	-	0.020	
L ₁	0.60 Ref			0.024 Ref			
L ₂		0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-	
θ	0°	4°	8°	0°	4°	8°	
θ_1	7° Nom			7° Nom			
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540							

Document Number: 71200 18-Dec-06

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Recommended Land Pattern For TSOP-5L / TSOP-6L



Note

• All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022 DWG: 3010



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