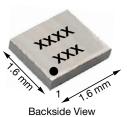
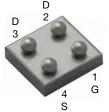
Vishay Siliconix

P-Channel 20 V (D-S) MOSFET

MICRO FOOT® 1.6 x 1.6





Bump Side View

PRODUCT SUMMARY						
V _{DS} (V)	-20					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5 \text{ V}$	0.021					
$R_{DS(on)}$ max. (Ω) at V_{GS} = -2.5 V	0.025					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.8 \text{ V}$	0.039					
Q _g typ. (nC)	31.2					
I _D (A)	-9.7 ^a					
Configuration	Single					

FEATURES

- TrenchFET® Gen III p-channel power MOSFET
- Low 0.6 mm maximum height
- · Low on-resistance
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912

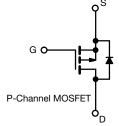


RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- · Load switch
 - With low voltage drop
- Power management in batteryoperated, mobile, and wearable devices



ORDERING INFORMATION	
Package	MICRO FOOT
Lead (Pb)-free and halogen-free	Si8481DB-T1-E1

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	-20	V	
Gate-source voltage		V _{GS}	± 8	v	
Continuous drain current (T _J = 150 °C)	T _A = 25 °C		-9.7 ^a		
	T _A = 70 °C		-7.8 ^a		
	T _A = 25 °C	I _D	-6.2 ^b		
	T _A = 70 °C		-5 b	Α	
Pulsed drain current (t = 100 μs)		I _{DM}	-30		
	T _A = 25 °C		-2.3 ^a		
Continuous source-drain diode current	T _A = 70 °C	I _S	-0.92 ^b		
	T _A = 25 °C		2.8 ^a		
Manian and a sure discipation	T _A = 70 °C		1.8 ^a	14/	
Maximum power dissipation	T _A = 25 °C	P _D	1.1 ^b	W	
	T _A = 70 °C		0.73 b		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150		
Package reflow conditions ^c		VPR	260	°C	
		IR / convection			

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient a, f	+ 50	В	35	45	°C/W	
Maximum junction-to-ambient b, g	t = 5 s	R _{thJA}	85	110		

Notes

- a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
- b. Surface mounted on 1" \times 1" FR4 board with minimum copper, t = 5 s.
- c. Refer to IPC / JEDEC® (J-STD-020), no manual or hand soldering.
- d. In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.
- e. Based on $T_A = 25$ °C.
- f. Maximum under steady state conditions is 85 °C/W.
- g. Maximum under steady state conditions is 175 °C/W.



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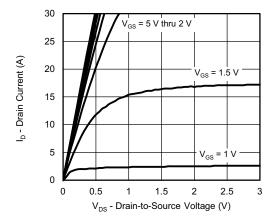
PARAMETER SYMBOL TEST CONDITIONS				TYP.	MAX.	UNIT
Static			•			
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-20	-	-	٧
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	1 050 A	-	-13	-	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	-	2.5	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.4	-	-0.9	٧
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$	-	-	± 100	nA
-		V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1	
Zero gate voltage drain current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	μA
On-state drain current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-5	-	-	Α
	, ,	$V_{GS} = -4.5 \text{ V}, I_D = -3 \text{ A}$	-	0.017	0.021	
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = -2.5 \text{ V}, I_D = -3 \text{ A}$	-	0.020	0.025	Ω
		V _{GS} = -1.8 V, I _D = -1 A	-	0.026	0.039	
Forward transconductancea	9fs	$V_{DS} = -5 \text{ V}, I_{D} = -3 \text{ A}$	-	22	-	S
Dynamic ^b			•			
Input capacitance	C _{iss}		-	2500	-	pF
Output capacitance	Coss	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	320	-	
Reverse transfer capacitance	C _{rss}		-	260	-	
Total gate charge	Qg	$V_{DS} = -10 \text{ V}, V_{GS} = -8 \text{ V}, I_D = -3 \text{ A}$	-	54	81	
		$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -3 \text{ A}$	-	31.2	47	
Gate-source charge	Q_{gs}	V 40VV 45VI 04	-	2.7	-	nC
Gate-drain charge	Q_{gd}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -3 \text{ A}$	-	6.3	-	
Gate resistance	Rg	f = 1 MHz	-	17	-	Ω
Turn-on delay time	t _{d(on)}		-	16	30	
Rise time	t _r	V_{DD} = -10 V, R_L = 3.3 Ω , $I_D \cong$ -3 A,	-	25	50	1
Turn-off delay time	t _{d(off)}	$V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$	-	300	600	
Fall time	t _f		-	110	220	
Turn-on delay time	t _{d(on)}		-	7	15	ns
Rise time	t _r	$V_{DD} = -10 \text{ V}, R_1 = 3.3 \Omega, I_D \cong -3 \text{ A},$	-	20	40	
Turn-off delay time	t _{d(off)}	$V_{GEN} = -8 \text{ V}, R_g = 1 \Omega$	-	400	800	
Fall time	t _f		-	110	220	
Drain-Source Body Diode Characteristi	cs		•			
Continuous source-drain diode current	Is	T _A = 25 °C	-	-	-2.3 ^c	_
Pulse diode forward current	I _{SM}		-	-	-15	Α
Body diode voltage	V _{SD}	$I_S = -3 \text{ A}, V_{GS} = 0 \text{ V}$	-	-0.8	-1.2	V
Body diode reverse recovery time	t _{rr}		-	150	300	ns
Body diode reverse recovery charge	Q _{rr}		-	235	470	nC
Reverse recovery fall time	ta	$I_F = -3 \text{ A, dI/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 °\text{C}$		47	-	
Reverse recovery rise time	t _b		_	103	_	ns

Notes

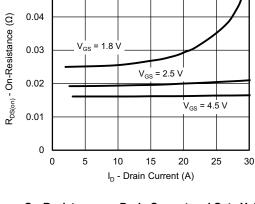
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



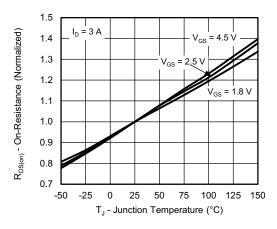


Output Characteristics

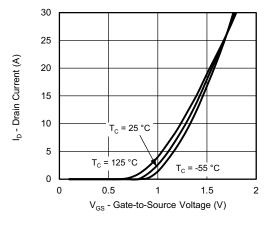


0.05

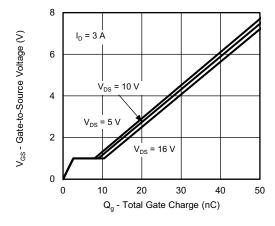
On-Resistance vs. Drain Current and Gate Voltage



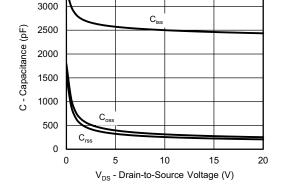
On-Resistance vs. Junction Temperature



Transfer Characteristics



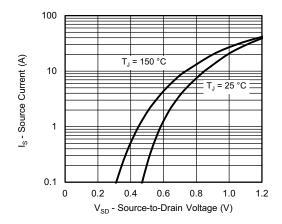
Gate Charge



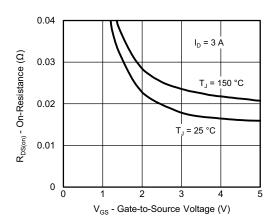
Capacitance

3500

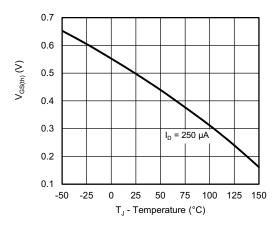




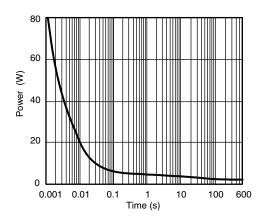
Source-Drain Diode Forward Voltage



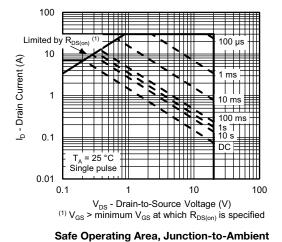
On-Resistance vs. Gate-to-Source Voltage



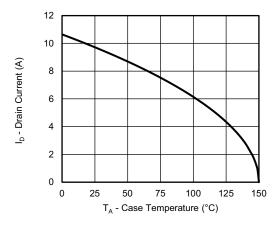
Threshold Voltage

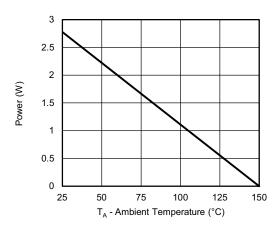


Single Pulse Power, Junction-to-Ambient







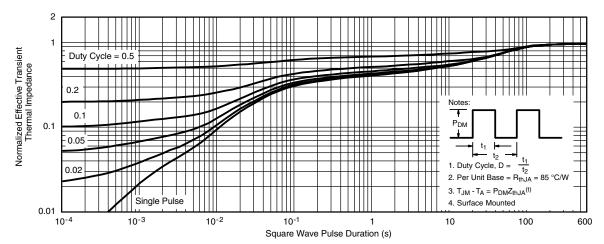


Current Derating a

Power, Junction-to-Ambient ^a

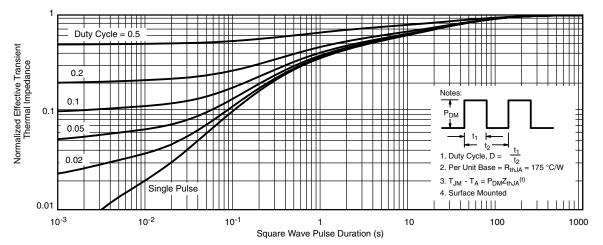
Note

a. When surface mounted on 1" \times 1" FR4 board with full copper, t = 5 s.



Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with maximum copper)





Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with minimum copper)

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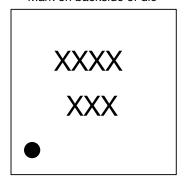


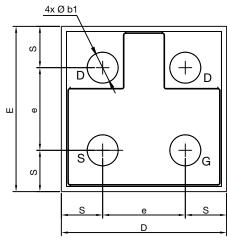
www.vishay.com

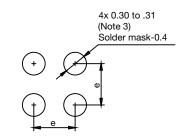
Vishay Siliconix

MICRO FOOT®: 4-Bumps (1.6 mm x 1.6 mm, 0.8 mm Pitch, 0.290 mm Bump Height)

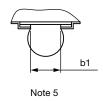
Mark on backside of die

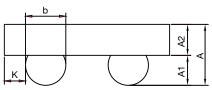






Recommended land pattern





Notes

- 1. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
- 2. Backside surface is coated with a Ti/Ni/Ag layer.
- 3. Non-solder mask defined copper landing pad.
- 4. Laser marks on the silicon die back.
- 5. "b1" is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
- 6. is the location of pin 1

DIM.	MILLIMETERS			INCHES			
DIIVI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.550	0.575	0.600	0.0217	0.0226	0.0236	
A1	0.260	0.275	0.290	0.0102	0.0108	0.0114	
A2	0.290	0.300	0.310	0.0114	0.0118	0.0122	
b	0.370	0.390	0.410	0.0146	0.0153	0.0161	
b1		0.300			0.0118		
е	e 0.800 0.0314						
s	0.360	0.380	0.400	0.0141	0.0150	0.0157	
D	1.520	1.560	1.600	0.0598	0.0614	0.0630	
E	1.520	1.560	1.600	0.0598	0.0614	0.0630	
K	0.155	0.185	0.215	0.0061	0.0073	0.0085	

Note

• Use millimeters as the primary measurement.

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DWG: 6038

Revision: 27-Apr-15 1 Document Number: 69378



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