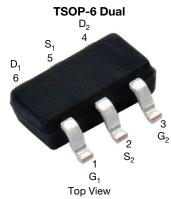
SQ3987EV

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Vishay Siliconix

Automotive Dual P-Channel 30 V (D-S) 175 °C MOSFET



Marking code: 8X

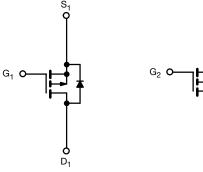
PRODUCT SUMMARY				
V _{DS} (V)	-30			
$R_{DS(on)} (\Omega)$ at $V_{GS} = -10 V$	-0.110			
$R_{DS(on)} (\Omega)$ at $V_{GS} = -4.5 V$	-0.185			
I _D (A)	-2.75			
Configuration	Dual			
Package	TSOP-6			

FEATURES

- TrenchFET[®] power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



RoHS COMPLIANT HALOGEN FREE



P-Channel MOSFET

D₂ P-Channel MOSFET

 S_2

	otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V _{DS}	-30	v	
Gate-source voltage	V _{GS}	± 20	v	
Continuous ducin ourrent (T 150 °C) à	T _C = 25 °C		-3	
Continuous drain current (T _J = 150 °C) ^a	T _C = 125 °C		-1.74	
Pulsed drain current	I _{DM}	-11	— A	
Continuous source current (diode conduction) ^a	I _S	-2.1	7	
Maximum neuror dissinction a	T _C = 25 °C	D	1.67	W
Maximum power dissipation ^a	T _C = 125 °C	P _D	0.56	
Unclamped inductive surge UIS		I _{AV}	-5	A
Operating junction and storage temperature ran	ge	T _J , T _{sta}	-55 to +175	°C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Maximum junction-to-ambient ^a	Steady state	R _{thJA}	150	°C/W	
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	90		

Note

a. Surface mounted on 1" x 1" FR4 board

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SPECIFICATIONS (T _J	= 25°C, ur	nless otherwise	noted)					
PARAMETER	SYMBOL	T	MIN.	TYP.	MAX.	UNIT		
Static								
Gate threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$		-1.5	-	-2.5	V	
Gate-body leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	-	± 100	nA	
Zero gate voltage drain current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = -30 V	-	-	-1	μA	
		$V_{GS} = 0 V$	V_{DS} = -30 V, T_{J} = 175 °C	-	-	-50		
On-state drain current ^a	I _{D(on)}	V _{GS} = -10 V	$V_{DS} \le -5 V$	-4	-	-	А	
Drain-source on-state resistance ^a	Б	$V_{GS} = -10 V$	I _D = -1.5 A	-	0.085	0.133	Ω	
	R _{DS(on)}	V _{GS} = -4.5 V	I _D = -2 A	-	0.135	0.185		
Forward transconductance a	g _{fs}	V	_{DS} = -5 V, I _D = -1 A	-	4.2	-	S	
Diode forward voltage ^a	V _{SD}	I _S	= -0.5 A, V _{GS} = 0 V	-	-0.83	-1.10	V	
Dynamic ^b								
Input capacitance	C _{iss}			-	456	570		
Output capacitance	Coss	$V_{GS} = 0 V$	$V_{DS} = -15 V$	-	85	106	pF	
Reverse capacitance	C _{rss}			-	59	74		
Total gate charge	Qg	V _{GS} = -10 V	V _{DS} = -15 V, I _D = -3 A	-	9.7	12.2		
Gate-source charge	Q _{gs}			-	1.3	-	nC	
Gate-drain charge	Q _{gd}			-	2	-	1	
Gate resistance	Rg	f = 1 MHz		9	-	24	Ω	
Turn-on delay time	t _{d(on)}	$V_{DD} = -10 \text{ V}, \text{ R}_{\text{L}} = 10 \Omega,$ $\text{I}_{\text{D}} \cong -1 \text{ A}, \text{ V}_{\text{GEN}} = -10 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		-	6.6	8.3		
Rise time	t _r			-	2.4	3]	
Turn-off delay time	t _{d(off)}			-	18.4	23	ns	
Fall time	t _f			-	2.2	2.8		
Source-Drain Diode Ratings	and Charac	teristic ^b		•				
Pulsed current	I _{SM}			-	-	-11	А	
Forward voltage	V _{SD}	I _F = 0.5 A, V _{GS} = 0 V		-	-0.83	-1.1	V	
Reverse recovery fall time	t _a	V _{DD} = -24 V, I _{FM} = -1.5 A, di/dt = 100 A/μs, R = 160 Ω, L = 1 mH, pulse W = 2 μs		-	9.1	-	ns	
Reverse recovery rise time	t _b			-	4.8	-	ns	
Body diode reverse recovery time	t _{rr}			-	14	28	ns	
Body diode reverse recovery charge	Q _{rr}			-	9	18	μC	
Body diode peak reverse recovery current	I _{RM(REC)}			-	-1.4	-	А	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing

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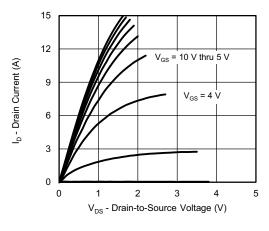
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

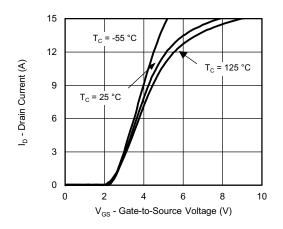


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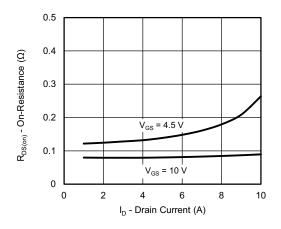
TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



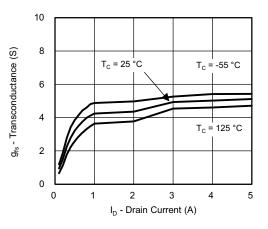
Output Characteristics



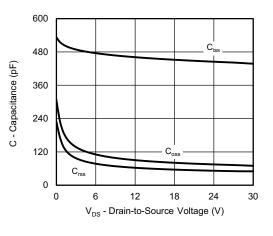
Transfer Characteristics



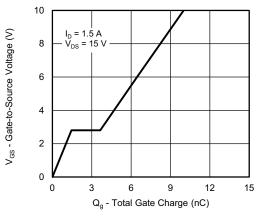
On-Resistance vs. Drain Current



Transconductance







Gate Charge

S19-0398-Rev. B, 06-May-2019

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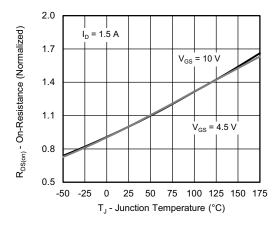
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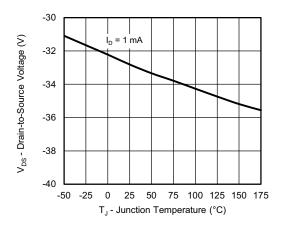
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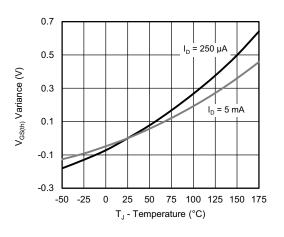
TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



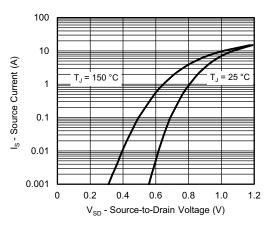
On-Resistance vs. Junction Temperature



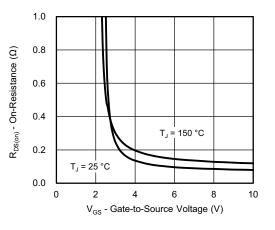
Drain Source Breakdown vs. Junction Temperature



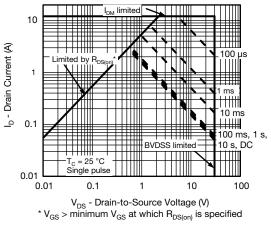
Threshold Voltage



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



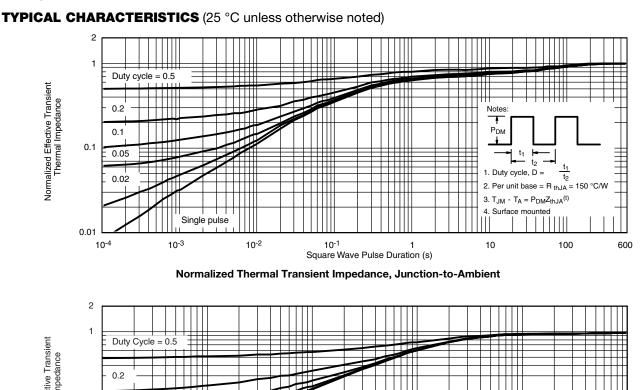
Safe Operating Area, Junction-to-Case

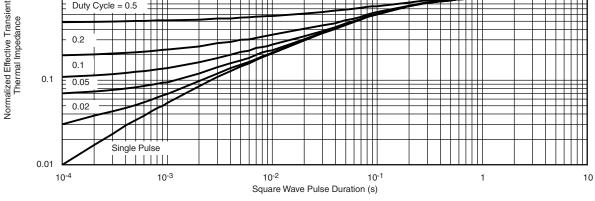
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Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75315.

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S19-0398-Rev. B, 06-May-2019



Package Information

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TSOP: 5/6-LEAD JEDEC Part Number: MO-193C









6-LEAD TSOP



	MIL	LIMETER	RS	INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
Α	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
С	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
Е	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
е	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref				0.024 Ref	
L ₂	0.25 BSC				0.010 BSC	
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ_1	7° Nom				7° Nom	
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540						

PAD Pattern



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Recommended Land Pattern For TSOP-5L / TSOP-6L





TSOP 5L





Note

• All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022	
DWG: 3010	

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