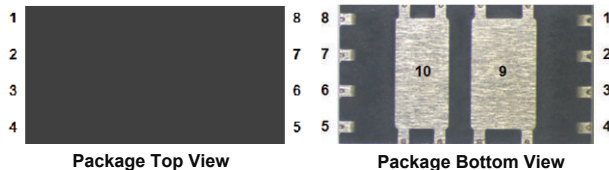




Automotive 40 V N- and P-Channel Common Drain MOSFET Pair and 200 V N-Channel MOSFET

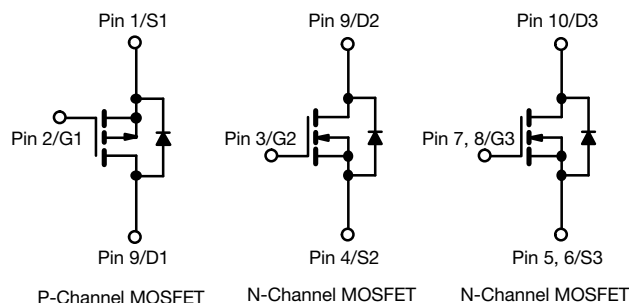


FEATURES

- Optimized triple die package
- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- AEC-Q101 qualified
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912

AUTOMOTIVE
GRADERoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY			
	N-CH 2	P-CH 1	N-CH 3
V_{DS} (V)	40	-40	200
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0092	0.030	0.075
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.0135	0.048	-
I_D (A)	30	-30	16
Q_g typ. (nC)	25.5	30.2	11
Configuration	N- and p-pair		
Package	Triple die		



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)						
PARAMETER	SYMBOL	N-CH 2	P-CH 1	N-CH 3	UNIT	
Drain-source voltage	V_{DS}	40	-40	200	V	
Gate-source voltage	V_{GS}	20	20	20		
Continuous drain current ($T_J = 175$ °C)	$T_C = 25$ °C $T_C = 125$ °C	I_D	30	-30	16	A
			30	-30	9.1	
Pulsed drain current ($t = 300$ μ s)		I_{DM}	120	-120	50	
Continuous source drain current	$T_C = 25$ °C $T_C = 125$ °C	I_S	30	-30	16	
			30	-30	10	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	26.5	-25	16	
Single pulse avalanche energy		E_{AS}	35	31	12.8	mJ
Maximum power dissipation	$T_C = 25$ °C	P_D	48	48	50	W
	$T_C = 125$ °C		16	16	16	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175			°C	

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	N-CH 2	P-CH 1	N-CH 3	UNIT
Junction-to-case (drain)	R_{thJC}	2.6	2.6	3.0	°C/W

Notes

- Package limited, $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch 2	40	-	-	V
		V _{GS} = 0 V, I _D = -250 μA	P-Ch 1	-40	-	-	
		V _{GS} = 0 V, I _D = 250 μA	N-Ch 3	200	-	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch 2	1.5	2.0	2.5	
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch 1	1.5	2.0	2.5	
		V _{DS} = V _{GS} , I _D = 250 μA	N-Ch 3	2.5	3.0	3.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	N-Ch 2	-	-	± 100	nA
			P-Ch 1	-	-	± 100	
			N-Ch 3	-	-	± 100	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	N-Ch 2	-	-	1	mA
		V _{DS} = -40 V, V _{GS} = 0 V	P-Ch 1	-	-	-1	
		V _{DS} = 200 V, V _{GS} = 0 V	N-Ch 3	-	-	1	
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 125 °C	N-Ch 2	-	-	50	
		V _{DS} = -40 V, V _{GS} = 0 V, T _J = 125 °C	P-Ch 1	-	-	-50	
		V _{DS} = 200 V, V _{GS} = 0 V, T _J = 125 °C	N-Ch 3	-	-	50	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch 2	25	-	-	A
		V _{DS} ≤ 5 V, V _{GS} = -10 V	P-Ch 1	-25	-	-	
		V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch 3	20	-	-	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 9.8 A	N-Ch 2	-	0.0077	0.0092	Ω
		V _{GS} = -10 V, I _D = -6 A	P-Ch 1	-	0.0220	0.0300	
		V _{GS} = 10 V, I _D = 5 A	N-Ch 3	-	0.0710	0.0750	
		V _{GS} = 4.5 V, I _D = 8.9 A	N-Ch 2	-	0.0940	0.0135	
		V _{GS} = 4.5 V, I _D = -4.7 A	P-Ch 1	-	0.0360	0.0480	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 9.8 A	N-Ch 2	-	65	-	S
		V _{DS} = -15 V, I _D = 6 A	P-Ch 1	-	16	-	
		V _{DS} = 15 V, I _D = 19 A	N-Ch 3	-	19	-	
Dynamic ^b							
Input capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	N-Ch 2	-	1474	-	pF
		V _{DS} = -20 V, V _{GS} = 0 V, f = 1 MHz	P-Ch 1	-	1302	-	
		V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	N-Ch 3	-	600	-	
Output capacitance	C _{oss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	N-Ch 2	-	218	-	
		V _{DS} = -20 V, V _{GS} = 0 V, f = 1 MHz	P-Ch 1	-	222	-	
		V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	N-Ch 3	-	70	-	
Reverse transfer capacitance	C _{rss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	N-Ch 2	-	89	-	nC
		V _{DS} = -20 V, V _{GS} = 0 V, f = 1 MHz	P-Ch 1	-	154	-	
		V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	N-Ch 3	-	5	-	
Total gate charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 10 A	N-Ch 2	-	23	-	
		V _{DS} = -20 V, V _{GS} = -10 V, I _D = -10 A	P-Ch 1	-	30.2	-	
		V _{DS} = 100 V, V _{GS} = 10 V, I _D = 10 A	N-Ch 3	-	11	-	
Gate-source charge	Q _{gs}	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 10 A	N-Ch 2	-	4.4	-	
		V _{DS} = -20 V, V _{GS} = -10 V, I _D = -10 A	P-Ch 1	-	4.1	-	
		V _{DS} = 100 V, V _{GS} = 10 V, I _D = 10 A	N-Ch 3	-	3.2	-	
Gate-drain charge	Q _{gd}	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 10 A	N-Ch 2	-	4.3	-	
		V _{DS} = -20 V, V _{GS} = -10 V, I _D = -10 A	P-Ch 1	-	7.4	-	
		V _{DS} = 100 V, V _{GS} = 10 V, I _D = 10 A	N-Ch 3	-	3	-	
Gate resistance	R _g	f = 1 MHz	N-Ch 2	-	-	2.1	Ω
			P-Ch 1	-	-	9.5	
			N-Ch 3	-	-	2.4	



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Dynamic ^b							
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω, I _D = 10 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch 2	-	8	-	ns
		V _{DD} = -20 V, R _L = 2 Ω, I _D = -10 A, V _{GEN} = -10 V, R _g = 1 Ω	P-Ch 1	-	7	-	
		V _{DD} = 100 V, R _L = 5.2 Ω, I _D = 10 A, V _{GEN} = 10 V, R _g = 2.5 Ω	N-Ch 3	-	9	-	
Rise time	t _r	V _{DD} = 20 V, R _L = 2 Ω, I _D = 10 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch 2	-	12	-	
		V _{DD} = -20 V, R _L = 2 Ω, I _D = -10 A, V _{GEN} = -10 V, R _g = 1 Ω	P-Ch 1	-	9	-	
		V _{DD} = 100 V, R _L = 5.2 Ω, I _D = 10 A, V _{GEN} = 10 V, R _g = 2.5 Ω	N-Ch 3	-	3	-	
Turn-off delay time	t _{d(off)}	V _{DD} = 20 V, R _L = 2 Ω, I _D = 10 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch 2	-	22	-	
		V _{DD} = -20 V, R _L = 2 Ω, I _D = -10 A, V _{GEN} = -10 V, R _g = 1 Ω	P-Ch 1	-	43	-	
		V _{DD} = 100 V, R _L = 5.2 Ω, I _D = 10 A, V _{GEN} = 10 V, R _g = 2.5 Ω	N-Ch 3	-	14	-	
Fall time	t _f	V _{DD} = 20 V, R _L = 2 Ω, I _D = 10 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch 2	-	10	-	
		V _{DD} = -20 V, R _L = 2 Ω, I _D = -10 A, V _{GEN} = -10 V, R _g = 1 Ω	P-Ch 1	-	19	-	
		V _{DD} = 100 V, R _L = 5.2 Ω, I _D = 10 A, V _{GEN} = 10 V, R _g = 2.5 Ω	N-Ch 3	-	2	-	
Source-Drain Diode Ratings and Characteristics							
Pulsed current	I _{SM}		N-Ch 2	-	-	120	A
			P-Ch 1	-	-	-120	
			N-Ch 3	-	-	50	
Forward voltage	V _{SD}	I _S = 6.5 A, V _{GS} = 0 V	N-Ch 2	-	0.79	-	V
		I _S = -3.4 A, V _{GS} = 0 V	P-Ch 1	-	-0.78	-	
		I _S = 19 A, V _{GS} = 0 V	N-Ch 3	-	0.9	-	

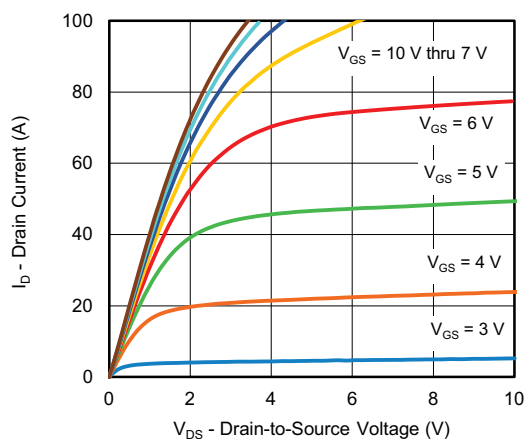
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

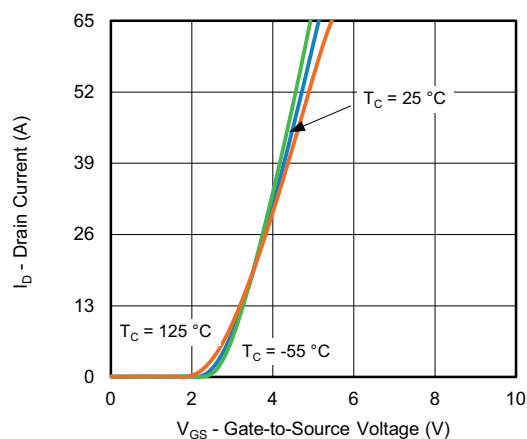
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



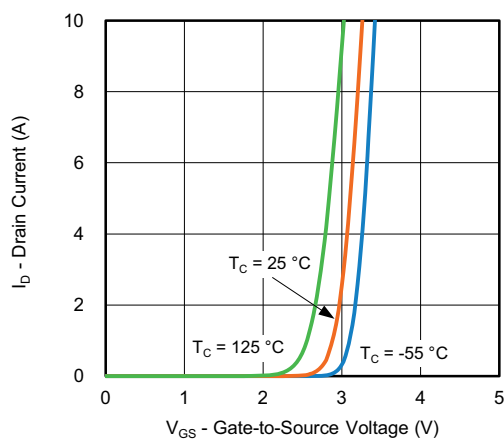
CHANNEL-1 TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



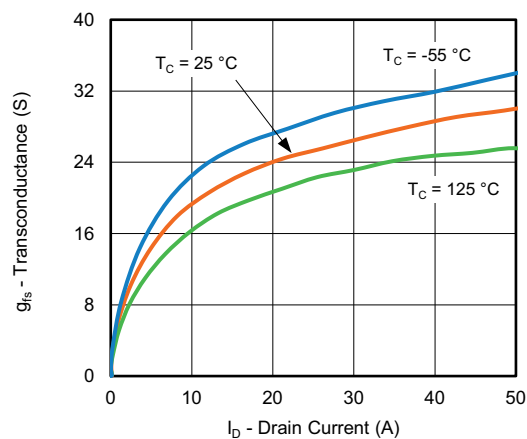
Output Characteristics



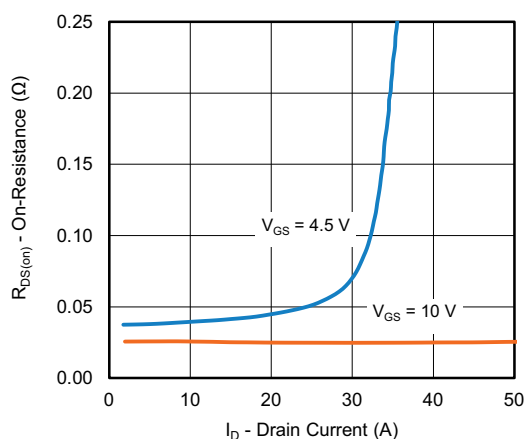
Transfer Characteristics



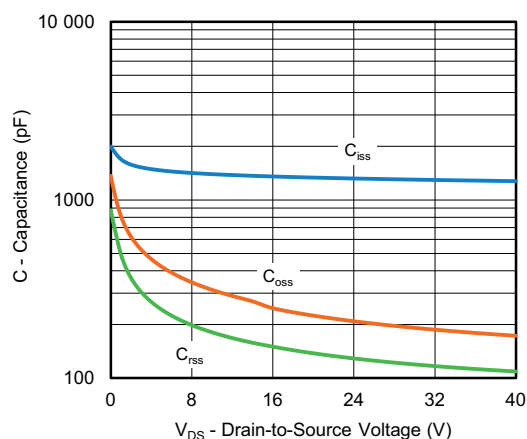
Transfer Characteristics



Transconductance



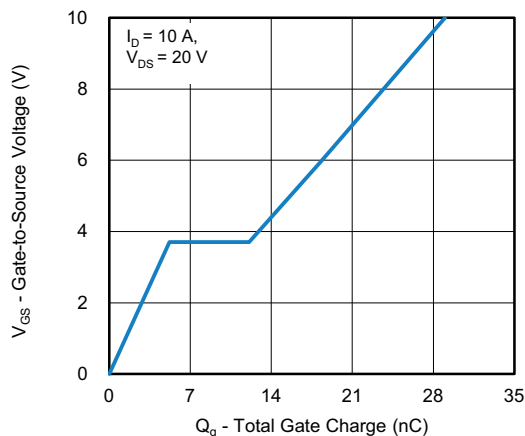
On-Resistance vs. Drain Current



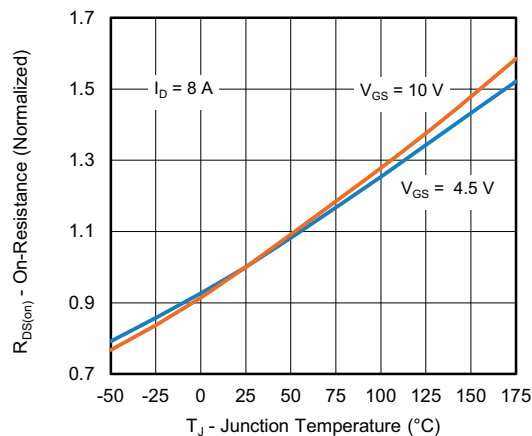
Capacitance



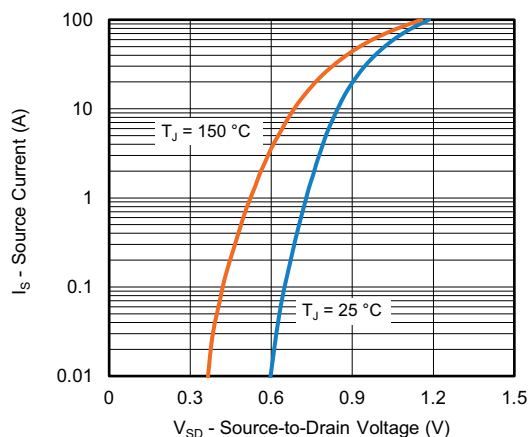
CHANNEL-1 TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



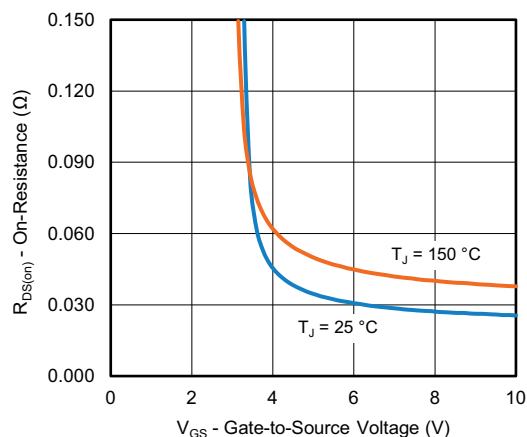
Gate Charge



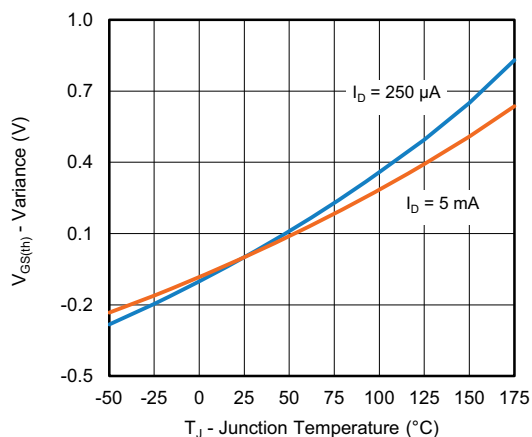
On-Resistance vs. Junction Temperature



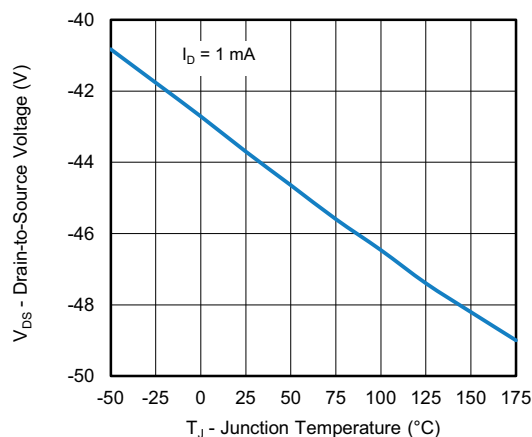
Source Drain Diode Forward Voltage



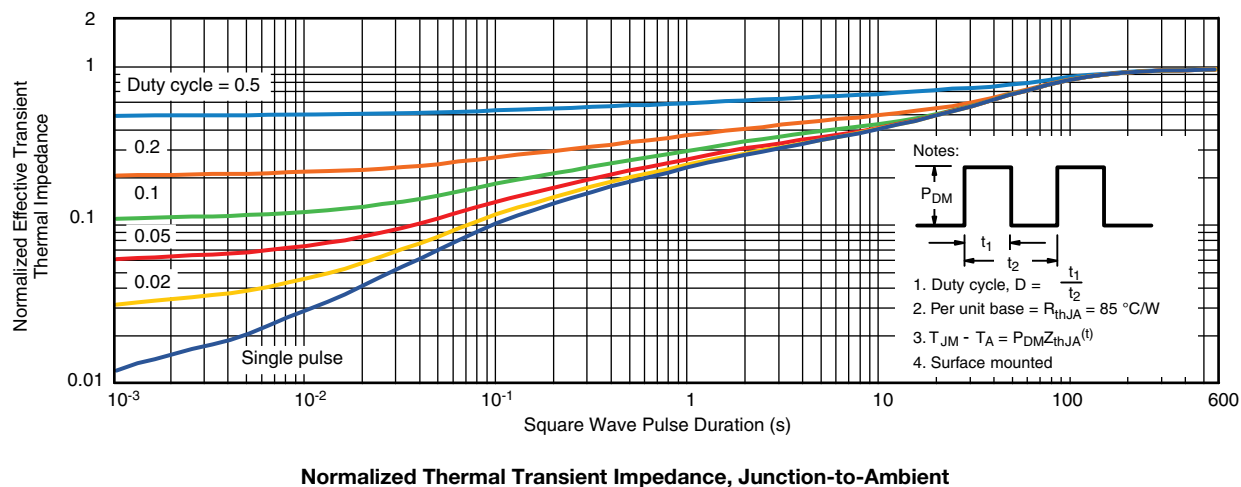
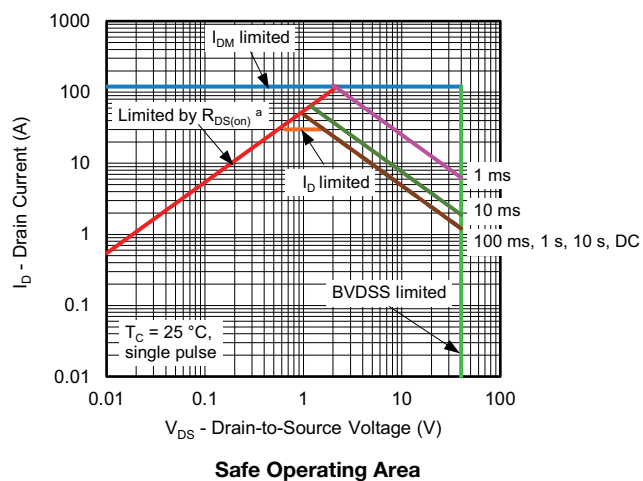
On-Resistance vs. Gate-to-Source Voltage



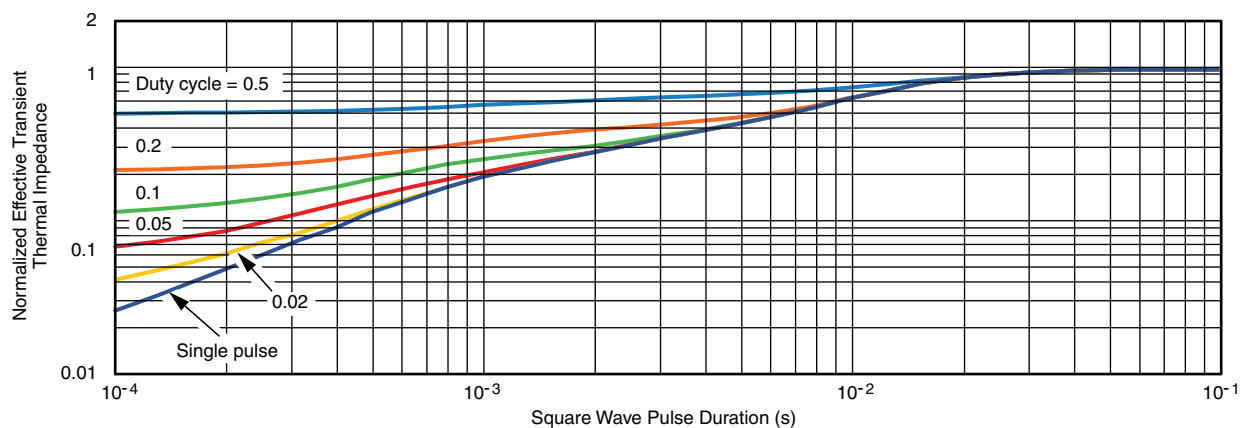
Threshold Voltage



Drain Source Breakdown vs. Junction Temperature

CHANNEL-1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Note

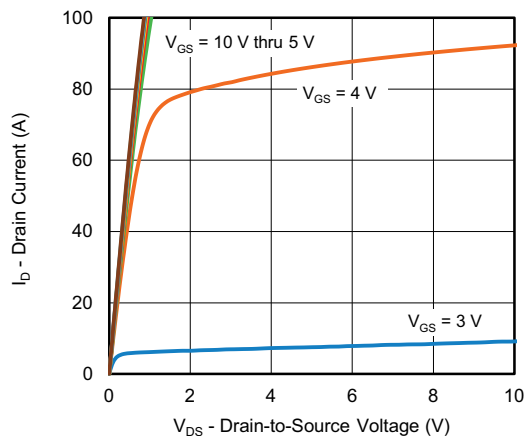
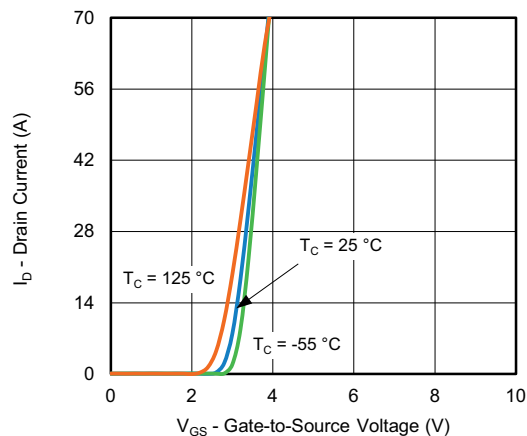
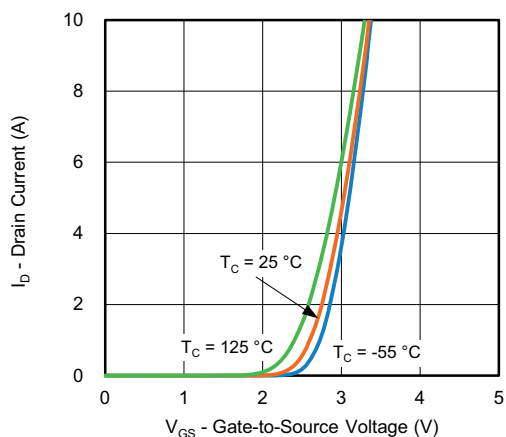
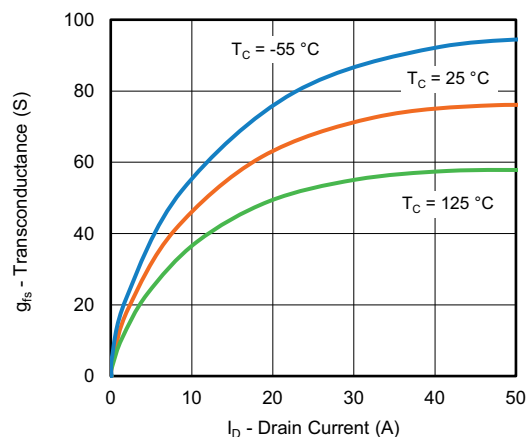
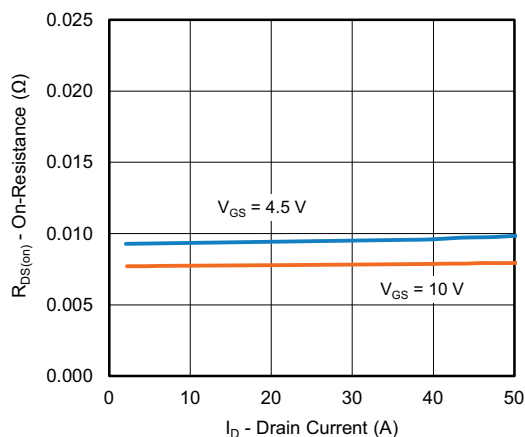
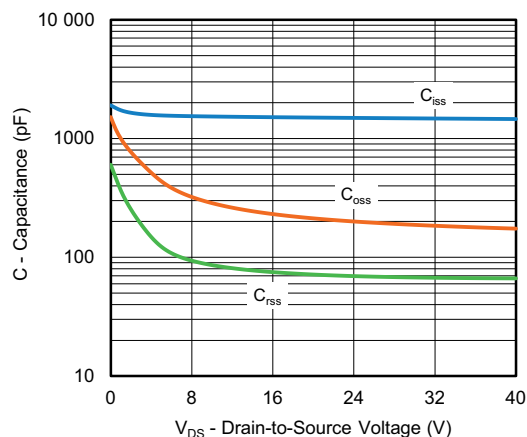
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

CHANNEL-1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)


Normalized Thermal Transient Impedance, Junction-to-Case

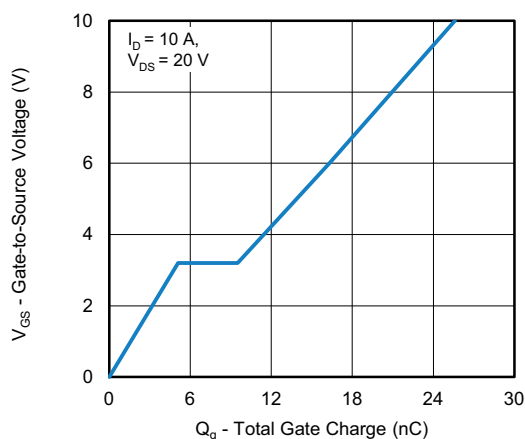
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

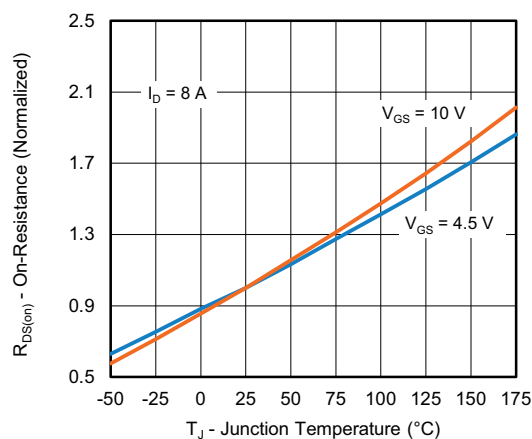
CHANNEL-2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance



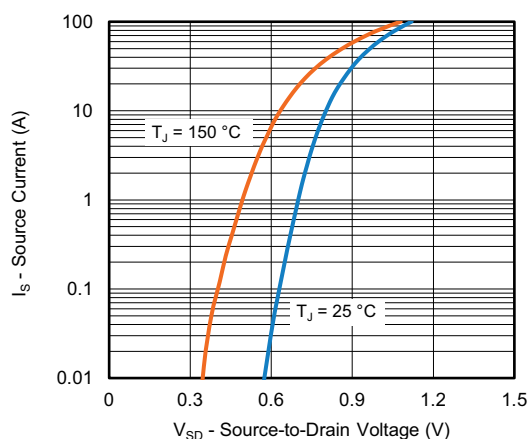
CHANNEL-2 TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



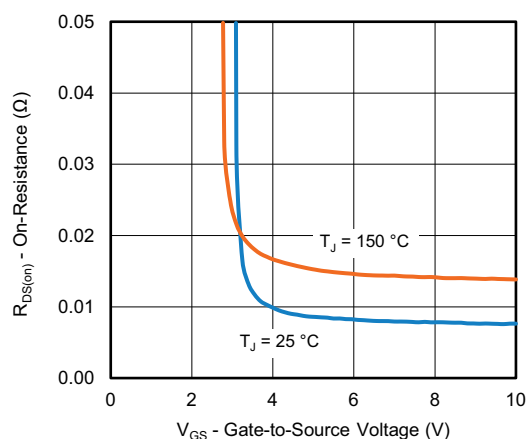
Gate Charge



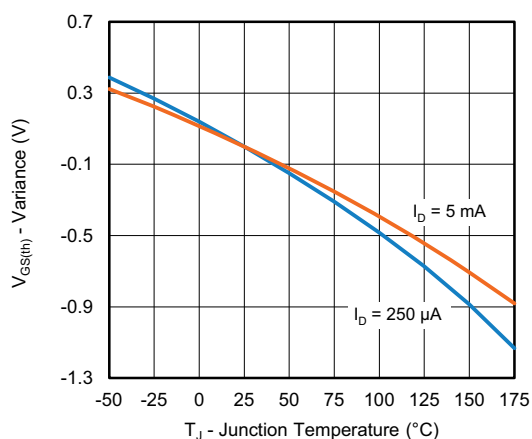
On-Resistance vs. Junction Temperature



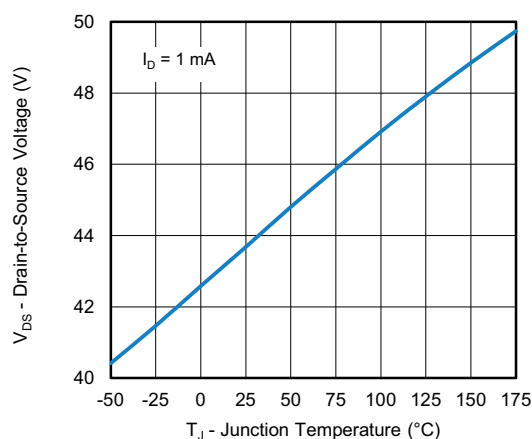
Source Drain Diode Forward Voltage



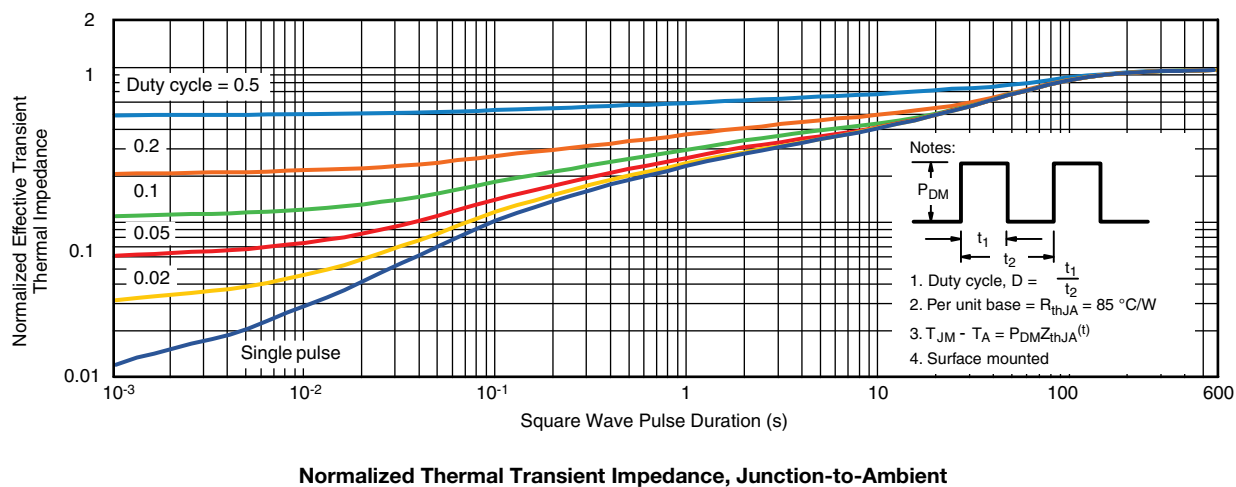
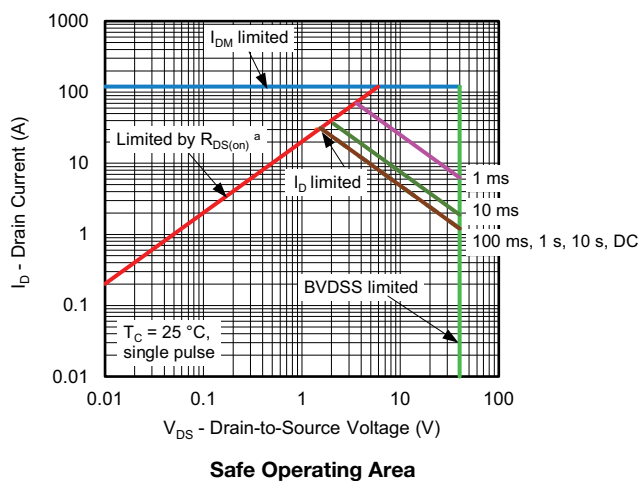
On-Resistance vs. Gate-to-Source Voltage



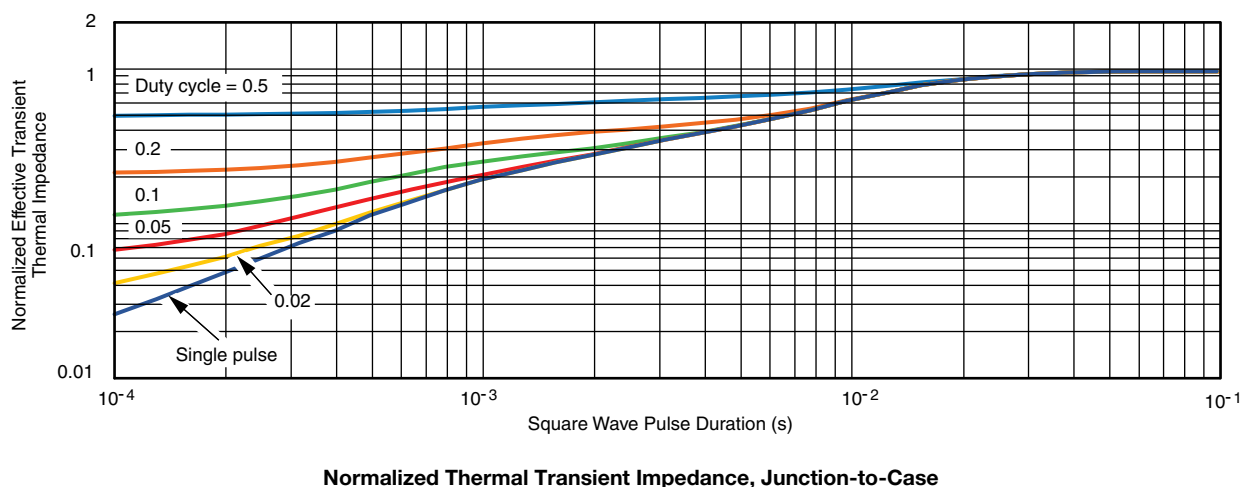
Threshold Voltage



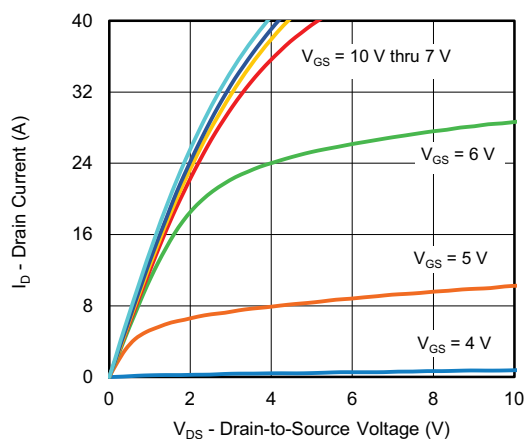
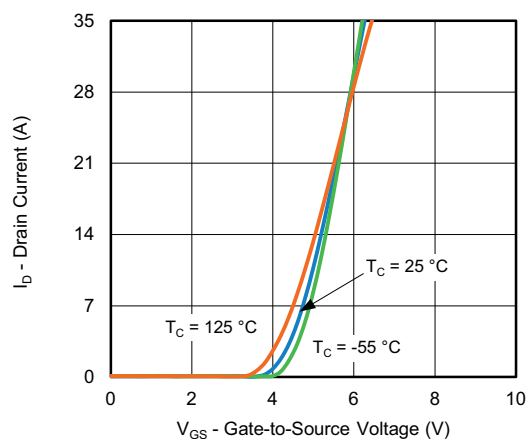
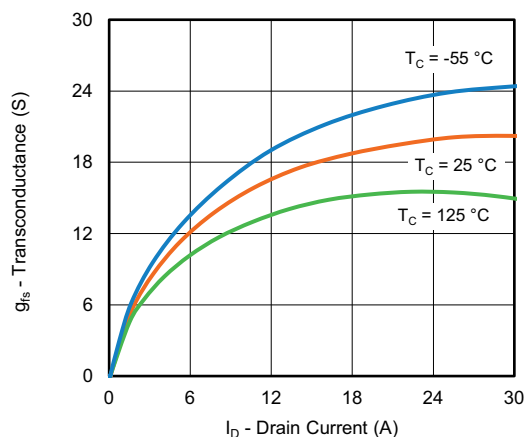
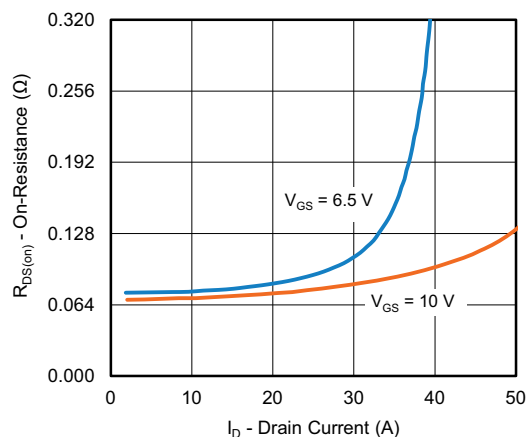
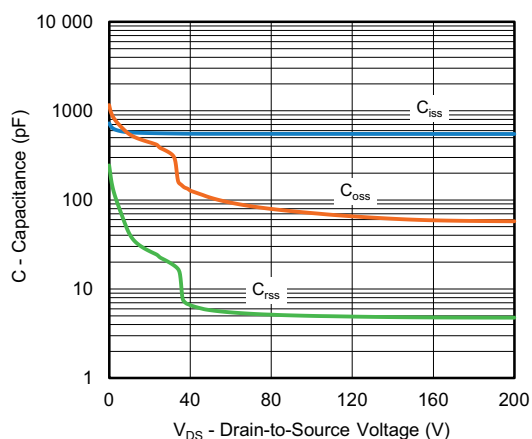
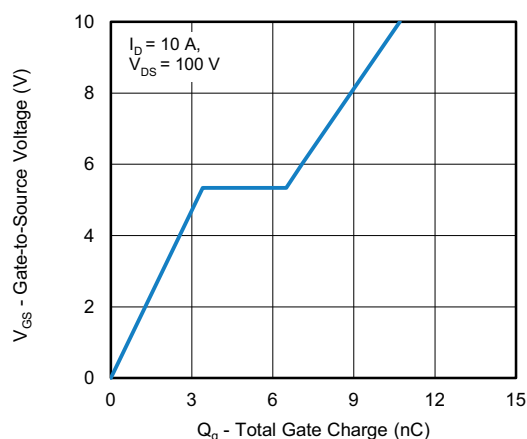
Drain Source Breakdown vs. Junction Temperature

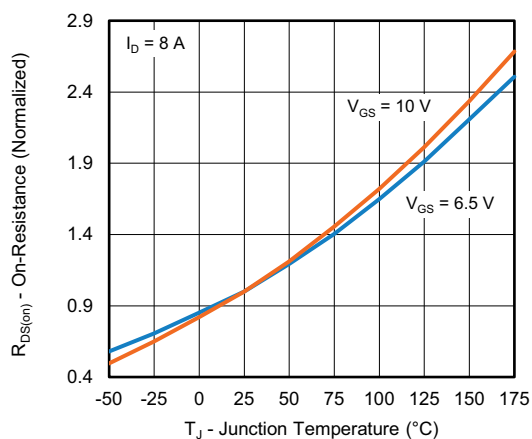
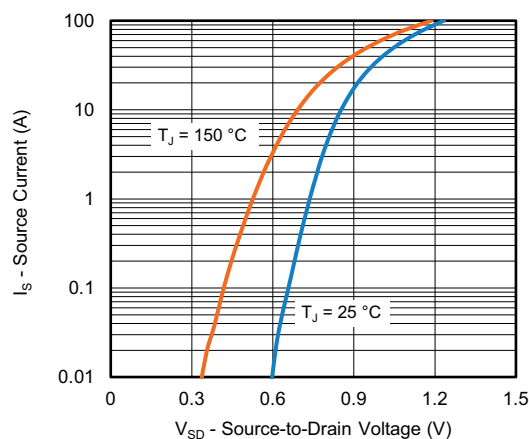
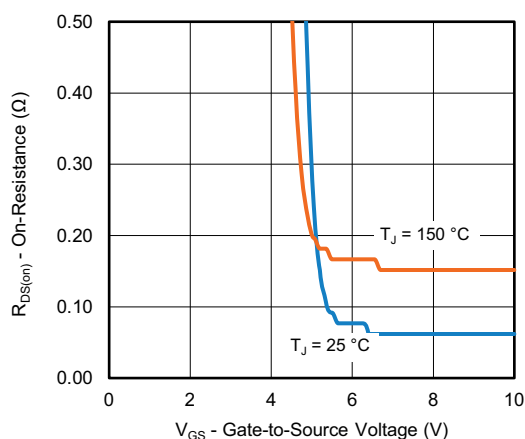
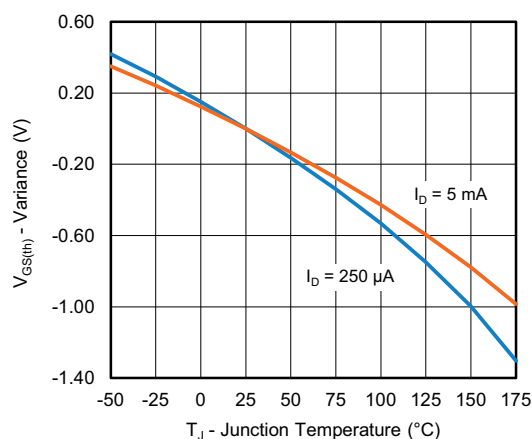
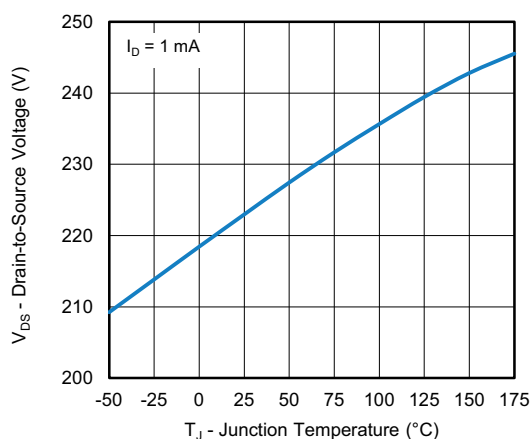
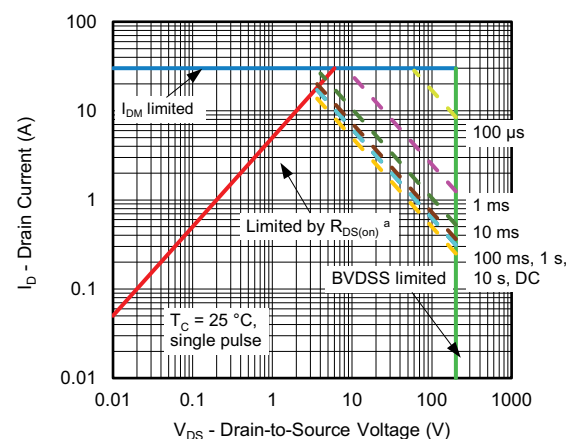
CHANNEL-2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

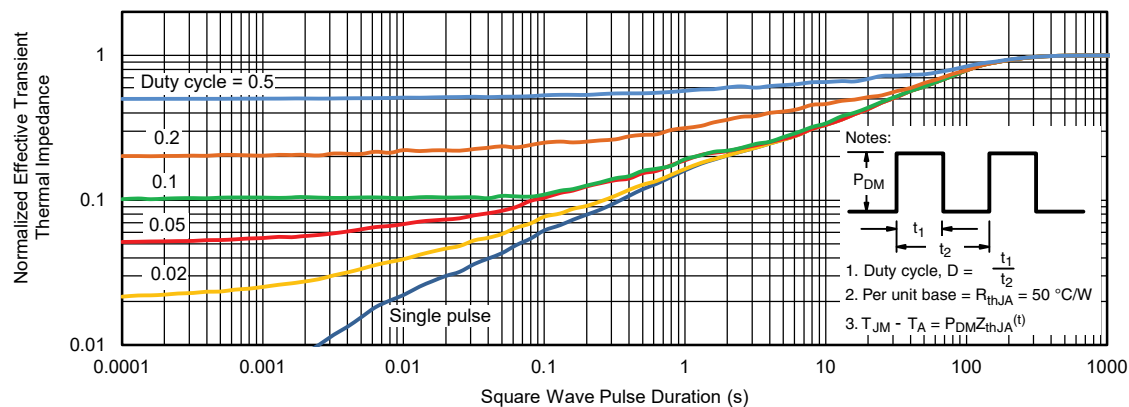
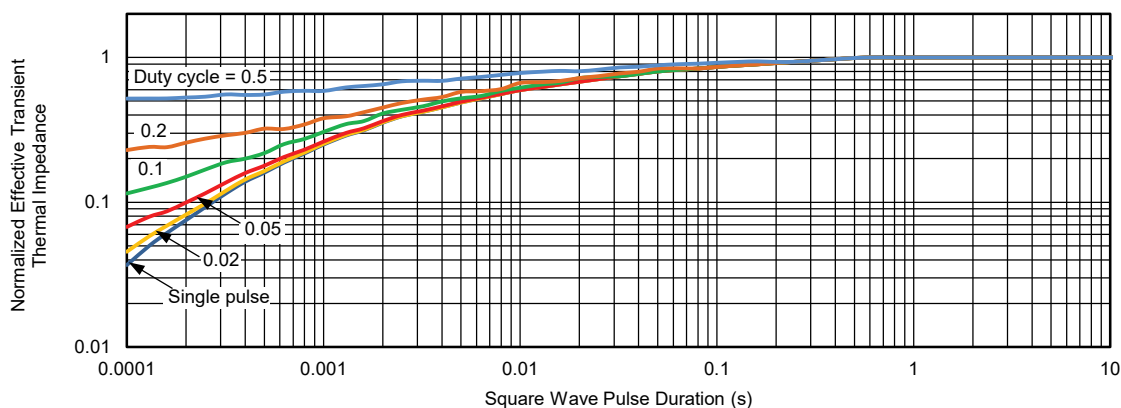
CHANNEL-2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

CHANNEL-3 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

CHANNEL-3 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature

Safe Operating Area
Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

CHANNEL-3 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
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