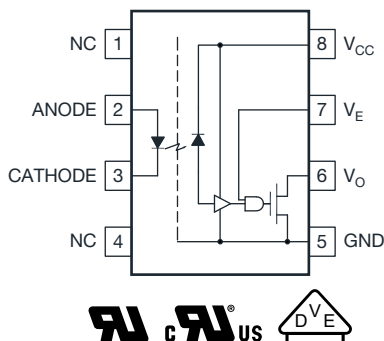
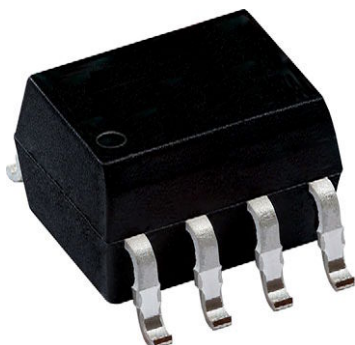


High Speed Optocoupler, 10 MBd



DESCRIPTION

The VOIH060A is a single channel 10 MBd optocoupler utilizing a high efficient input LED coupled to a high speed integrated photo-detector logic gate with a strobable output. This detector features an open drain output. The internal shield provides a guaranteed common mode transient immunity of 15 kV/ μ s.

FEATURES

- CMTI of 15 kV/ μ s (min.)
- 3.3 V / 5 V dual supply voltage
- LVTTL/LVCMOS compatibility
- Low power consumption
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

APPLICATIONS

- Microprocessor system interface
- Ground loop elimination
- Digital bus systems isolation
- High speed A/D and D/A conversion
- Digital control power supply
- Level shifting

AGENCY APPROVALS

- UL1577 (pending)
- cUL (pending)
- [DIN EN 60747-5-5 \(VDE 0884-5\), available with option 1](#)

LINKS TO ADDITIONAL RESOURCES



ORDERING INFORMATION

V	O	I	H	0	6	0	A	-	X	0	#	#	T
PART NUMBER								PACKAGE OPTION				TAPE AND REEL	

AGENCY CERTIFIED / PACKAGE	
UL, cUL	
SOIC-8	VOIH060AT
UL, cUL, VDE (option 1)	
SOIC-8	VOIH060A-X001T

Note

- Additional options may be possible, please contact sales office

**ABSOLUTE MAXIMUM RATINGS** ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
INPUT				
Input forward current		I_F	20	mA
Reverse input voltage		V_R	5	V
Enable input voltage		V_E	$V_{CC} + 0.5\text{ V}$	V
Enable input current		I_E	5	mA
Input power dissipation		P_{diss}	40	mW
OUTPUT				
Supply voltage		V_{CC}	7	V
Output current		I_O	50	mA
Output voltage		V_O	7	V
Output power dissipation		P_{diss}	85	mW
COUPLER				
Storage temperature		T_{stg}	-55 to +125	$^{\circ}\text{C}$
Operating temperature		T_{amb}	-40 to +110	$^{\circ}\text{C}$
Solder reflow temperature ⁽¹⁾	5 s		260	$^{\circ}\text{C}$

Notes

- Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.

⁽¹⁾ Refer to reflow profile for soldering conditions for surface mounted devices (SMD)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Operating temperature	T_{amb}	-40	+110	$^{\circ}\text{C}$
Supply voltage	V_{CC}	2.7	3.6	V
	V_{CC}	4.5	5.5	V
Input current low level	I_{FL}	0	250	μA
Input current high level	I_{FH}	5	15	mA
Logic low enable voltage	V_{EL}	0	0.8	V
Logic high enable voltage	V_{EH}	2	V_{CC}	V
Output pull up resistor	R_L	330	4000	Ω
Fanout ($R_L = 1\text{ k}\Omega$)	N	-	5	TTL loads

TRUTH TABLE (positive logic)

LED	ENABLE	OUTPUT
On	H	L
Off	H	H
On	L	H
Off	L	H
On	Not connected / open	L
Off	Not connected / open	H



ELECTRICAL CHARACTERISTICS ($T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+110\text{ }^{\circ}\text{C}$, $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $I_F = 7.5\text{ mA}$, unless otherwise specified; typical values are at $V_{CC} = 3.3\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
INPUT						
Input forward voltage	$I_F = 10\text{ mA}$	V_F	-	1.38	1.70	V
Input forward voltage temperature coefficient	$I_F = 10\text{ mA}$	$\Delta V_F / \Delta T$	-	-1.5	-	mV/K
Input reverse voltage	$I_R = 10\text{ }\mu\text{A}$	BV_R	5	-	-	V
Input threshold current	$V_E = 2\text{ V}$, $V_O = 0.6\text{ V}$, $V_{CC} = 3.3\text{ V}$, $I_{OL}(\text{sinking}) = 13\text{ mA}$	I_{TH}	-	2	5	mA
Input capacitance	$f = 1\text{ MHz}$, $V_F = 0\text{ V}$	C_I	-	34	-	pF
OUTPUT						
Low level supply current	$I_F = 10\text{ mA}$, $V_{CC} = 3.3\text{ V}$, $V_E = 0.5\text{ V}$	I_{CCL}	-	3.1	5	mA
High level supply current	$I_F = 0\text{ mA}$, $V_{CC} = 3.3\text{ V}$, $V_E = 0.5\text{ V}$	I_{CCH}	-	3.3	5	mA
Low level enable current	$V_{CC} = 3.3\text{ V}$, $V_E = 0.5\text{ V}$	I_{EL}	-	-0.41	-1.6	mA
High level enable current	$V_{CC} = 3.3\text{ V}$, $V_E = 2\text{ V}$	I_{EH}	-	-0.19	-1.6	mA
Low level enable voltage		V_{EL}	-	-	0.8	V
High level enable voltage		V_{EH}	2	-	-	V
Low level output voltage	$V_{CC} = 3.3\text{ V}$, $V_E = 2\text{ V}$, $I_F = 5\text{ mA}$, $I_{OL}(\text{sinking}) = 13\text{ mA}$	V_{OL}	-	0.2	0.6	V
High level output current	$V_{CC} = 3.3\text{ V}$, $V_E = 2\text{ V}$, $V_O = 3.3\text{ V}$, $I_F = 250\text{ }\mu\text{A}$	I_{OH}	-	1	10	μA
COUPLER						
Input to output capacitance	$f = 1\text{ MHz}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$	C_{IO}	-	1	-	pF

Note

- Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

ELECTRICAL CHARACTERISTICS ($T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+110\text{ }^{\circ}\text{C}$, $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $I_F = 7.5\text{ mA}$, unless otherwise specified; typical values are at $V_{CC} = 5.0\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
INPUT						
Input forward voltage	$I_F = 10\text{ mA}$	V_F	-	1.38	1.70	V
Input forward voltage temperature coefficient	$I_F = 10\text{ mA}$	$\Delta V_F / \Delta T$	-	-1.5	-	mV/K
Input reverse voltage	$I_R = 10\text{ }\mu\text{A}$	BV_R	5	-	-	V
Input threshold current	$V_E = 2\text{ V}$, $V_O = 0.6\text{ V}$, $V_{CC} = 5.5\text{ V}$, $I_{OL}(\text{sinking}) = 13\text{ mA}$	I_{TH}	-	2	5	mA
Input capacitance	$f = 1\text{ MHz}$, $V_F = 0\text{ V}$	C_I	-	34	-	pF
OUTPUT						
Low level supply current	$I_F = 10\text{ mA}$, $V_{CC} = 5.5\text{ V}$, $V_E = 0.5\text{ V}$	I_{CCL}	-	3.5	5	mA
High level supply current	$I_F = 0\text{ mA}$, $V_{CC} = 5.5\text{ V}$, $V_E = 0.5\text{ V}$	I_{CCH}	-	3.7	5	mA
Low level enable current	$V_{CC} = 5.5\text{ V}$, $V_E = 0.5\text{ V}$	I_{EL}	-	-0.9	-1.6	mA
High level enable current	$V_{CC} = 5.5\text{ V}$, $V_E = 2\text{ V}$	I_{EH}	-	-0.6	-1.6	mA
Low level enable voltage		V_{EL}	-	-	0.8	V
High level enable voltage		V_{EH}	2	-	-	V
Low level output voltage	$V_{CC} = 5.5\text{ V}$, $V_E = 2\text{ V}$, $I_F = 5\text{ mA}$, $I_{OL}(\text{sinking}) = 13\text{ mA}$	V_{OL}	-	0.20	0.60	V
High level output current	$V_{CC} = 5.5\text{ V}$, $V_E = 2\text{ V}$, $V_O = 5.5\text{ V}$, $I_F = 250\text{ }\mu\text{A}$	I_{OH}	-	1	10	μA
COUPLER						
Input to output capacitance	$f = 1\text{ MHz}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$	C_{IO}	-	1	-	pF

Note

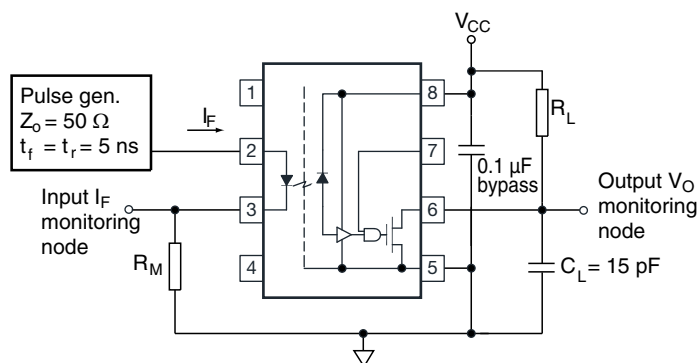
- Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

SWITCHING CHARACTERISTICS ($T_{amb} = -40^{\circ}\text{C}$ to $+110^{\circ}\text{C}$, $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $I_F = 7.5\text{ mA}$, unless otherwise specified; typical values are at $V_{CC} = 3.3\text{ V}$, $T_{amb} = 25^{\circ}\text{C}$)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to high output level	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$	t_{PLH}	25	50	90	ns
Propagation delay time to low output level	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$	t_{PHL}	25	44	75	ns
Pulse width distortion	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$	$ t_{PLH} - t_{PHL} $	-	6	-	ns
Propagation delay skew	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$	t_{PSK}	-	-	40	ns
Output rise time (10 % to 90 %)	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$	t_r	-	11	-	ns
Output fall time (90 % to 10 %)	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$	t_f	-	2.3	-	ns
Propagation delay time of enable from V_{EH} to V_{EL}	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$, $V_{EL} = 0\text{ V}$, $V_{EH} = 3\text{ V}$	t_{ELH}	-	15	-	ns
Propagation delay time of enable from V_{EL} to V_{EH}	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$, $V_{EL} = 0\text{ V}$, $V_{EH} = 3\text{ V}$	t_{EHL}	-	15	-	ns

SWITCHING CHARACTERISTICS ($T_{amb} = -40^{\circ}\text{C}$ to $+110^{\circ}\text{C}$, $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $I_F = 7.5\text{ mA}$, unless otherwise specified; typical values are at $V_{CC} = 5.0\text{ V}$, $T_{amb} = 25^{\circ}\text{C}$)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to high output level	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$, $T_{amb} = 25^{\circ}\text{C}$	t_{PLH}	25	50	90	ns
	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$	t_{PLH}	-	-	100	ns
Propagation delay time to low output level	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$, $T_{amb} = 25^{\circ}\text{C}$	t_{PHL}	25	40	75	ns
	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$	t_{PHL}	-	-	100	ns
Pulse width distortion	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$	$ t_{PLH} - t_{PHL} $	-	10	-	ns
Propagation delay skew	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$	t_{PSK}	-	-	40	ns
Output rise time (10 % to 90 %)	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$	t_r	-	11	-	ns
Output fall time (90 % to 10 %)	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$	t_f	-	2.3	-	ns
Propagation delay time of enable from V_{EH} to V_{EL}	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$, $V_{EL} = 0\text{ V}$, $V_{EH} = 3\text{ V}$	t_{ELH}	-	15	-	ns
Propagation delay time of enable from V_{EL} to V_{EH}	$R_L = 350\ \Omega$, $C_L = 15\text{ pF}$, $V_{EL} = 0\text{ V}$, $V_{EH} = 3\text{ V}$	t_{EHL}	-	15	-	ns



The probe and jig capacitances are included in C_L

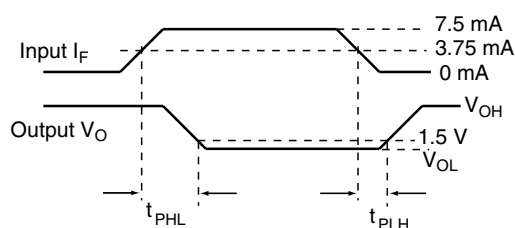
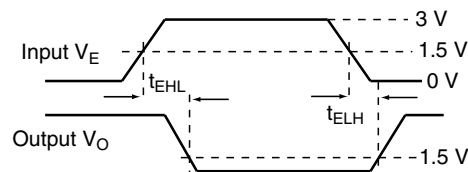
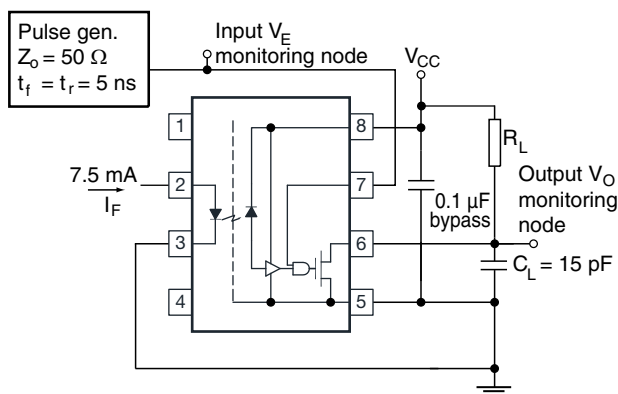


Fig. 1 - Test Circuit for t_{PLH} , t_{PHL} , t_r , and t_f

18964-7



The probe and Jig capacitances are included in C_L

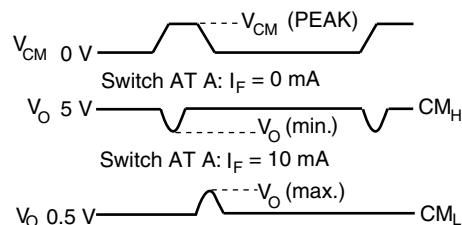
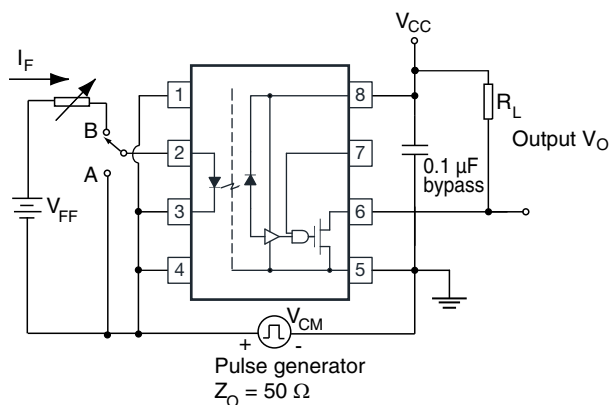
18975-5

Fig. 2 - Test Circuit for t_{EHL} and t_{ELH}

COMMON MODE TRANSIENT IMMUNITY ($T_{amb} = 25^\circ\text{C}$, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Logic high common mode transient immunity	$V_{CC} = 3.3\text{ V}$, $ V_{CM} = 1000\text{ V}$, $I_F = 0\text{ mA}$, $V_O > 2.0\text{ V}$, $R_L = 350\ \Omega$	$ CM_H $	15 000	-	-	V/ μs
	$V_{CC} = 5\text{ V}$, $ V_{CM} = 1000\text{ V}$, $I_F = 0\text{ mA}$, $V_O > 2.0\text{ V}$, $R_L = 350\ \Omega$	$ CM_H $	15 000	-	-	V/ μs
Logic low common mode transient immunity	$V_{CC} = 5\text{ V}$, $ V_{CM} = 1000\text{ V}$, $I_F = 10\text{ mA}$, $V_O < 0.8\text{ V}$, $R_L = 350\ \Omega$	$ CM_L $	15 000	-	-	V/ μs
	$V_{CC} = 5\text{ V}$, $ V_{CM} = 1000\text{ V}$, $I_F = 10\text{ mA}$, $V_O < 0.8\text{ V}$, $R_L = 350\ \Omega$	$ CM_L $	15 000	-	-	V/ μs

Notes

- No external pull up is required for a high logic state on the enable input. If the enable pin is not used, connect it to V_{CC} .



18976-8

Fig. 3 - Test Circuit for Common Mode Transient Immunity

SAFETY AND INSULATION RATINGS

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Climatic classification	According to IEC 68 part 1		40 / 100 / 21	
Pollution degree	According to DIN VDE 0109		2	
Comparative tracking index	Insulation group IIIa	CTI	175	
Maximum rated withstanding isolation voltage	According to UL1577, t = 1 min	V_{ISO}	3750	V_{RMS}
Maximum transient isolation voltage	According to DIN EN 60747-5-5	V_{IOTM}	6000	V_{peak}
Maximum repetitive peak isolation voltage	According to DIN EN 60747-5-5	V_{IORM}	567	V_{peak}
Isolation resistance	$T_{amb} = 25^{\circ}C$, $V_{IO} = 500 V$	R_{IO}	$\geq 10^{12}$	Ω
Maximum output power dissipation		P_{SO}	85	mW
Maximum input current		I_{SI}	50	mA
Maximum ambient temperature (derated)		T_S	175	$^{\circ}C$
Creepage distance			≥ 5	mm
Clearance distance			≥ 5	mm
Insulation thickness		DTI	≥ 0.4	mm

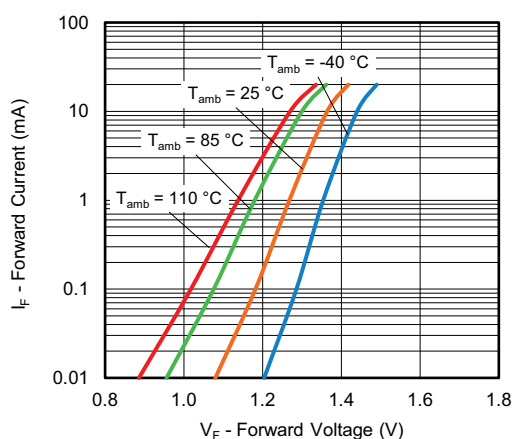
TYPICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}C$, unless otherwise specified)


Fig. 4 - Diode Forward Current vs. Forward Voltage

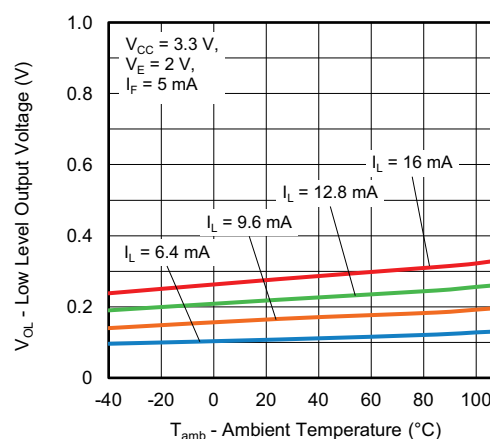


Fig. 6 - Low Level Output Voltage vs. Ambient Temperature

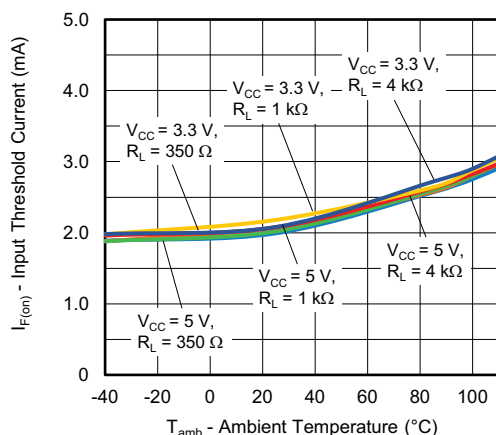


Fig. 5 - Input Threshold Current vs. Ambient Temperature

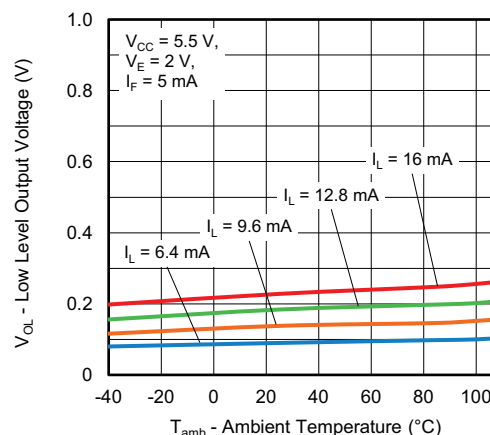


Fig. 7 - Low Level Output Voltage vs. Ambient Temperature

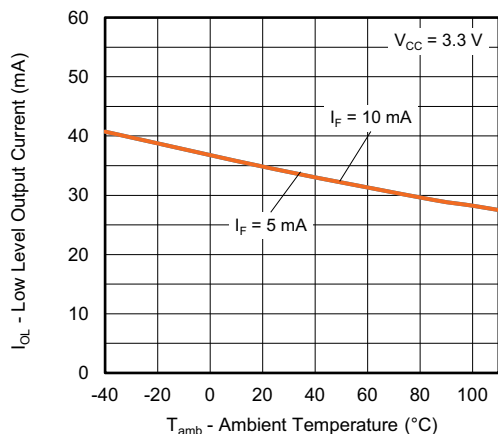


Fig. 8 - Low Level Output Current vs. Ambient Temperature

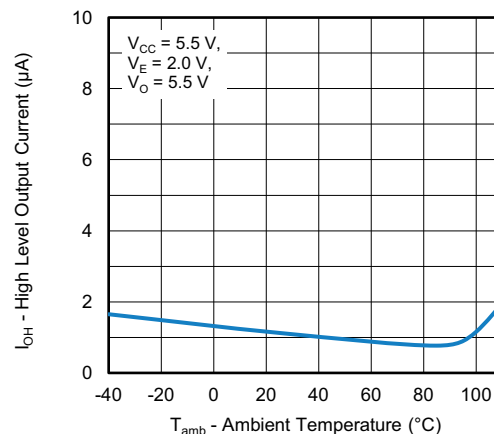


Fig. 11 - High Level Output Current vs. Ambient Temperature

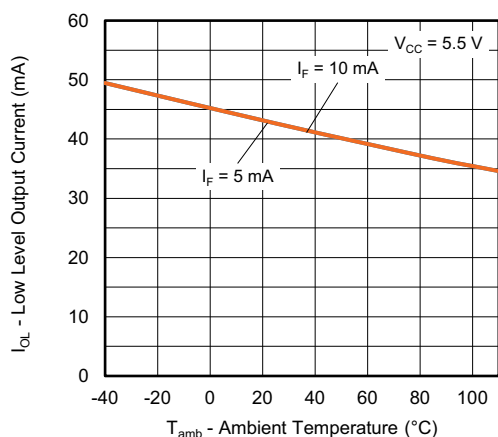


Fig. 9 - Low Level Output Current vs. Ambient Temperature

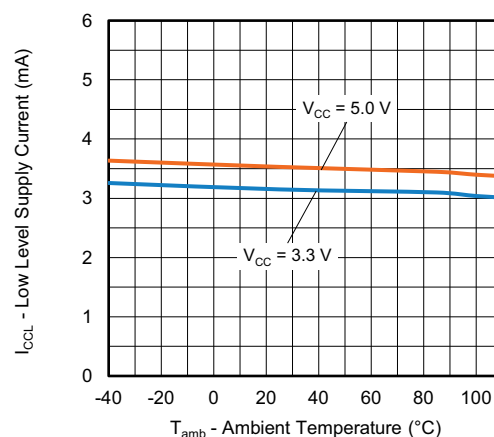


Fig. 12 - Low Level Supply Current vs. Ambient Temperature

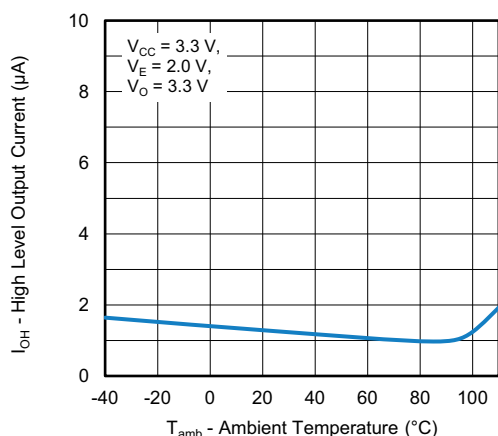


Fig. 10 - High Level Output Current vs. Ambient Temperature

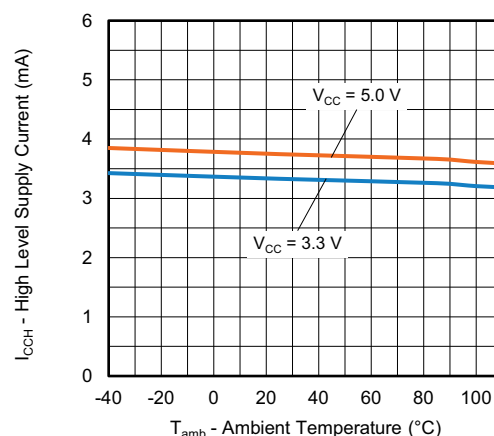


Fig. 13 - High Level Supply Current vs. Ambient Temperature

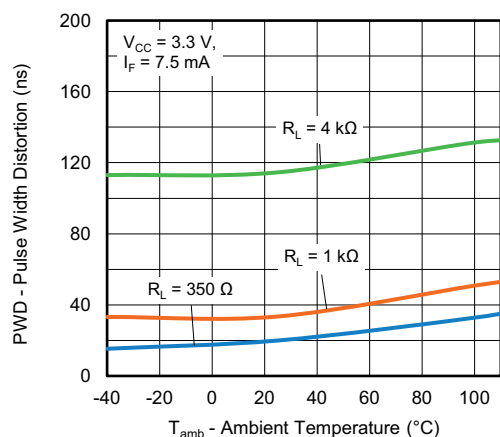


Fig. 14 - Pulse Width Distortion vs. Ambient Temperature

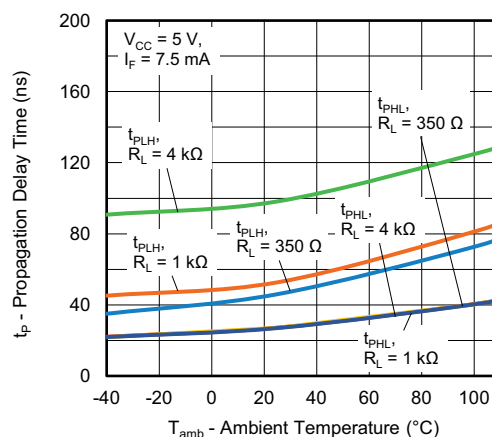


Fig. 17 - Propagation Delay Time vs. Ambient Temperature

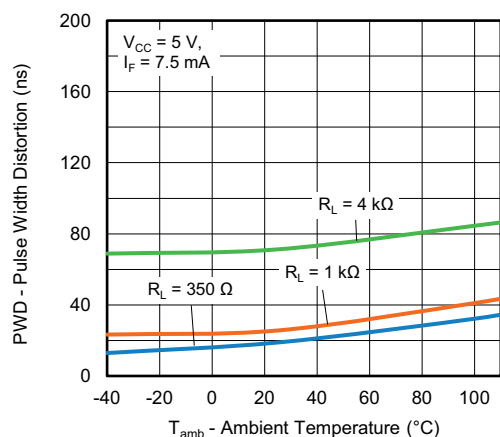


Fig. 15 - Pulse Width Distortion vs. Ambient Temperature

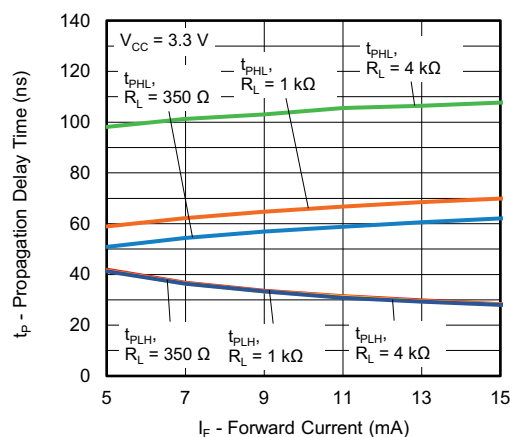


Fig. 18 - Propagation Delay Time vs. Forward Current

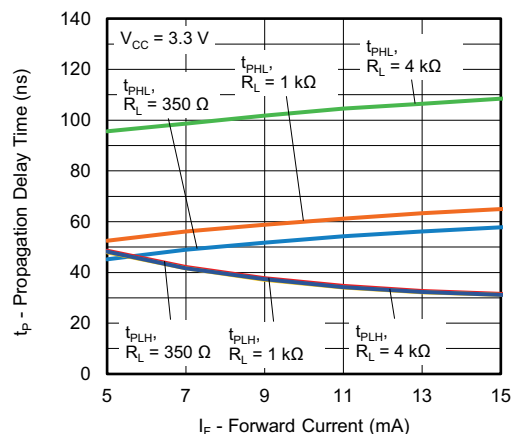


Fig. 16 - Propagation Delay Time vs. Ambient Temperature

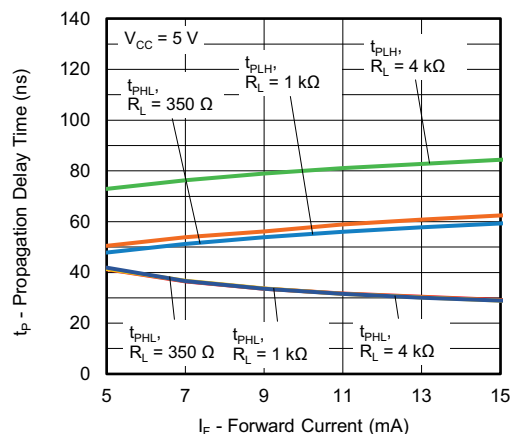


Fig. 19 - Propagation Delay Time vs. Forward Current

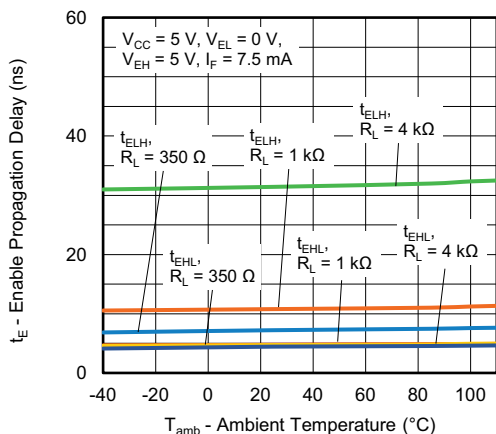


Fig. 20 - Enable Propagation Delay vs. Ambient Temperature

PACKAGE DIMENSIONS (in millimeters)

SOIC-8

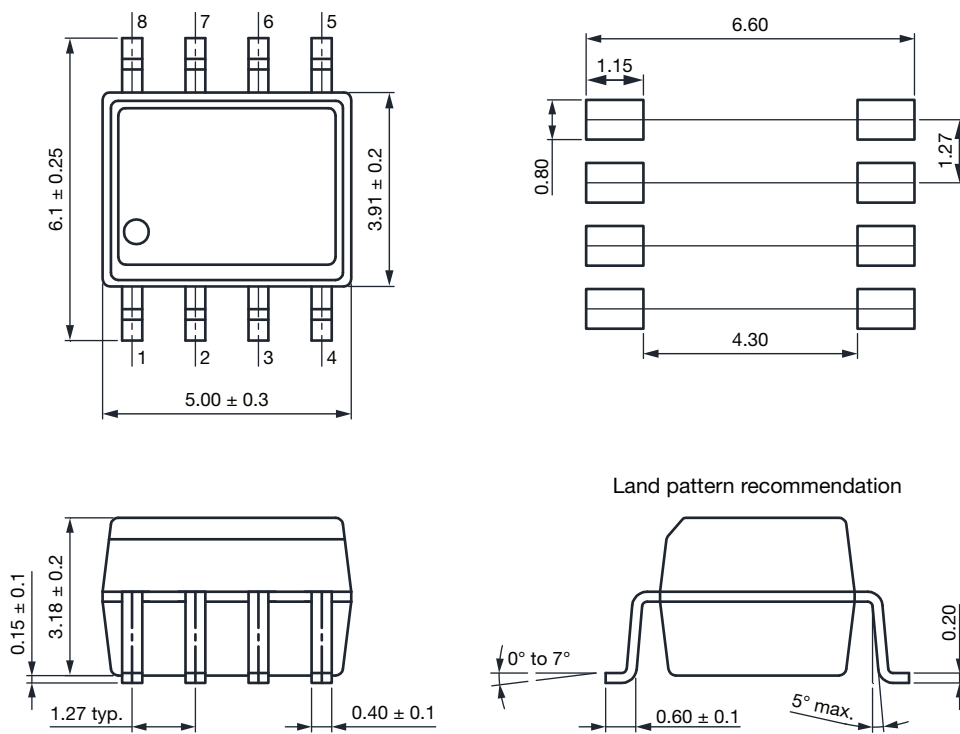


Fig. 21

PACKAGE MARKING

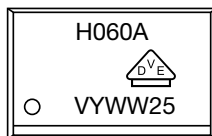


Fig. 22 - Example of VOIH060A-X001T

Notes

- “YWW” is the date code marking (Y = year code, WW = week code)
- The VDE symbol is only marked on VDE option parts
- Tape and reel suffix (T) is not part of the package marking

PACKAGING INFORMATION (in millimeters)

SOIC-8 Tape

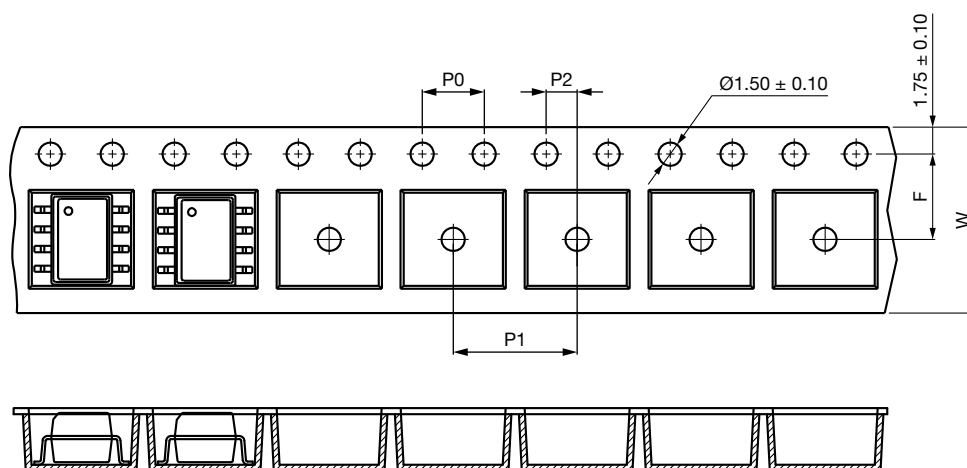


Fig. 23 - Tape and Reel Packaging (2000 pieces on reel)

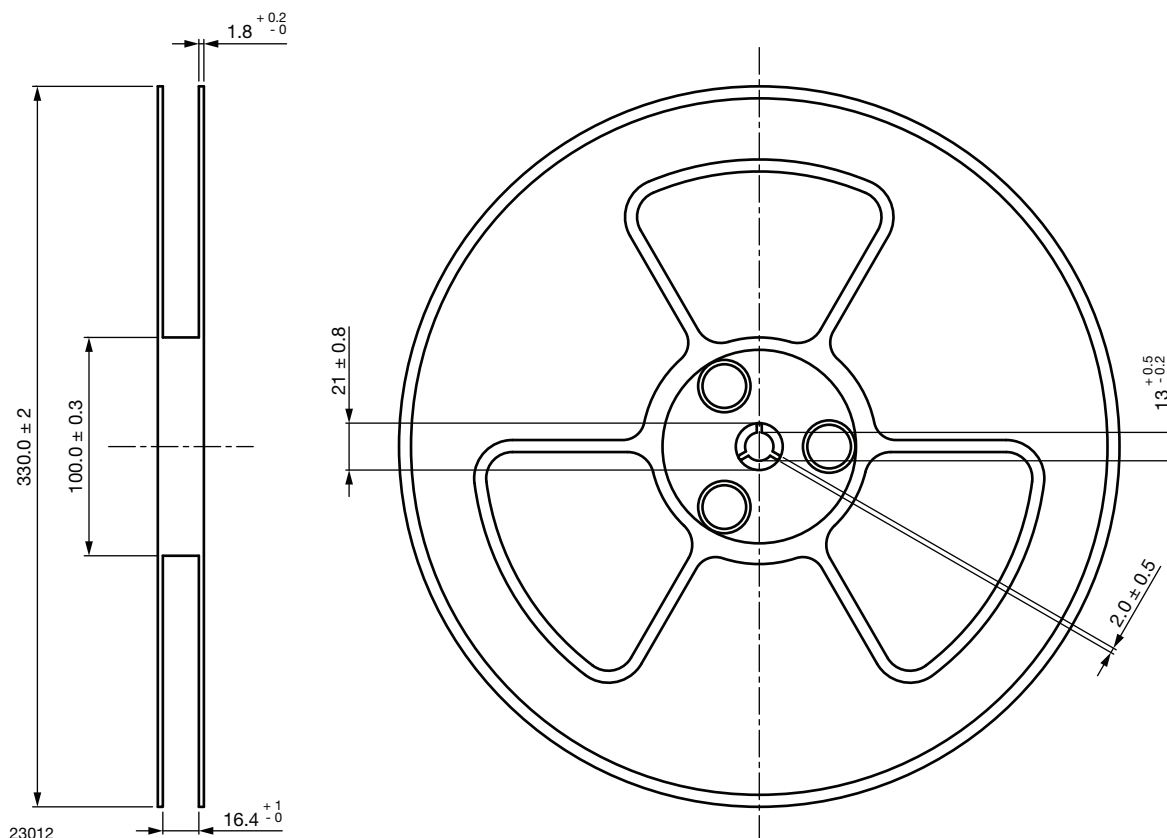
Reel


Fig. 24 - Tape and Reel Shipping Medium

SOLDER PROFILES

IR Reflow Soldering (JEDEC® J-STD-020C compliant)

One time soldering reflow is recommended within the condition of temperature and time profile shown below. Do not solder more than three times.

PROFILE ITEM	CONDITIONS
Preheat	
- Temperature minimum ($T_{S \text{ min.}}$)	150 °C
- Temperature maximum ($T_{S \text{ max.}}$)	200 °C
- Time (min. to max.) (t_S)	90 s $\pm$ 30 s
Soldering zone	
- Temperature (T_L)	217 °C
- Time (t_L)	60 s
Peak temperature (T_p)	260 °C
Ramp-up rate	3 °C/s max.
Ramp-down rate	3 °C/s to 6 °C/s

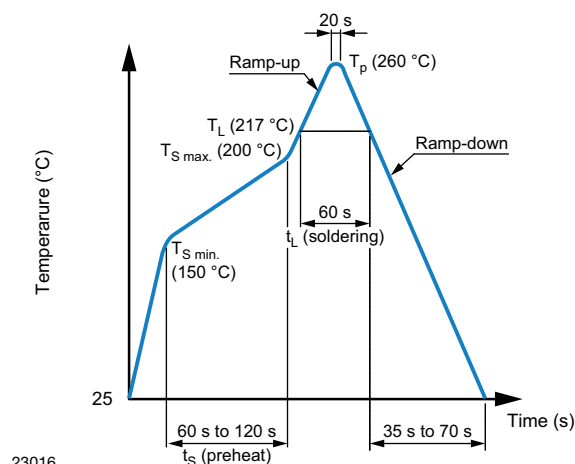


Fig. 25

Wave Soldering (JEDEC JESD22-A111 compliant)

One time soldering is recommended within the condition of temperature.

Temperature: 260 °C + 0 °C / - 5 °C

Time: 10 s

Preheat temperature: 25 °C to 140 °C

Preheat time: 30 s to 80 s

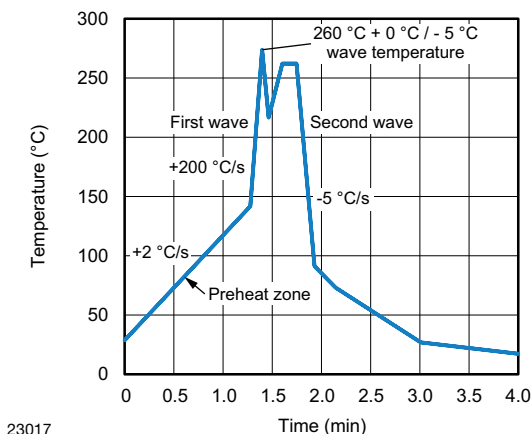


Fig. 26

Hand Soldering by Soldering Iron

Allow single lead soldering in every single process. One time soldering is recommended.

Temperature: 380 °C + 0 °C / - 5 °C

Time: 3 s max.

HANDLING AND STORAGE CONDITIONS

ESD level: HBM class 2

Floor life: unlimited

Conditions: $T_{\text{amb}} < 30 \text{ °C}$, RH < 85 %

Moisture sensitivity level 1, according to J-STD-020



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