



# Solid-State Relays Current Limit Performance

## DESCRIPTION

Most Vishay form A solid-state relays (SSRs) have built-in, active, current-limit circuitry. This feature protects not only SSRs, but can also protect the circuitry beyond the SSRs from fault conditions. These SSRs limit current through the device at a prescribed value. Current-limit trip and reset is automatic, smooth, fast, and precise.

Refer to figure 1. In operation, current through the input LED produces light for the photodiode array (PDA). The PDA develops a voltage that is directly applied to the gates of the MOSFET switches. If excessive current flows through the MOSFETs, the current-limiting circuitry activates and pulls down on the PDA, robbing current and dropping the voltage available for the gates of the MOSFET switches. Lower gate voltage increases switch resistance and thereby limits the current through the switches.

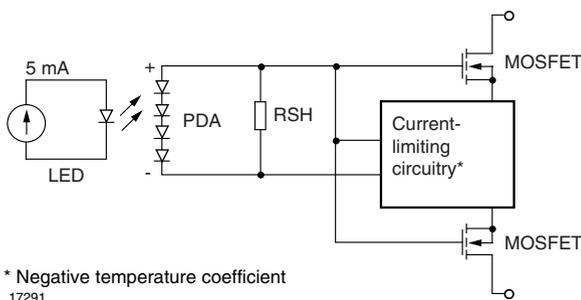


Fig. 1 - Current-Limit SSR Schematic

The current-limit circuit has a negative temperature coefficient, thereby limiting power dissipation to safe levels during extended high on-voltage conditions. When the excessive current is removed, the SSR immediately resumes normal operation.

How an SSR performs in current limiting depends on how it is driven into current limiting. A DC current allows the SSR to gradually heat up, slowly decreasing the current limit value which minimizes SSR power dissipation.

## RELAY PROTECTION

For the SSRs to withstand transients, some form of voltage-limit protection is required. The voltage protection also limits the voltage below the SSR's maximum load voltage when the SSR is in the off-state.

## CURRENT-LIMIT PERFORMANCE DURING FAST TRANSIENTS OR LIGHTNING

When a transient occurs and the SSR is off, the voltage across the poles of the SSR rises to the trip voltage of the protection device being used. The SSR remains off without leaking current.

When a transient occurs and the SSR is on, current through the SSR reacts as follows:

First, the SSR exhibits a time delay before current limiting trips. The time required to trip depends on the current through the SSR. The amount of current conducted during this initial rise and the current-limit trip time is dependent upon the specific SSR, the rise time of the fault, and the series resistance in the conduction path between the transient voltage and the SSR. Currents range from 0.5 A to 4 A and trip times from 200 ns to 10  $\mu$ s, for an 800 V, 10 x 560  $\mu$ s impulse waveform.

Next, current limiting trips and the SSR turns off. The voltage rises to an amplitude bounded by the protection device across the SSR. The SSR remains in this state for the duration of the SSR's specified turn-on time.

Lastly, the SSR turns back on and limits the transient current to the SSR's specified current-limit value. In current limiting, the SSR presents a high impedance to the fault. The SSR can dissipate a substantial amount of power while in this state. However, SSR characteristics and the protection device both assist in limiting the power dissipation of the SSR. The SSR's current-limit circuit exhibits a negative temperature coefficient.

As the SSR heats up from current limiting, its impedance increases, reducing current flow through the SSR, thereby reducing its power dissipation.

If a crowbar protection device is used, it will have already shunted current flow (assuming the transient was of sufficient potential to break over the crowbar device), thereby relieving the SSR from any power dissipation during this state. If an MOV protection device is used, it sets the maximum voltage that is imposed on the SSR and shunts some of the current around the SSR when its zener voltage is exceeded. The SSR remains in this state until the transient subsides. At this time, the SSR immediately resumes its normal operating characteristics.

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### CURRENT-LIMIT PERFORMANCE DURING POWER CROSS

Power cross is an AC fault condition where 50 Hz/60 Hz power waves are induced on telephone lines. This condition can produce a fault as high as 600 V<sub>RMS</sub> and 40 A, as specified in UL1459 50 A. The primary design criteria for components exposed to power-cross over-voltage conditions is that they must not present a risk of fire. The mold compound used in the construction of the LH1500 series of SSRs carries a stringent flammability rating of UL94 V-0.

Depending on the applications circuitry, the protection components, and the extent of the power-cross fault, the SSRs can survive some power-cross stresses. Refer to figure 2 for the acceptable operating region of the Vishay SSRs under transient conditions.

If an MOV that clamps over voltages to a specified value is used to limit voltage across an SSR, the MOV voltage should be limited to 125 V to 175 V in order for the SSRs to survive power-cross stress.

A desirable feature of the current-limited SSRs is the tendency of the SSR to thermally shut down under high power and extreme temperature. The SSRs will actually shut down at T<sub>J</sub> above 150 °C if LED drive currents are kept relatively low. At high temperatures, both the LED light output diminishes and the photodiode array output current decreases, lowering MOSFET switch gate voltage to below threshold and turning the SSR off. The SSR turns back on when the temperature subsides.

### SSR WITHOUT CURRENT LIMIT

1. An SSR draws substantial current due to application of an impulse waveform. The current is limited only by any series and load resistance in the circuit and the on-resistance of the SSR itself
2. The SSR is overcome by localized heating due to severe power dissipation and goes into secondary breakdown
3. In secondary breakdown, the SSR draws excessive current until the fault subsides

### VISHAY SSR WITH CURRENT LIMIT

1. The current-limit SSR draws a short pulse of current, indistinguishable on this millisecond scale
2. The current-limit SSR turns itself off during the worst part of the impulse wave dissipating no power
3. The current-limit SSR turns itself back on into current limiting and remains in current limit until the fault subsides

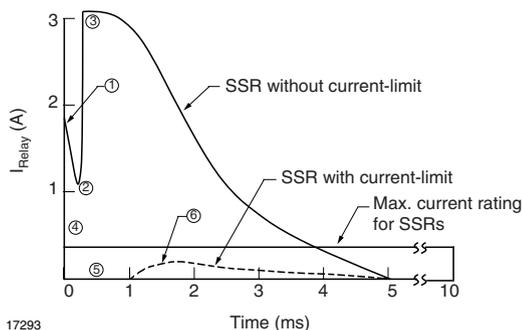
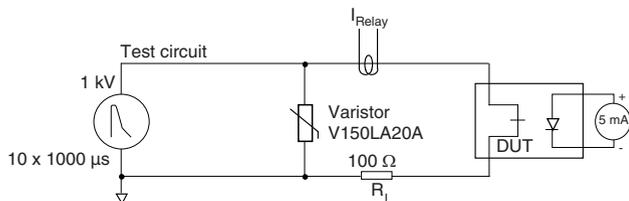


Fig. 2 - Anatomy of a Current-Limit SSR During Lightning