

## VCUT10A1-SD0

RoHS

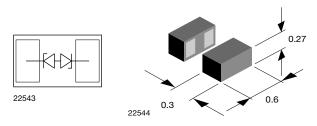
COMPLIANT

HALOGEN FREE

**GREEN** 

Vishay Semiconductors

# Bidirectional Symmetrical (BiSy) Single Line ESD-Protection Diode in Silicon Package



#### **MARKING** (example only)



1 = year code Open circle = month code and pin 1 XY = type code

#### **DESIGN SUPPORT TOOLS AVAILABLE**



#### **FEATURES**

- Ultra compact CLP0603-2L package
- Low package height < 0.3 mm
- 1-line ESD-protection
- Working range ± 10 V
- Low leakage current < 0.1 μA
- Low load capacitance C<sub>D</sub> = 7.7 pF (typ.)
- ESD-protection acc. IEC 61000-4-2
   ± 24 kV contact discharge
   ± 24 kV air discharge
- Lead plating: Au (e4)
- Lead material: Ni
- Topside coating
- e4 precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912">www.vishav.com/doc?99912</a>



PACKAGE DATA							
DEVICE NAME PACKAGE NAME		TYPE CODE	WEIGHT	SOLDERING CONDITIONS			
VCUT10A1-SD0	CLP0603-2L	10	0.12 mg	Peak temperature max. 260 °C Reflow soldering according JEDEC® STD-020			

ABSOLUTE MAXIMUM RATINGS						
PARAMETER	TEST CONDITIONS SYMBOL		VALUE	UNIT		
Peak pulse current	acc. IEC 61000-4-5, 8/20 µs/single shot	I <sub>PPM</sub>	4	Α		
Peak pulse power	Pin 1 to pin 2 acc. IEC 61000-4-5; $t_p$ = 8/20 $\mu$ s; single shot	P <sub>PP</sub>	72	W		
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V	± 24	197		
	Air discharge acc. IEC 61000-4-2; 10 pulses	- V <sub>ESD</sub>	± 24	kV		
Operating temperature	Junction temperature	T <sub>J</sub>	-55 to +150	°C		
Storage temperature		T <sub>stg</sub>	-55 to +150	°C		

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1 Document Number: 85937
For technical questions, contact: ESDprotection@vishav.com



# VCUT10A1-SD0

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#### **CUT THE SPIKES WITH VCUT10A1-SD0**

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The VCUT10A1-SD0 is a Bidirectional and Symmetrical (BiSy) ESD-protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VCUT10A1-SD0 offers a high isolation (low leakage current, low capacitance) within the specified working range. Due to the short leads and small package size of the tiny CLP0603-2L package the line inductance is very low, so that fast transients like and ESD-strike can be clamped with minimal over- or undershoots.

<b>ELECTRICAL CHARACTERISTICS</b> (T <sub>amb</sub> = 25 °C, unless otherwise specified)							
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Protection paths	Number of lines which can be protected	N <sub>channel</sub>	-	-	1	lines	
Reverse stand-off voltage	Max. reverse working voltage	V <sub>RWM</sub>	-	-	10	V	
Reverse voltage	at I <sub>R</sub> = 0.1 μA	$V_R$	10	-	-	V	
Reverse current	at V <sub>RWM</sub> = 10 V	I <sub>R</sub>	-	-	50	nA	
Reverse breakdown voltage	at I <sub>R</sub> = 1 mA	$V_{BR}$	11	12	13	V	
Devenue elemente e veltare	at I <sub>PP</sub> = 1 A; t <sub>p</sub> = 8/20 μs	V <sub>C</sub>	-	13	15	V	
Reverse clamping voltage	at I <sub>PP</sub> = I <sub>PPM</sub> = 4 A; t <sub>p</sub> = 8/20 μs	V <sub>C</sub>	-	16	18	V	
0	at V <sub>R</sub> = 0 V; f = 1 MHz	C <sub>D</sub>	-	7.7	9	pF	
Capacitance	at V <sub>R</sub> = 5 V; f = 1 MHz	C <sub>D</sub>	-	5.4	-	pF	
Clamping voltage Transmission Line Pulse (TLP); $t_p = 100$ $I_{TLP} = 8 \text{ A}$		V <sub>C-TLP</sub>	-	15.3	-	V	
Clamping voltage	Clamping voltage Transmission Line Pulse (TLP); $t_p = 100 \text{ ns}$ $I_{TLP} = 16 \text{ A}$		-	17.4	-	V	
Dynamic resistance	Transmission Line Pulse (TLP); t <sub>p</sub> = 100 ns	R <sub>DYN</sub>	-	0.29	-	Ω	

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## **TYPICAL CHARACTERISTICS** (T<sub>amb</sub> = 25 °C, unless otherwise specified)

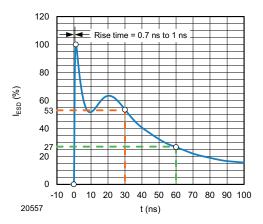


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

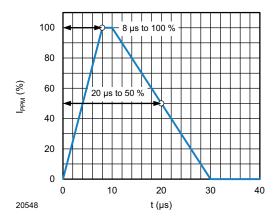


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

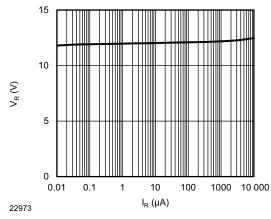


Fig. 3 - Typical Reverse Voltage vs. Reverse Current

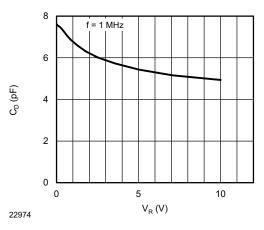


Fig. 4 - Typical Capacitance vs. Reverse Voltage

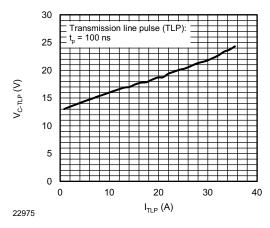


Fig. 5 - Typical Clamping Voltage vs. Peak Pulse Current

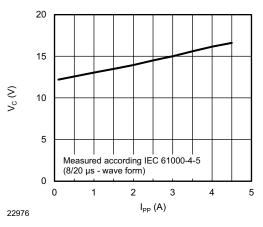


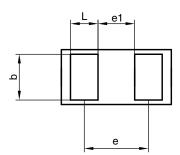
Fig. 6 - Typical Peak Clamping Voltage vs. Peak Pulse Current



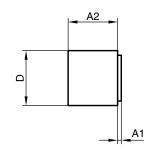
# VCUT10A1-SD0

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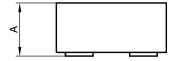
### PACKAGE DIMENSIONS in millimeters (mils): CLP0603-2L

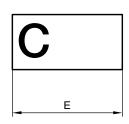


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Package = chip dimensions in mm [mils]





	Millimeters			mils			
	min.	nom.	max.	min.	nom.	max.	
Α	0.25	0.28	0.30	9.84	11.02	11.81	
A1	0.01	0.01	0.02	0.39	0.39	0.79	
A2	0.24	0.27	0.28	9.45	10.63	11.02	
b	0.22	0.25	0.28	8.66	9.84	11.02	
D	0.27	0.30	0.33	10.62	11.81	12.99	
E	0.57	0.60	0.63	22.44	23.62	24.80	
е		0.40			15.75		
e1		0.25			9.84		
L	0.12	0.15	0.18	4.72	5.91	7.09	

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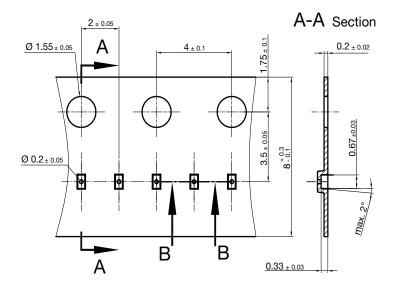
2 terminal leadless package (CLP) Document no.: S8-V-3906.04-023 (4) Created - Date: 22. Nov. 2010 Rev.8 - Date: 11. Nov. 2016

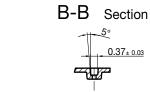
#### Footprint and soldering recommendation:

please see Application Note: www.vishay.com/doc?85917

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#### **CARRIER TAPE** in millimeters: **CLP0603-2L**

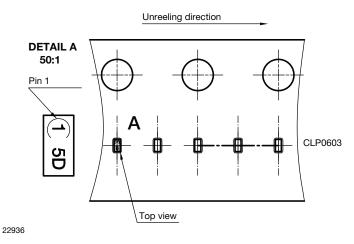




Cummulative tolerances of 10 sprocket holes is +/-0.2 mm

Document no. S8-V-3906.04-0025 (4) Created - Date: 22. Nov. 2010

## **ORIENTATION IN CARRIER CLP0603-2L**



Orientation in Carrier Tape (CLP0603) S8-V-3906.04-026 (4) 22.10.2010



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