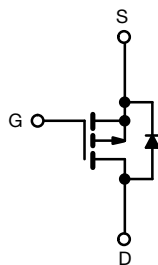
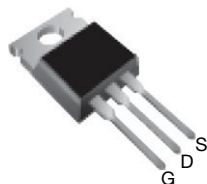


Power MOSFET

TO-220AB


P-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	-200	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	1.5
Q_g max. (nC)	22	
Q_{gs} (nC)	12	
Q_{gd} (nC)	10	
Configuration	Single	

FEATURES

- Dynamic dV/dt rating
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details



Available
RoHS*
Available

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF9620PbF
Lead (Pb)-free and halogen-free	IRF9620PbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-200	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	V_{GS} at -10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current ^a	I_{DM}	-14	
Linear serating factor		0.32	W/°C
Maximum power dissipation	P_D	40	W
Peak diode recovery dV/dt ^b	dV/dt	-5.0	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c	For 10 s	300	
Mounting torque	6-32 or M3 screw	10	
		1.1	N · m



Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $I_{SD} \leq -3.5$ A, $dI/dt \leq 95$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C
- 1.6 mm from case

THERMAL RESISTANCE RATINGS

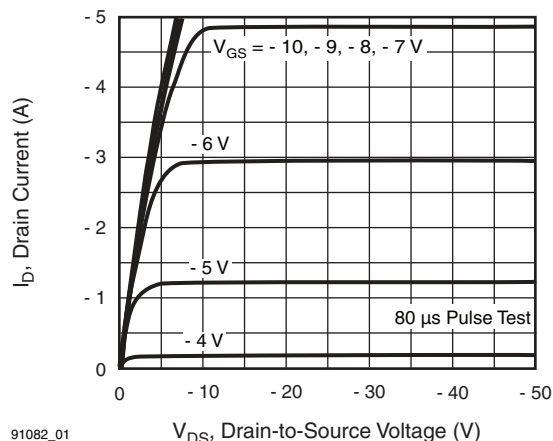
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	3.1	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

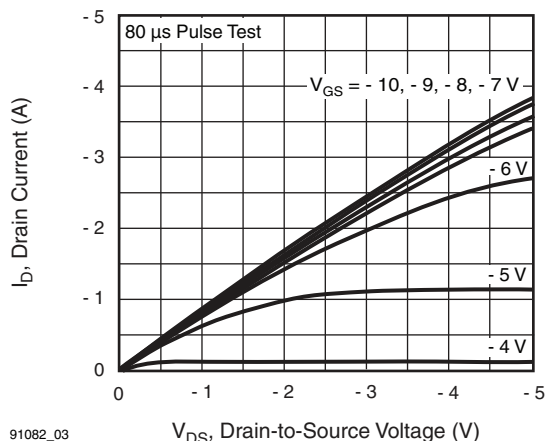
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA		-200	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = -1 mA		-	-0.22	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA		-2.0	-	-4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -200 V, V _{GS} = 0 V		-	-	-100	μA
		V _{DS} = -160 V, V _{GS} = 0 V, T _J = 125 °C		-	-	-500	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -1.5 A ^b	-	-	1.5	Ω
Forward transconductance	g _{fs}	V _{DS} = -50 V, I _D = -1.5 A ^b		1.0	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -25 V, f = 1.0 MHz, see fig. 5		-	350	-	pF
Output capacitance	C _{oss}			-	100	-	
Reverse transfer capacitance	C _{rss}			-	30	-	
Total gate charge	Q _g	V _{GS} = -10 V	I _D = -4.0 A, V _{DS} = -160 V, see fig. 11 and 18 ^b	-	-	22	nC
Gate-source charge	Q _{gs}			-	-	12	
Gate-drain charge	Q _{gd}			-	-	10	
Turn-on delay time	t _{d(on)}	V _{DD} = -100 V, I _D = -1.5 A, R _g = 50 Ω, R _D = 67 Ω, see fig. 17 ^b		-	15	-	ns
Rise time	t _r			-	25	-	
Turn-off delay time	t _{d(off)}			-	20	-	
Fall time	t _f			-	15	-	
Gate input resistance	R _g	f = 1 MHz, open drain		0.9	-	5.7	Ω
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	-3.5	A
Pulsed diode forward current ^a	I _{SM}			-	-	-14	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = -3.5 A, V _{GS} = 0 V ^b		-	-	-7.0	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = -3.5 A, dI/dt = 100 A/μs ^b		-	300	450	ns
Body diode reverse recovery charge	Q _{rr}			-	1.9	2.9	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

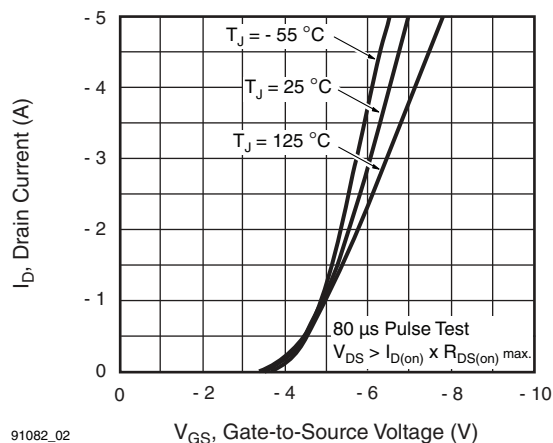
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\text{ }\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


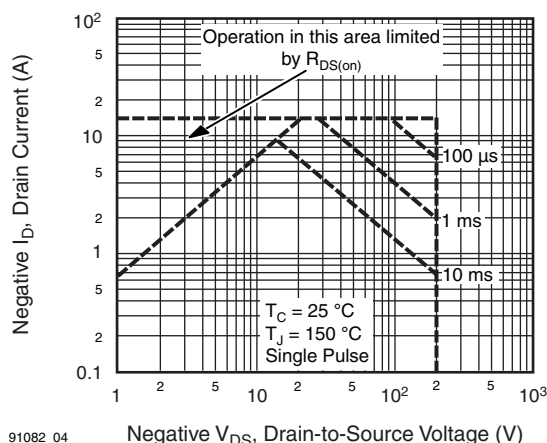
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Fig. 1 - Typical Output Characteristics


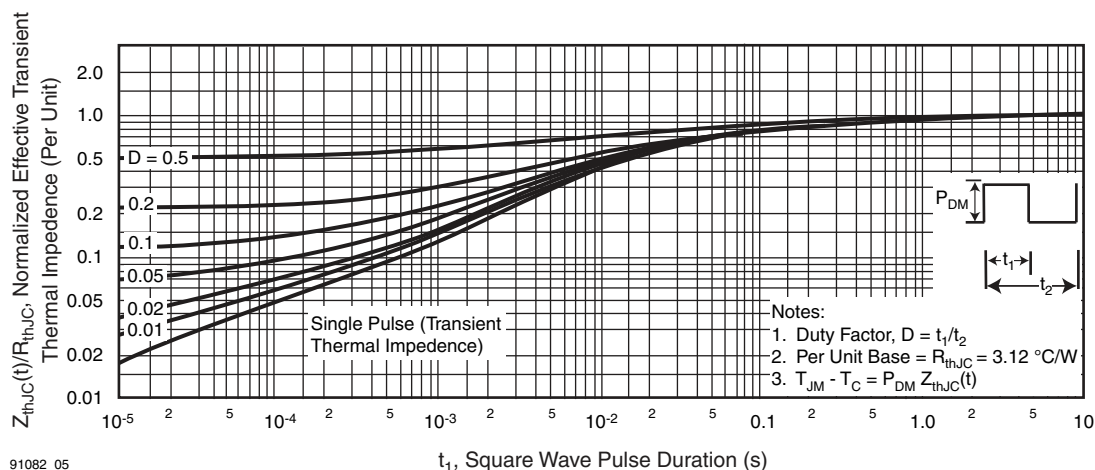
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Fig. 3 - Typical Saturation Characteristics


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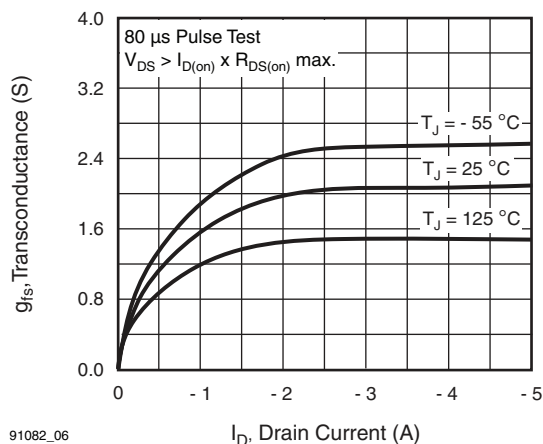
Fig. 2 - Typical Transfer Characteristics


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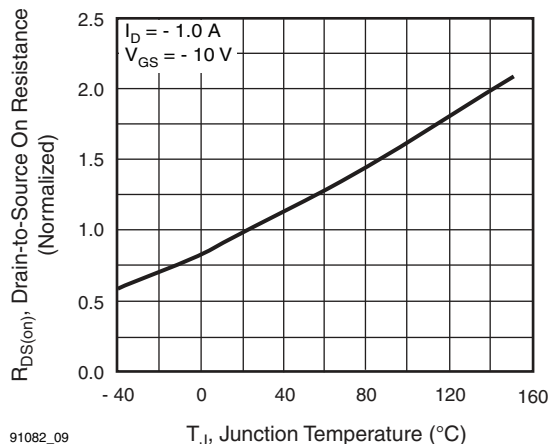
Fig. 4 - Maximum Safe Operating Area


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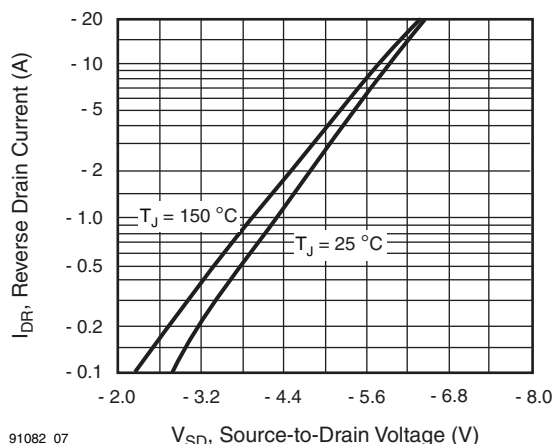
Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration



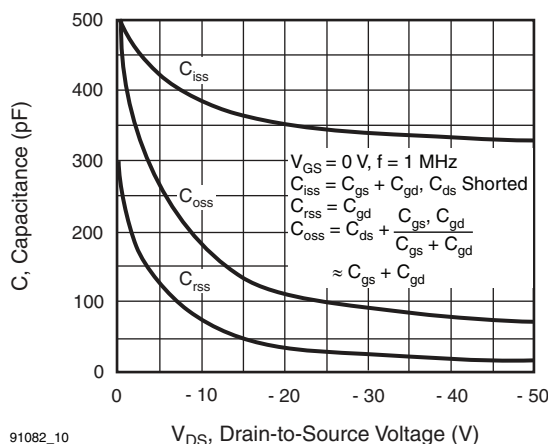
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Fig. 6 - Typical Transconductance vs. Drain Current


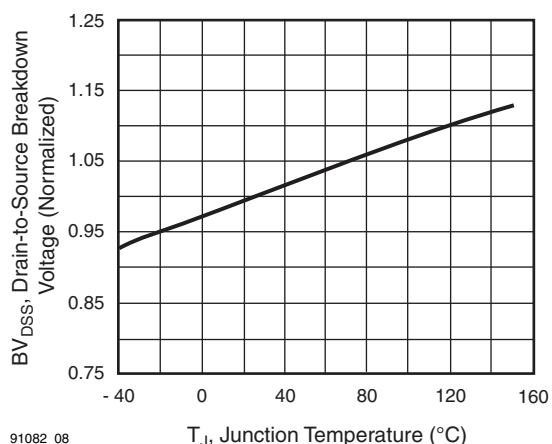
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Fig. 9 - Normalized On-Resistance vs. Temperature


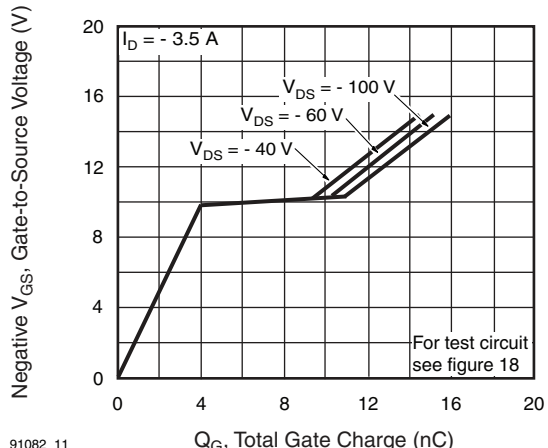
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Fig. 7 - Typical Source-Drain Diode Forward Voltage


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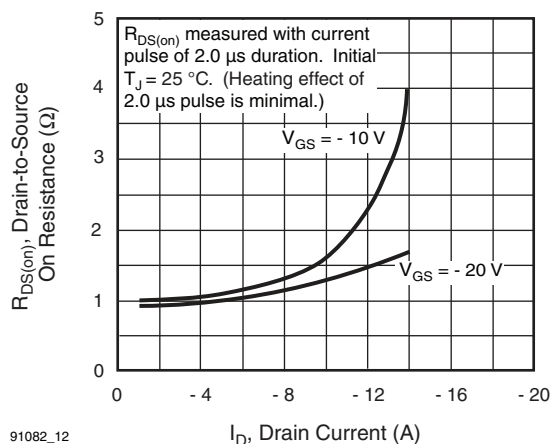
Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage


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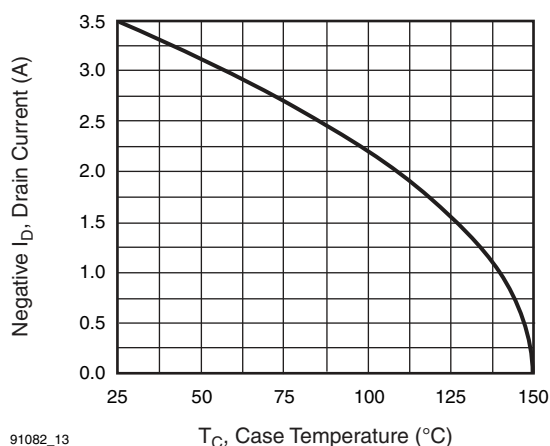
Fig. 8 - Breakdown Voltage vs. Temperature


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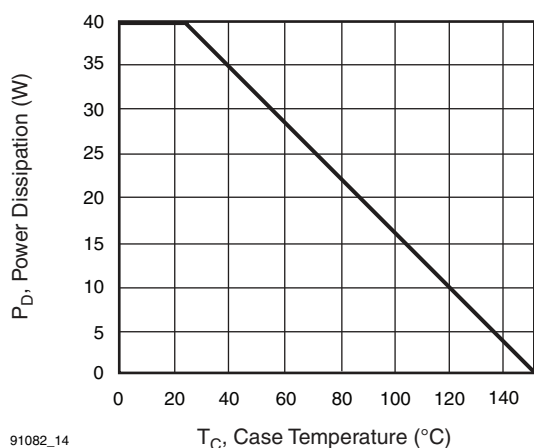
Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage



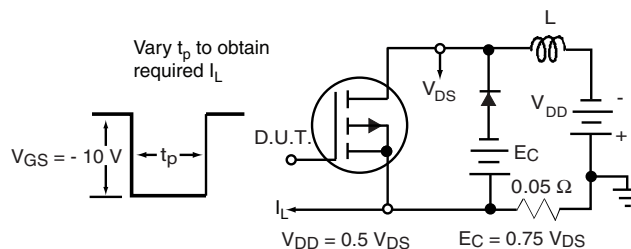
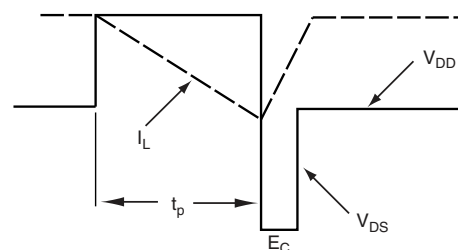
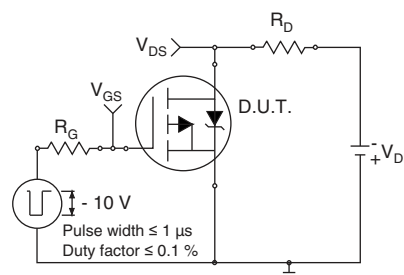
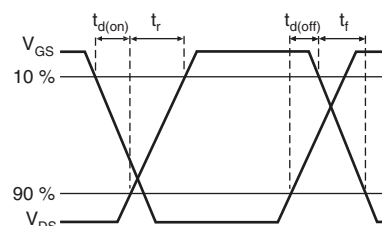
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Fig. 12 - Typical On-Resistance vs. Drain Current


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Fig. 13 - Maximum Drain Current vs. Case Temperature


91082_14

Fig. 14 - Power vs. Temperature Derating Curve

Fig. 15 - Clamped Inductive Test Circuit

Fig. 16 - Clamped Inductive Waveforms

Fig. 17a - Switching Time Test Circuit

Fig. 17b - Switching Time Waveforms

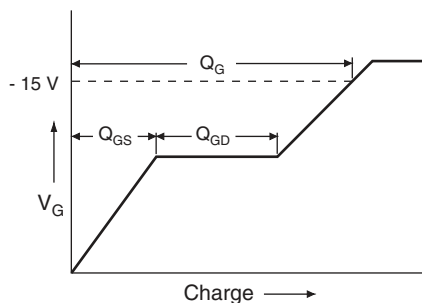


Fig. 18a - Basic Gate Charge Waveform

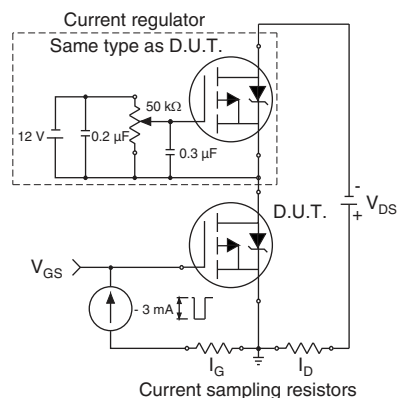


Fig. 18b - Gate Charge Test Circuit

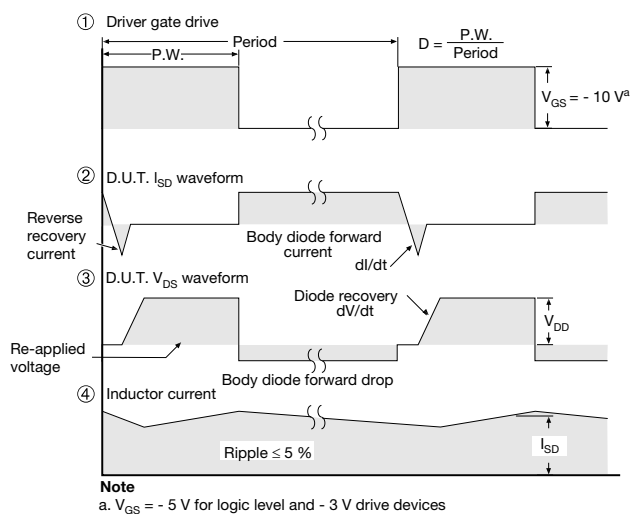
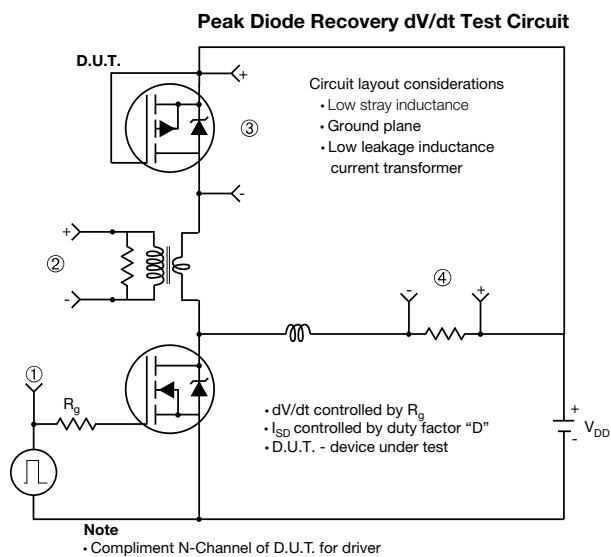


Fig. 19 - For P-Channel

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