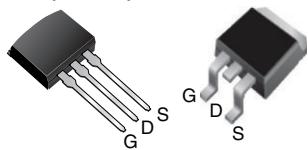
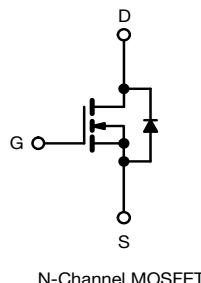


Power MOSFET

I²PAK (TO-262)

D²PAK (TO-263)


FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche, and dynamic dv/dt ruggedness
- Fully characterized capacitance and Avalanche voltage and current
- Effective C_{oss} specified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN FREE
Available

PRODUCT SUMMARY

V _{DS} (V)	600	
R _{DS(on)} (Ω)	V _{GS} = 10 V	2.2
Q _g max. (nC)	23	
Q _{gs} (nC)	5.4	
Q _{gd} (nC)	11	
Configuration	Single	

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

TYPICAL SMPS TOPOLOGIES

- Single transistor flyback

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and halogen-free	SiHFBC30AS-GE3	SiHFBC30ASTRL-GE3 ^a	SiHFBC30ASTRR-GE3 ^a	SiHFBC30AL-GE3
Lead (Pb)-free	IRFBC30ASPbF	IRFBC30ASTRLPbF ^a	-	IRFBC30ALPbF

Note

- a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	600	V
Gate-source voltage	V _{GS}	± 30	
Continuous drain current	V _{GS} at 10 V	3.6	A
		2.3	
Pulsed drain current ^{a, e}	I _{DM}	14	
Linear derating factor		0.69	W/°C
Single pulse avalanche energy ^b	E _{AS}	290	mJ
Avalanche current ^a	I _{AR}	3.6	A
Repetitive avalanche energy ^a	E _{AR}	7.4	mJ
Maximum power dissipation	P _D	74	W
Peak diode recovery dv/dt ^{c, e}	dv/dt	7.0	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d	for 10 s	300	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Starting T_J = 25 °C, L = 46 mH, R_G = 25 Ω, I_{AS} = 3.6 A (see fig. 12)
- c. I_{SD} ≤ 3.6 A, dI/dt ≤ 170 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C
- d. 1.6 mm from case
- e. Uses IRFBC30A/SiHFBC30A data and test conditions

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mounted, steady-state) ^a	R _{thJA}	-	40	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	1.7	

Note

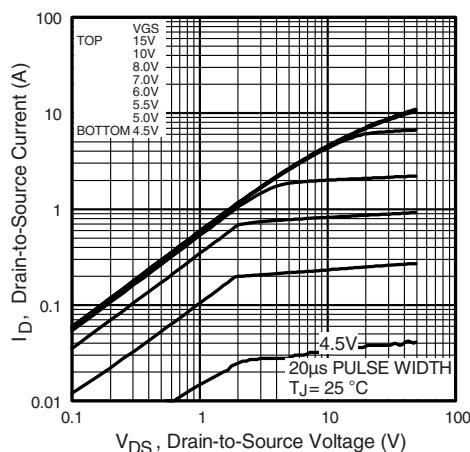
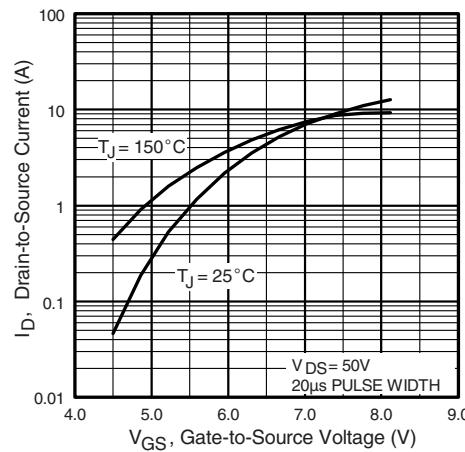
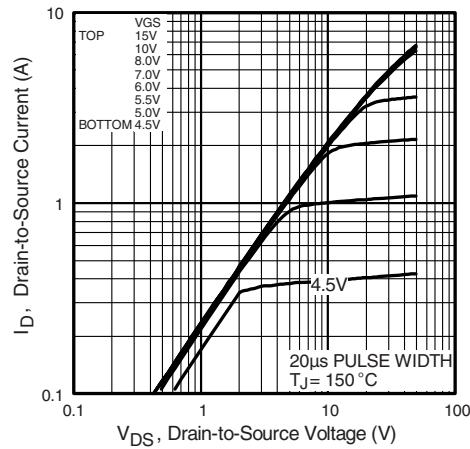
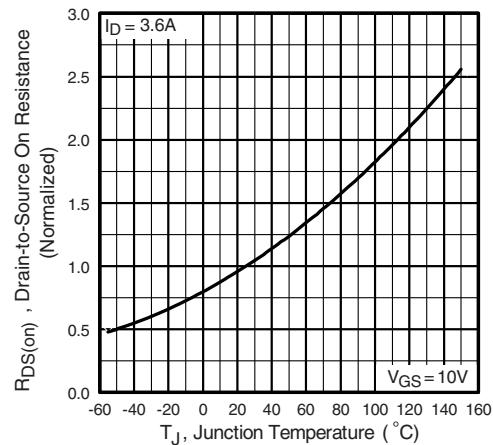
a. When mounted on 1" square PCB (FR-4 or G-10 material)

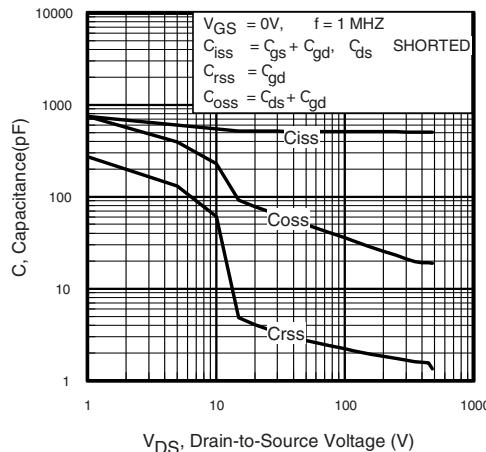
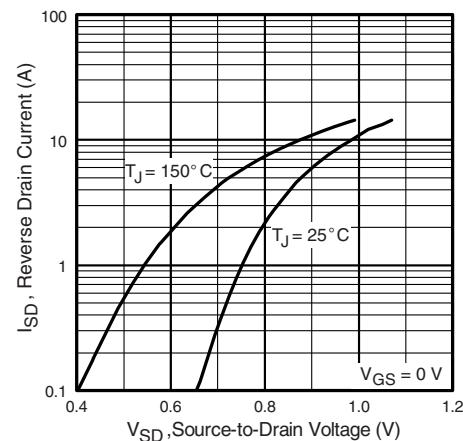
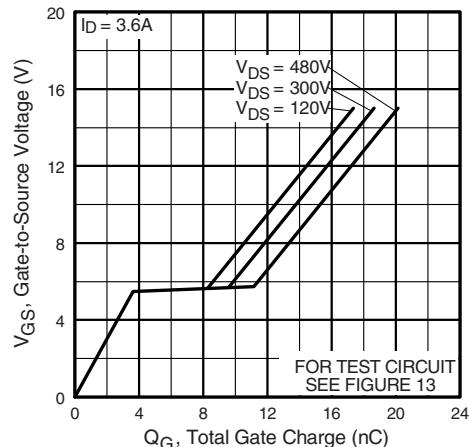
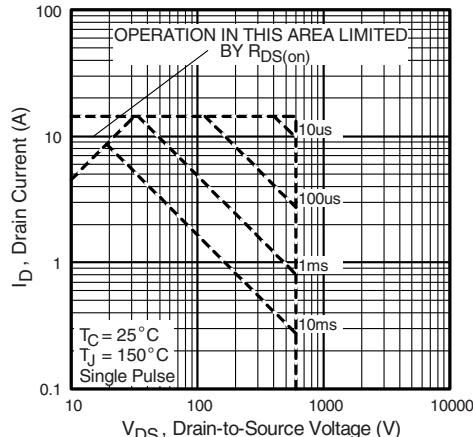
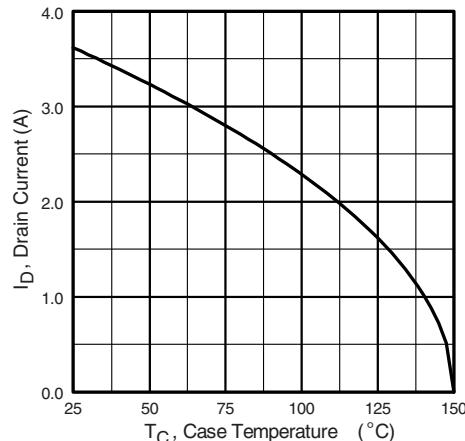
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

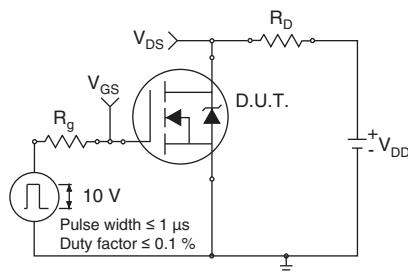
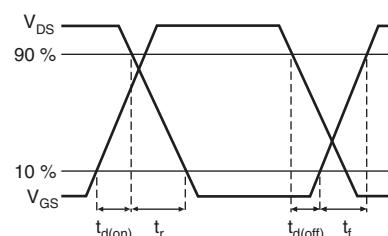
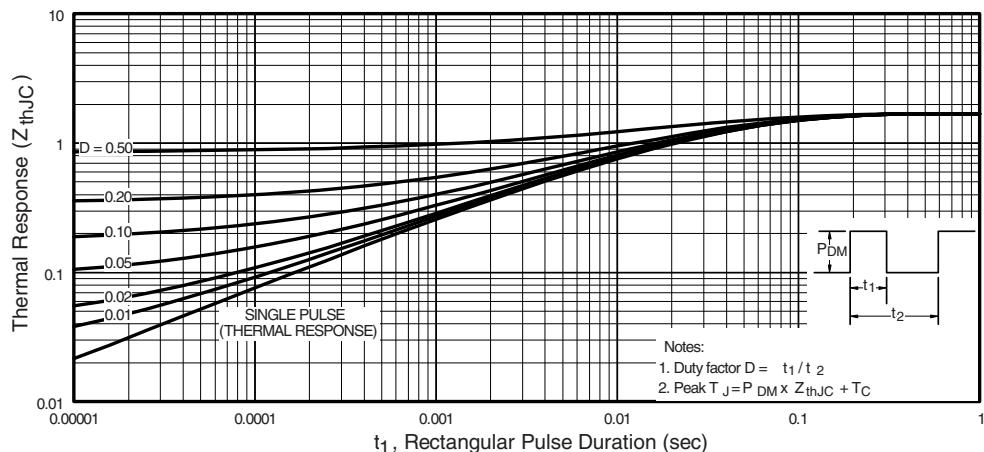
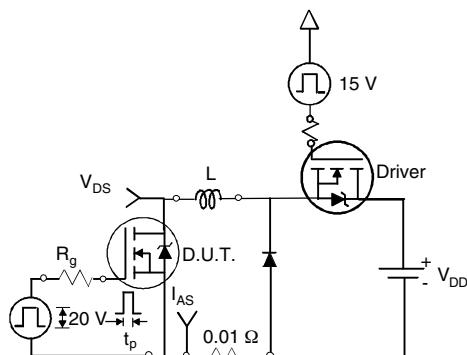
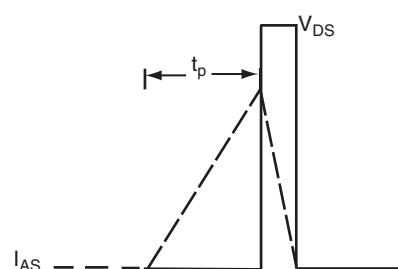
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		600	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA ^d		-	0.67	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.5	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 2.2 A ^b	-	-	2.2	Ω
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 2.2 A		2.1	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	510	-	pF
Output capacitance	C _{oss}			-	70	-	
Reverse transfer capacitance	C _{rss}			-	3.5	-	
Output capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	730	-	pF
Effective output capacitance	C _{oss eff.}		V _{DS} = 480 V, f = 1.0 MHz	-	19	-	
Total gate charge	Q _g		V _{DS} = 0 V to 480 V ^c	-	31	-	
Gate-source charge	Q _{gs}	V _{GS} = 10 V	I _D = 3.6 A, V _{DS} = 480 V, see fig. 6 and 13 ^b	-	-	23	nC
Gate-drain charge	Q _{gd}			-	-	5.4	
Turn-on delay time	t _{d(on)}			-	-	11	
Rise time	t _r	V _{DD} = 300 V, I _D = 3.6 A, R _g = 12 Ω, R _D = 82 Ω, see fig. 10 ^{b, d}	-	9.8	-	ns	
Turn-off delay time	t _{d(off)}		-	13	-		
Fall time	t _f		-	19	-		
Gate input resistance	R _g		f = 1 MHz, open drain	0.8	-	4.6	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode	I ^D	-	-	3.6	A
Pulsed diode forward current ^a	I _{SM}		I _S	-	-	14	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 3.6 A, V _{GS} = 0 V ^b		-	-	1.6	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 3.6 A, dI/dt = 100 A/μs ^b		-	400	600	ns
Body diode reverse recovery charge	Q _{rr}			-	1.1	1.7	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

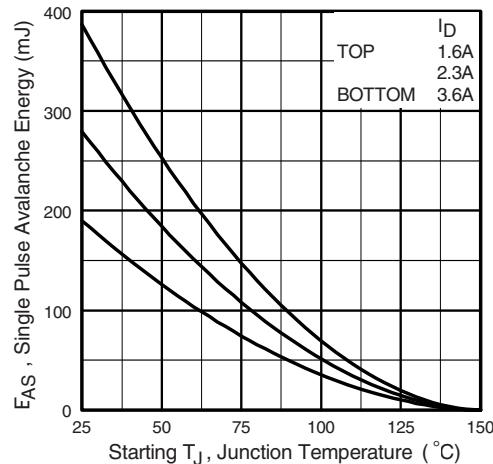
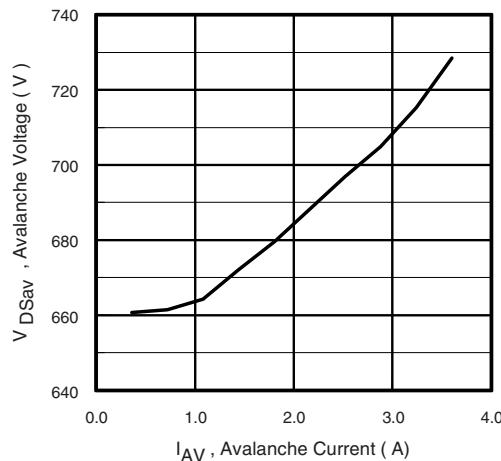
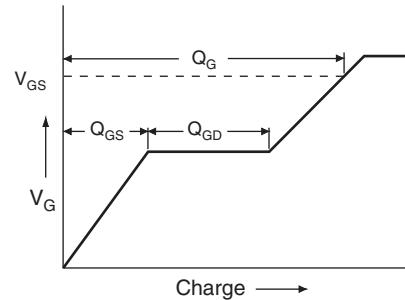
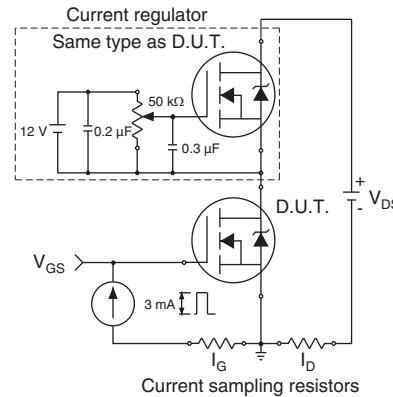
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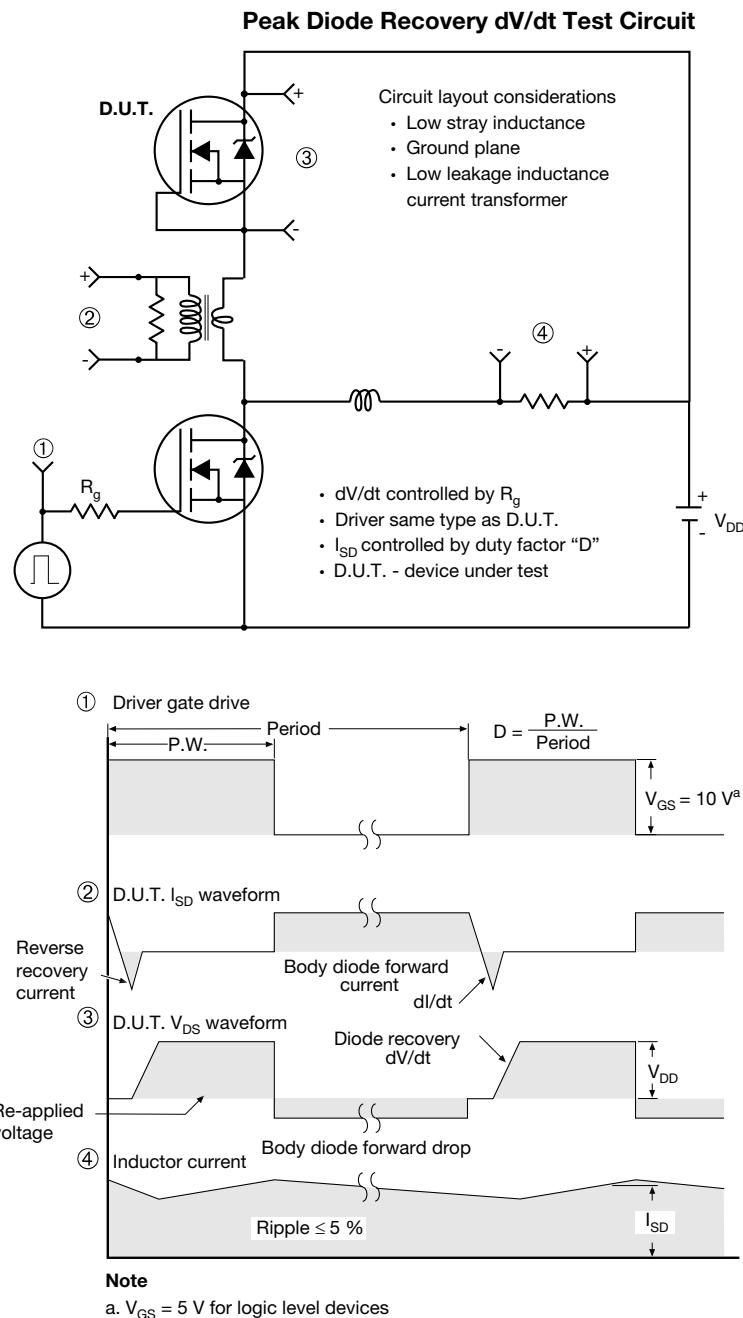
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %
- c. C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}
- d. Uses IRFBC30A/SiHFBC30A data and test conditions

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area

Fig. 9 - Maximum Drain Current vs. Case Temperature

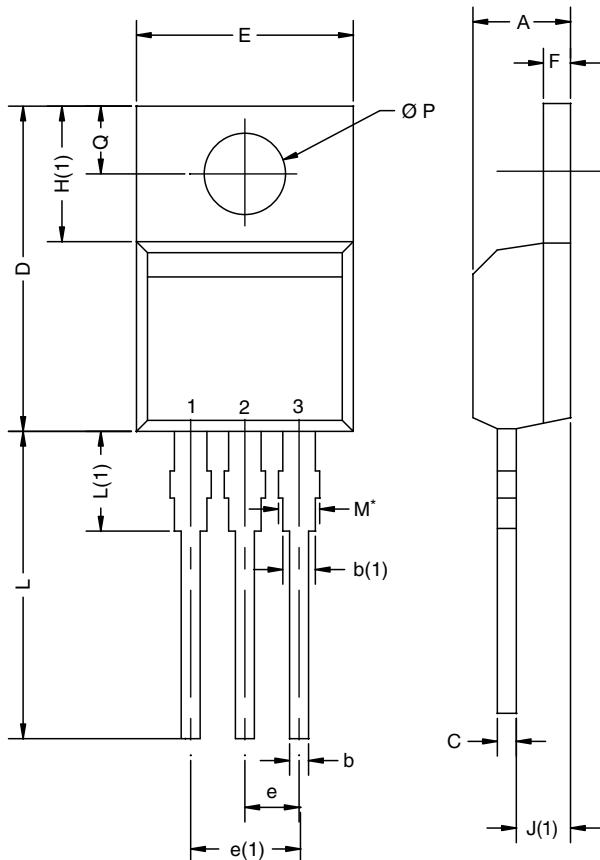
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit


Fig. 14 - For N-Channel

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TO-220AB



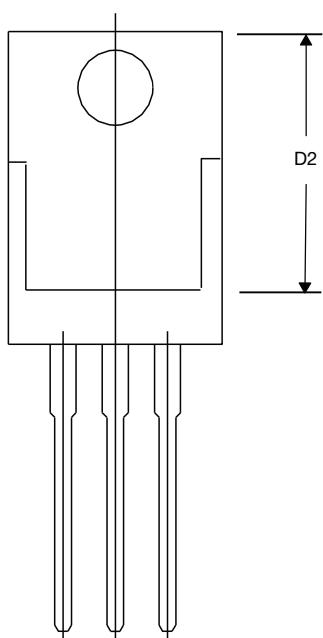
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
D2	12.19	12.70	0.480	0.500
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: T14-0413-Rev. P, 16-Jun-14

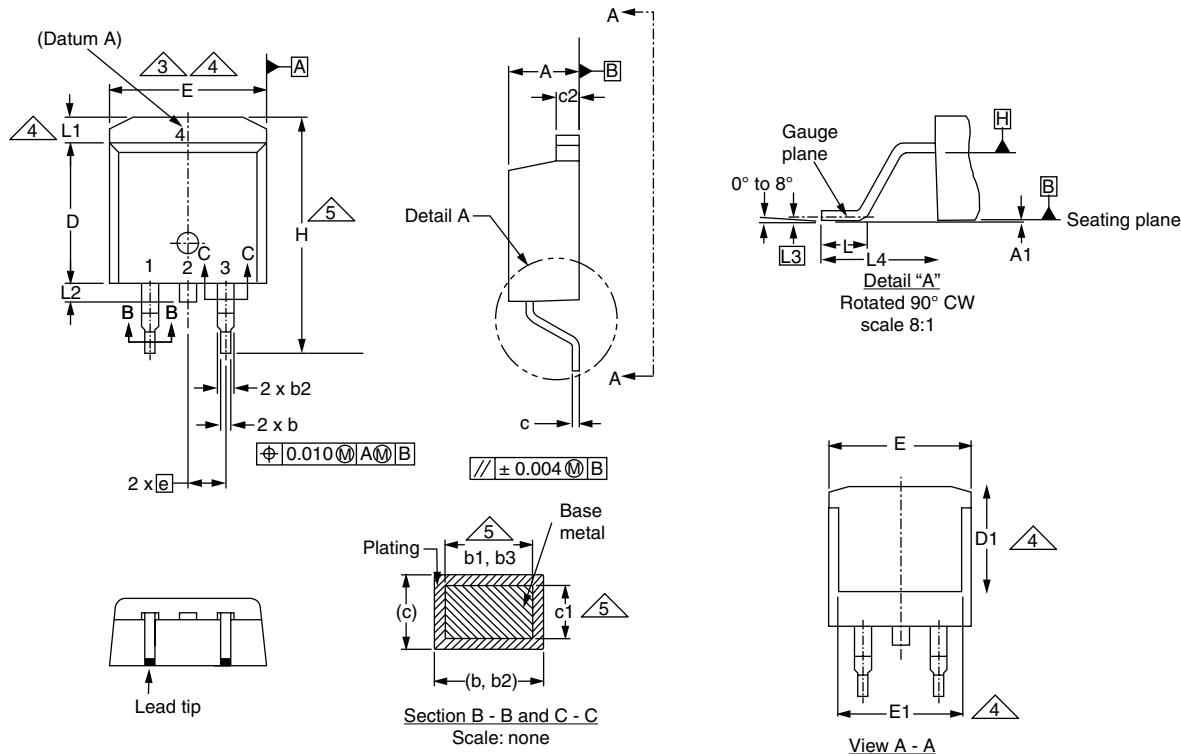
DWG: 5471

Note

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM



TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

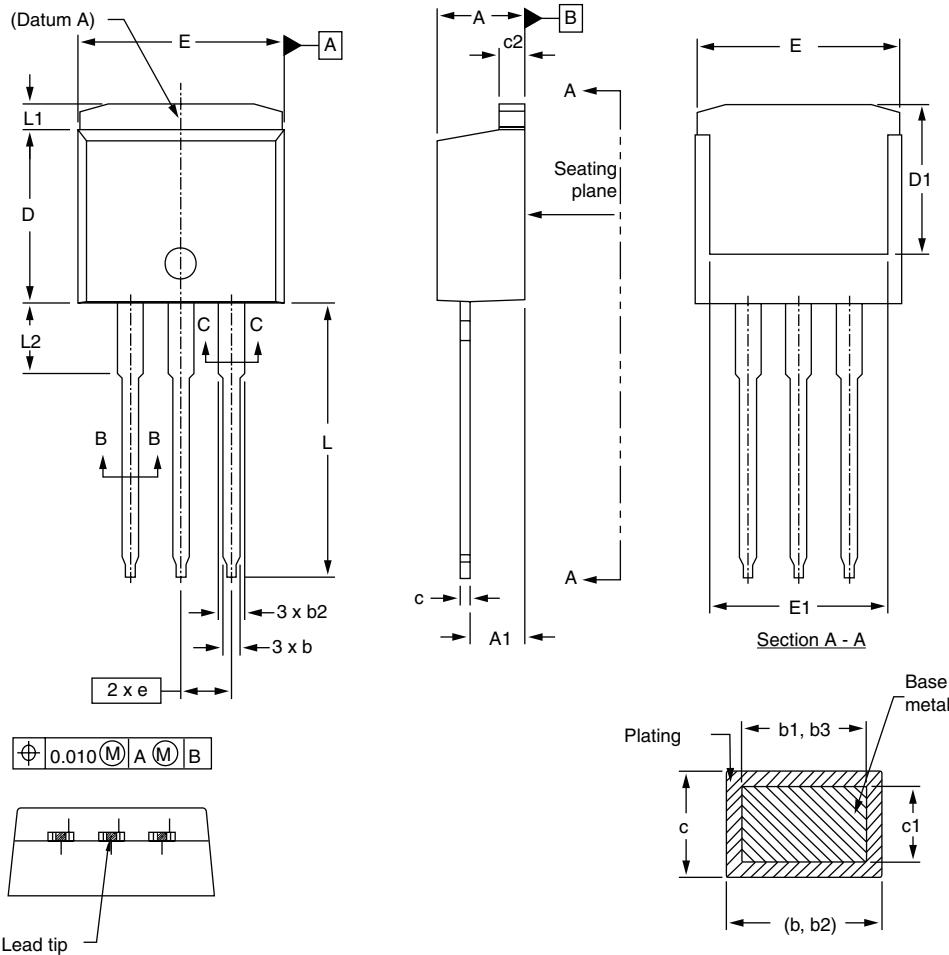
ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Dimensions are shown in millimeters (inches).
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- Thermal PAD contour optional within dimension E, L1, D1 and E1.
- Dimension b1 and c1 apply to base metal only.
- Datum A and B to be determined at datum plane H.
- Outline conforms to JEDEC outline to TO-263AB.

I²PAK (TO-262) (HIGH VOLTAGE)



Section B - B and C - C

Scale: None

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

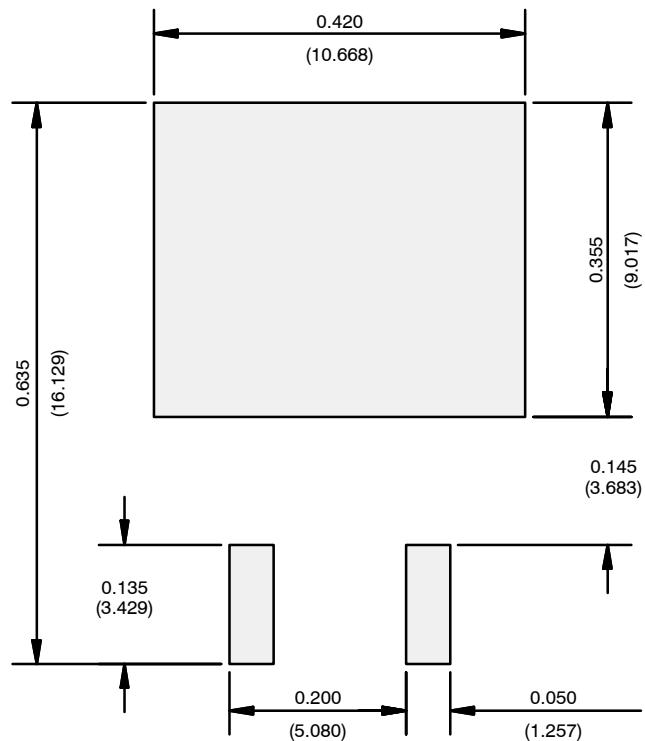
ECN: S-82442-Rev. A, 27-Oct-08

DWG: 5977

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
- Thermal pad contour optional within dimension E, L1, D1, and E1.
- Dimension b1 and c1 apply to base metal only.

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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