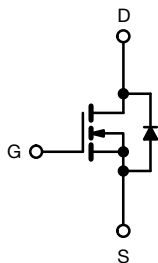


# Power MOSFET

**TO-220 FULLPAK**


N-Channel MOSFET

## FEATURES

- Low gate charge  $Q_g$  results in simple drive requirement
- Improved gate, avalanche and dynamic  $dV/dt$  ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

## APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching
- High voltage isolation = 2.5 kV<sub>RMS</sub> (t = 60 s, f = 60 Hz)

## TYPICAL SMPS TOPOLOGIES

- Single transistor flyback
- Single transistor forward

## PRODUCT SUMMARY

$V_{DS}$ (V)	650	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.93
$Q_g$ (Max.) (nC)	48	
$Q_{gs}$ (nC)	12	
$Q_{gd}$ (nC)	19	
Configuration	Single	

## ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIB5N65APbF

## ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	650	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current <sup>a</sup>	$I_D$	5.1	A
Continuous drain current		3.2	
Pulsed drain current <sup>a</sup>	$I_{DM}$	21	
Linear derating factor		0.48	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	325	mJ
Repetitive avalanche current <sup>a</sup>	$I_{AR}$	5.2	A
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	6	mJ
Maximum power dissipation	$P_D$	60	W
Peak diode recovery $dV/dt$ <sup>c</sup>	$dV/dt$	2.8	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300	
Mounting torque	M3 screw	0.6	Nm


### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 24\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 5.2\text{ A}$  (see fig. 12)
- $I_{SD} \leq 5.2\text{ A}$ ,  $dI/dt \leq 90\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case
- Drain current limited by maximum junction temperature

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	65	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	2.1	

**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

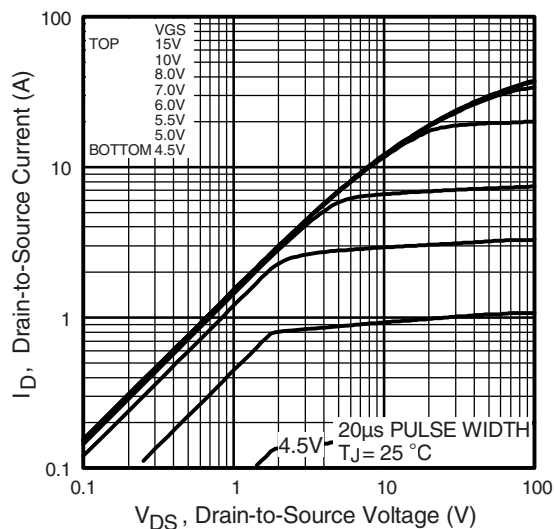
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-ssource breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		650	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA <sup>d</sup>		-	670	-	mV/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.1 A <sup>b</sup>	-	-	0.93	Ω
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 3.1 A		3.9	-	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	1417	-	pF
Output capacitance	C <sub>Oss</sub>			-	177	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	7.0	-	
Output capacitance	C <sub>Oss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 1.0 V, f = 1.0 MHz	-	1912	-	pF
			V <sub>DS</sub> = 520 V, f = 1.0 MHz	-	48	-	
Effective output capacitance	C <sub>Oss</sub> eff.		V <sub>DS</sub> = 0 V to 520 V <sup>c</sup>	-	84	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 5.2 A, V <sub>DS</sub> = 400 V see fig. 6 and 13 <sup>b</sup>	-	-	48	nC
Gate-source charge	Q <sub>gs</sub>			-	-	12	
Gate-drain charge	Q <sub>gd</sub>			-	-	19	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 325 V, I <sub>D</sub> = 5.2 A R <sub>G</sub> = 9.1 Ω, R <sub>D</sub> = 62 Ω, see fig. 10 <sup>b</sup>		-	14	-	ns
Rise time	t <sub>r</sub>			-	20	-	
Turn-off delay time	t <sub>d(off)</sub>			-	34	-	
Fall time	t <sub>f</sub>			-	18	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	5.2	A
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>			-	-	21	
Body diode voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 5.2 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.5	V
Body diode reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 5.2 A, dI/dt = 100 A/μs <sup>b</sup>		-	493	739	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	2.1	3.2	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

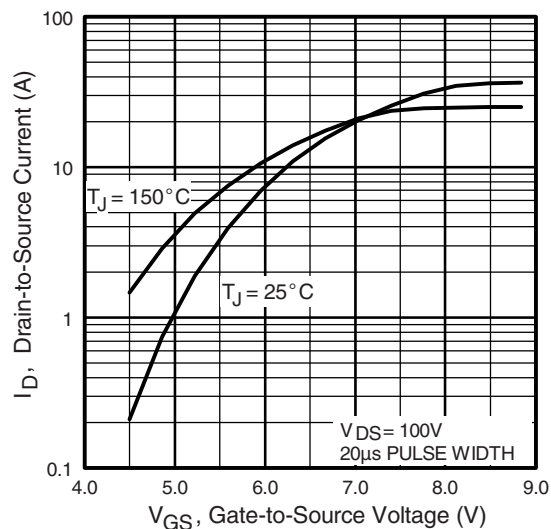
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$   
c.  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$   
d.  $t = 60\text{ s}$ ,  $f = 60\text{ Hz}$



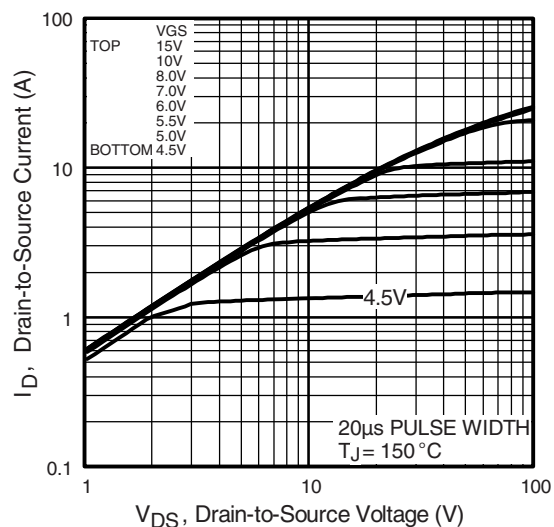
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



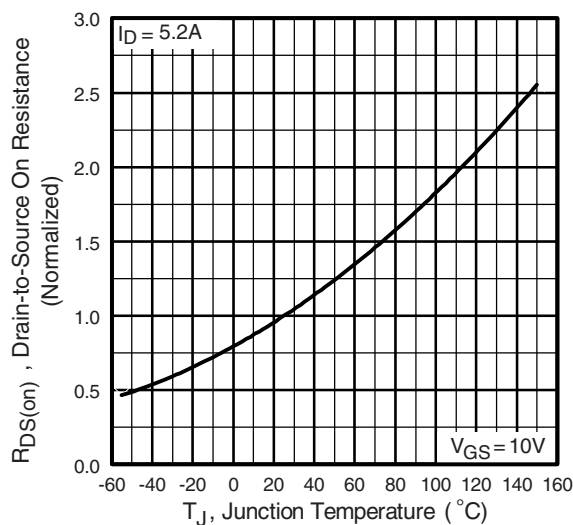
**Fig. 1 - Typical Output Characteristics**



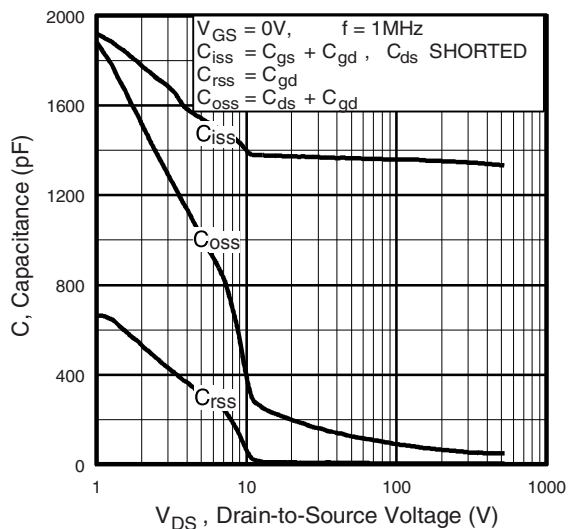
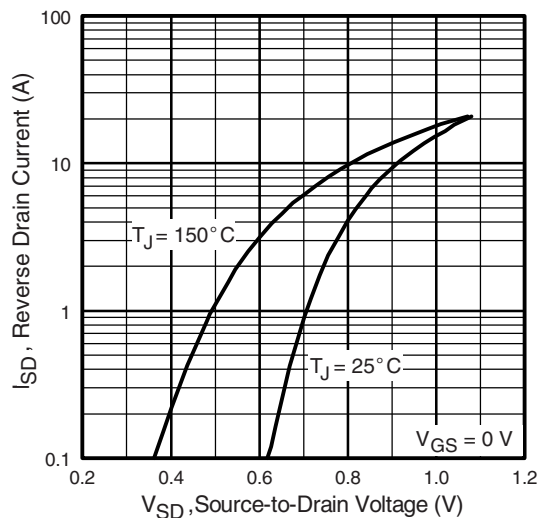
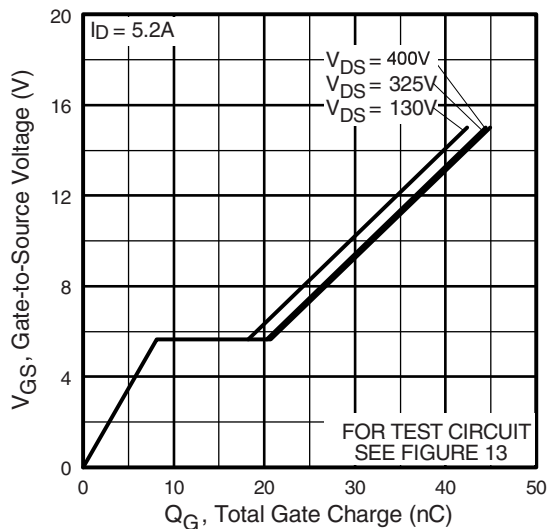
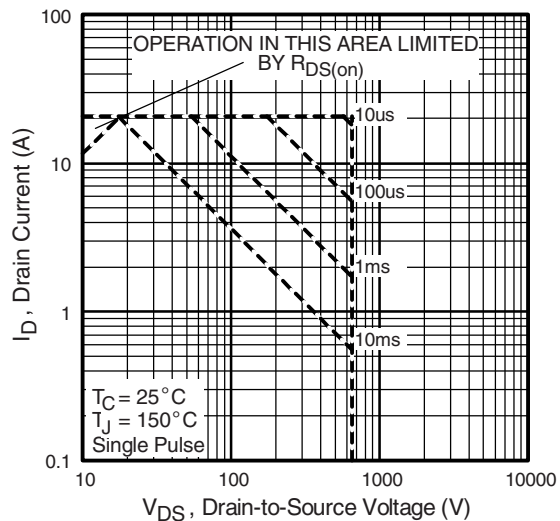
**Fig. 3 - Typical Transfer Characteristics**

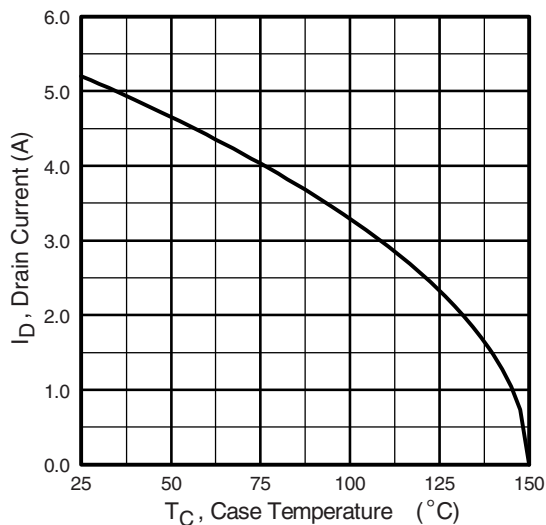
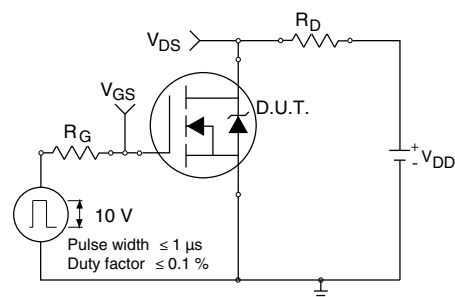
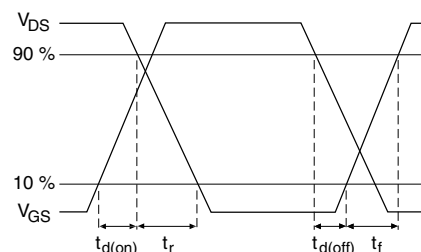
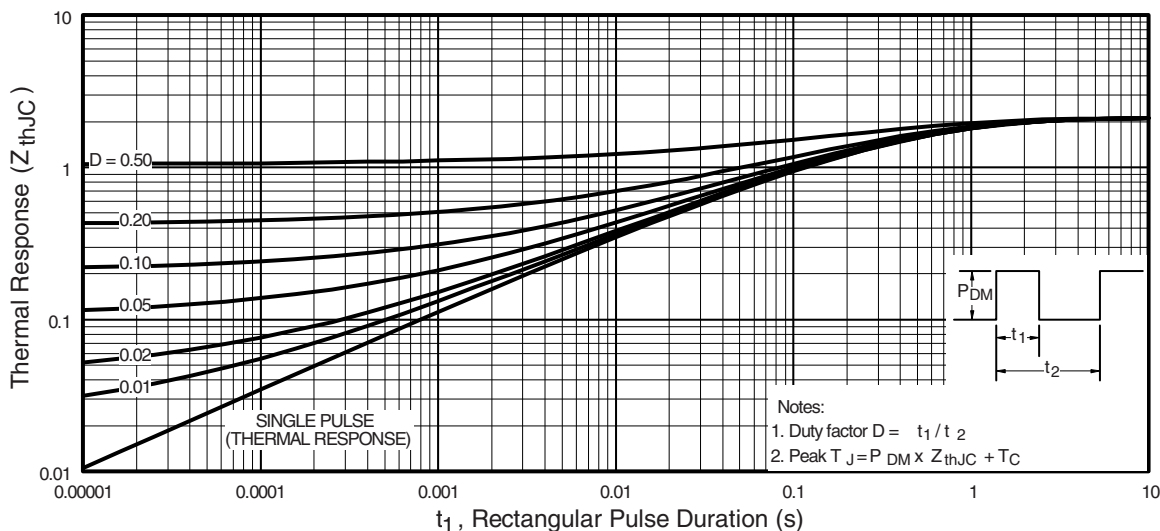


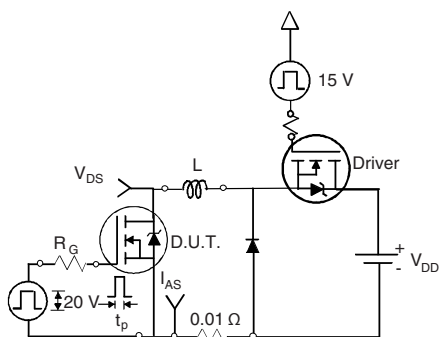
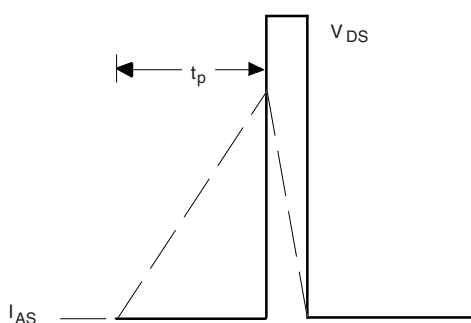
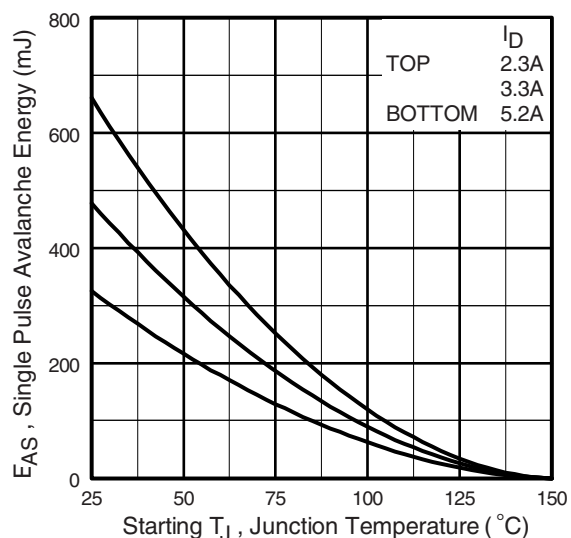
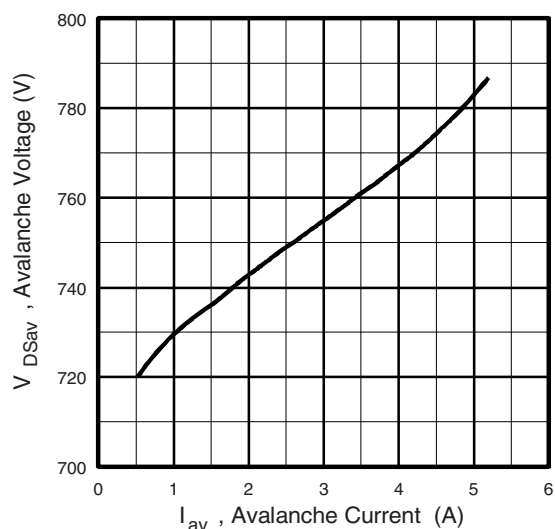
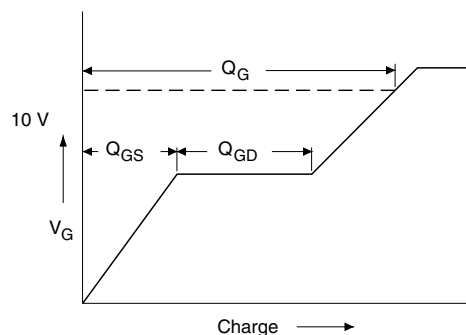
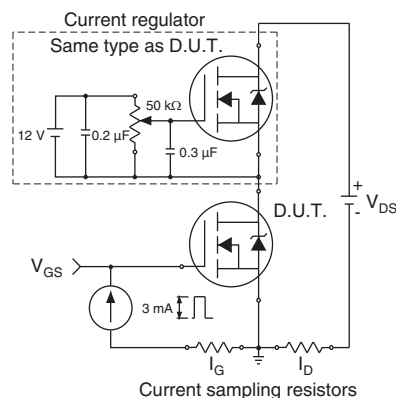
**Fig. 2 - Typical Output Characteristics**



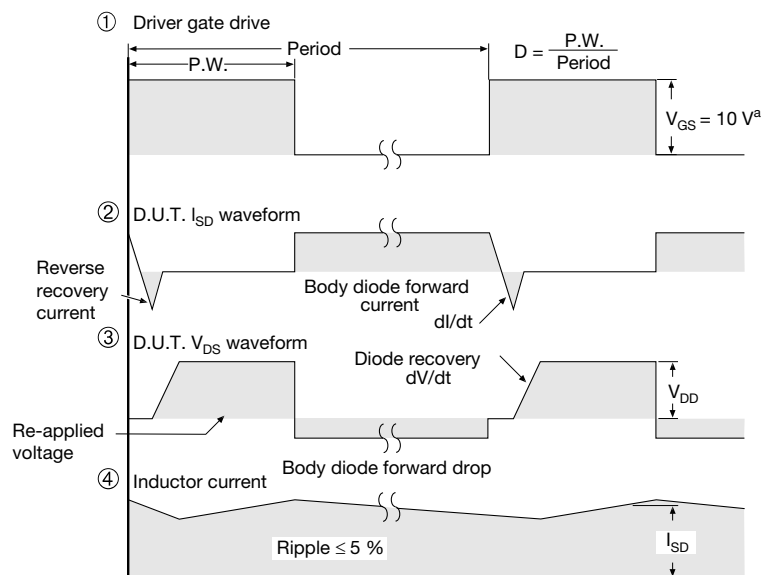
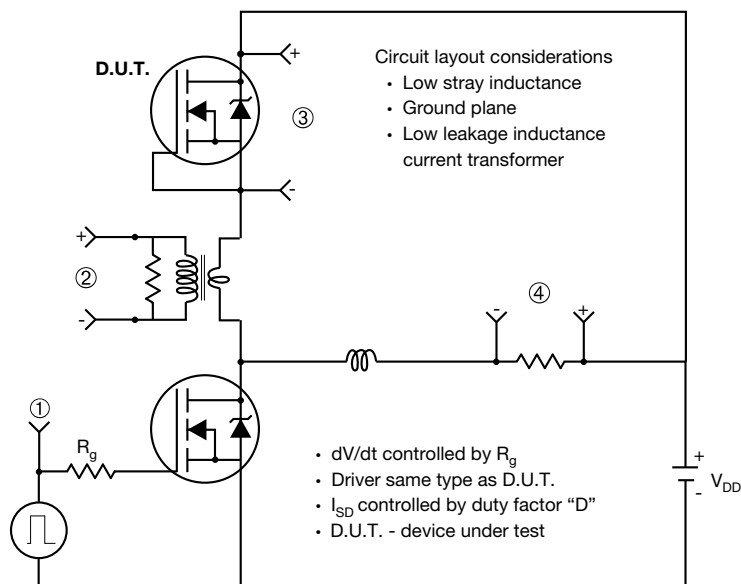
**Fig. 4 - Normalized On-Resistance vs. Temperature**


**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 8 - Maximum Safe Operating Area**


**Fig. 9 - Maximum Drain Current vs. Case Temperature**

**Fig. 10a - Switching Time Test Circuit**

**Fig. 10b - Switching Time Waveforms**

**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**


**Fig. 12a - Unclamped Inductive Test Circuit**

**Fig. 12b - Unclamped Inductive Waveforms**

**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

**Fig. 12d - Typical Drain-to Source Voltage vs. Avalanche Current**

**Fig. 13a - Basic Gate Charge Waveform**

**Fig. 13b - Gate Charge Test Circuit**

### Peak Diode Recovery dV/dt Test Circuit



#### Note

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

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## TO-220 FULLPAK (High Voltage)

### OPTION 1: FACILITY CODE = 9



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Ø R	3.08	3.18	3.28

#### Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking





## OPTION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019  
DWG: 5972

## Notes

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2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
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6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking



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