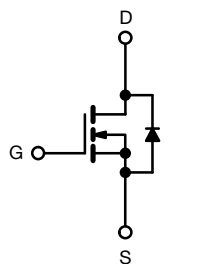
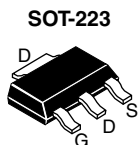


Power MOSFET



N-Channel MOSFET

Marking code: FB

| PRODUCT SUMMARY | | |
|---------------------------|------------------------|------|
| V_{DS} (V) | 100 | |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10\text{ V}$ | 0.54 |
| Q_g (Max.) (nC) | 8.3 | |
| Q_{gs} (nC) | 2.3 | |
| Q_{gd} (nC) | 3.8 | |
| Configuration | Single | |

| ORDERING INFORMATION | |
|---------------------------------|----------------------------------|
| Package | SOT-223 |
| Lead (Pb)-free and halogen-free | SiHFL110TR-GE3 ^a |
| | SiHFL110TR-BE3 ^{a, b} |
| | IRFL110TRPBF-BE3 ^{a, b} |
| Lead (Pb)-free | IRFL110TRPbF ^a |

Notes

- a. See device orientation
b. "-BE3" denotes alternate manufacturing location

| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | | |
|---|-------------------------|-------------------------|-----------------------------------|-------------|------|
| PARAMETER | | | SYMBOL | LIMIT | UNIT |
| Drain-source voltage | | | V _{DS} | 100 | V |
| Gate-source voltage | | | V _{GS} | ± 20 | |
| Continuous drain current | V _{GS} at 10 V | T _C = 25 °C | I _D | 1.5 | A |
| | | T _C = 100 °C | | 0.96 | |
| Pulsed drain current ^a | | | I _{DM} | 12 | W/°C |
| Linear derating factor | | | | 0.025 | |
| Linear derating factor (PCB mount) ^e | | | | 0.017 | |
| Single pulse avalanche energy ^b | | | E _{AS} | 150 | mJ |
| Avalanche current ^a | | | I _{AR} | 1.5 | A |
| Repetitive avalanche energy ^a | | | E _{AR} | 0.31 | mJ |
| Maximum power dissipation | T _C = 25 °C | | P _D | 3.1 | W |
| Maximum power dissipation (PCB mount) ^e | T _A = 25 °C | | | 2.0 | |
| Peak diode recovery dv/dt ^c | | | dV/dt | 5.5 | V/ns |
| Operating junction and storage temperature range | | | T _J , T _{stg} | -55 to +150 | °C |
| Soldering recommendations (peak temperature) ^d | For 10 s | | | 300 | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 25\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 3.0\text{ A}$ (see fig. 12)
c. $I_{SD} \leq 5.6\text{ A}$, $di/dt \leq 75\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
d. 1.6 mm from case
e. When mounted on 1" square PCB (FR-4 or G-10 material)

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.



RoHS
COMPLIANT
HALOGEN
FREE
Available

**THERMAL RESISTANCE RATINGS**

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--|------------|------|------|------|------|
| Maximum junction-to-ambient (PCB mount) ^a | R_{thJA} | - | - | 60 | °C/W |
| Maximum junction-to-case (drain) | R_{thJC} | - | - | 40 | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|----------------------------------|--|---|------|------|-------|------|
| Static | | | | | | | |
| Drain-source breakdown voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | | 100 | - | - | V |
| V _{DS} temperature coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA | | - | 0.63 | - | V/°C |
| Gate-source threshold voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | | 2.0 | - | 4.0 | V |
| Gate-source leakage | I _{GSS} | V _{GS} = ± 20 V | | - | - | ± 100 | nA |
| Zero gate voltage drain current | I _{DSS} | V _{DS} = 100 V, V _{GS} = 0 V | | - | - | 25 | μA |
| | | V _{DS} = 80 V, V _{GS} = 0 V, T _J = 125 °C | | - | - | 250 | |
| Drain-source on-state resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 0.90 A ^b | - | - | 0.54 | Ω |
| Forward transconductance | g _{fs} | V _{DS} = 50 V, I _D = 0.90 A | | 1.1 | - | - | S |
| Dynamic | | | | | | | |
| Input capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 | | - | 180 | - | pF |
| Output capacitance | C _{oss} | | | - | 81 | - | |
| Reverse transfer capacitance | C _{rss} | | | - | 15 | - | |
| Total gate charge | Q _g | V _{GS} = 10 V | I _D = 5.6 A, V _{DS} = 80 V, see fig. 6 and 13 ^b | - | - | 8.3 | nC |
| Gate-source charge | Q _{gs} | | | - | - | 2.3 | |
| Gate-drain charge | Q _{gd} | | | - | - | 3.8 | |
| Turn-on delay time | t _{d(on)} | V _{DD} = 50 V, I _D = 5.6 A, R _g = 24 Ω, R _D = 8.4 Ω, see fig. 10 ^b | | - | 6.9 | - | ns |
| Rise time | t _r | | | - | 16 | - | |
| Turn-off delay time | t _{d(off)} | | | - | 15 | - | |
| Fall time | t _f | | | - | 9.4 | - | |
| Internal drain inductance | L _D | Between lead, 6 mm (0.25") from package and center of die contact | | - | 4.0 | - | nH |
| Internal source inductance | L _S | | | - | 6.0 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous source-drain diode current | I _S | MOSFET symbol showing the integral reverse p - n junction diode | | - | - | 1.5 | A |
| Pulsed diode forward current ^a | I _{SM} | | | - | - | 12 | |
| Body diode voltage | V _{SD} | T _J = 25 °C, I _S = 1.5 A, V _{GS} = 0 V ^b | | - | - | 2.5 | V |
| Body diode reverse recovery time | t _{rr} | T _J = 25 °C, I _F = 5.6 A, dI/dt = 100 A/μs ^b | | - | 100 | 200 | ns |
| Body diode reverse recovery charge | Q _{rr} | | | - | 0.44 | 0.88 | μC |
| Forward turn-on time | t _{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D) | | | | | |

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

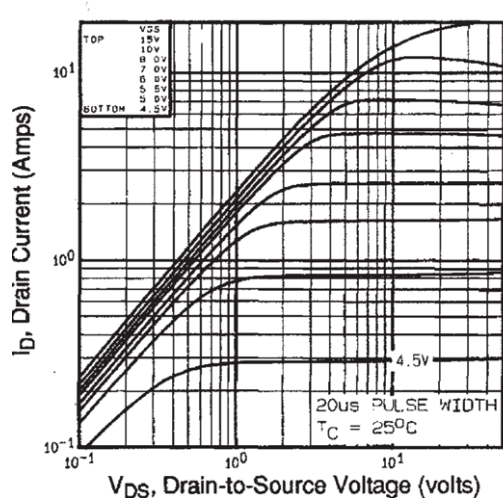


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$

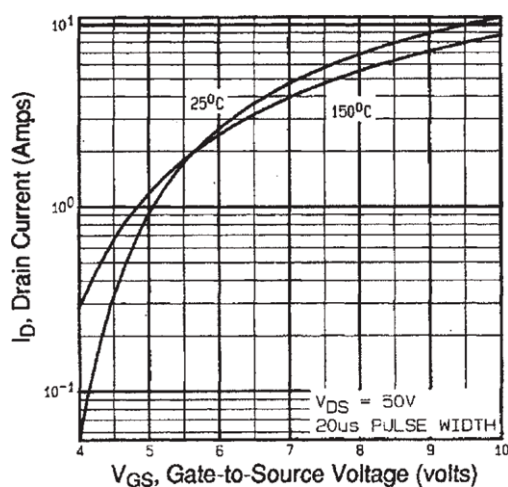


Fig. 3 - Typical Transfer Characteristics

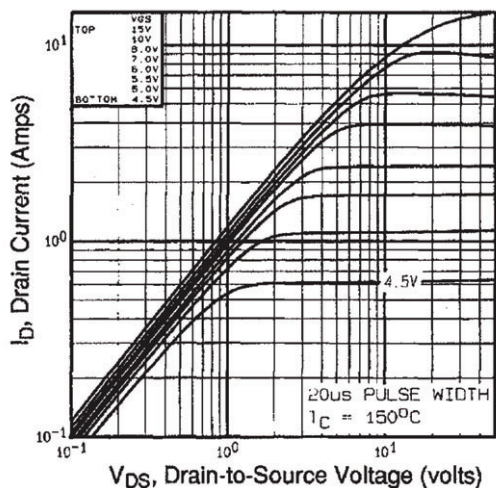


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^{\circ}\text{C}$

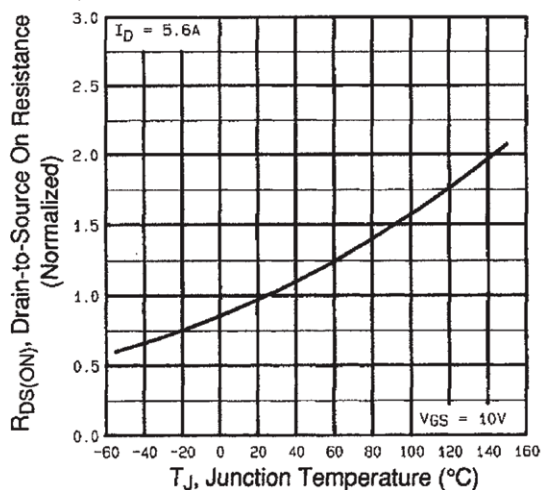
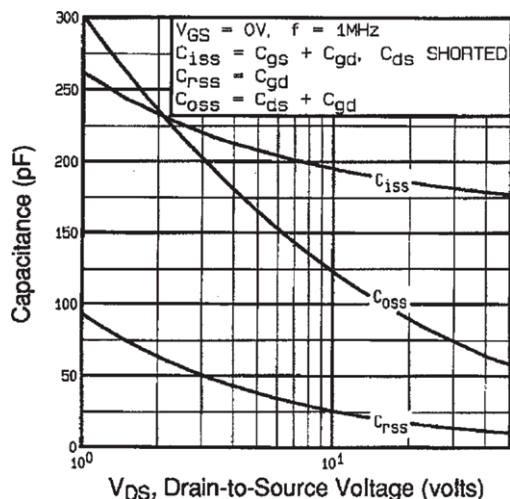
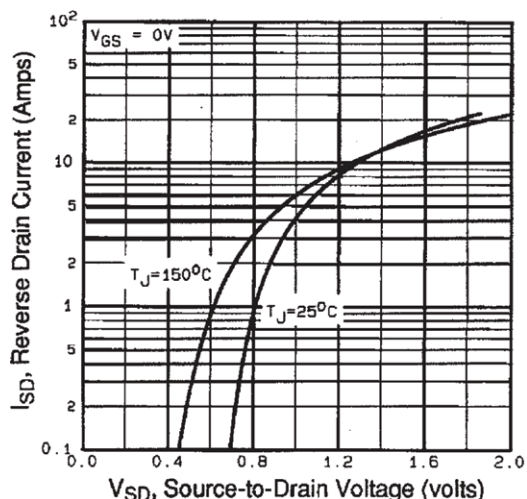
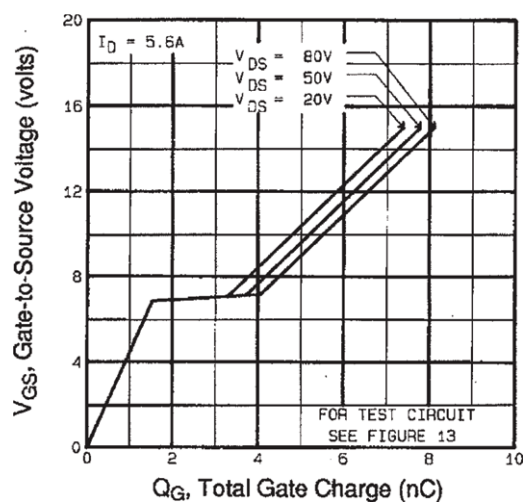
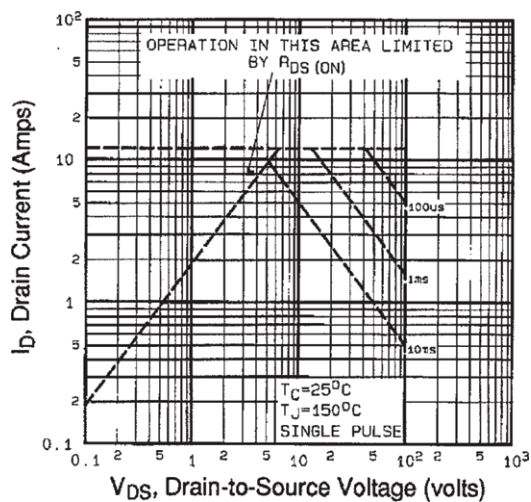
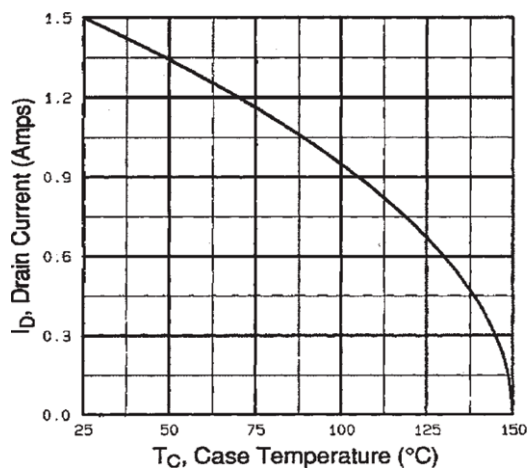
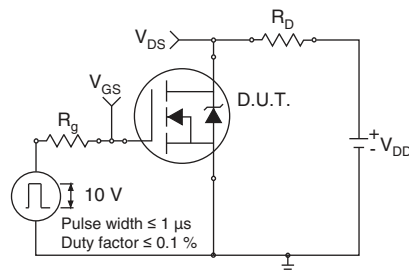
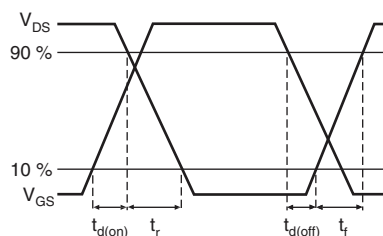
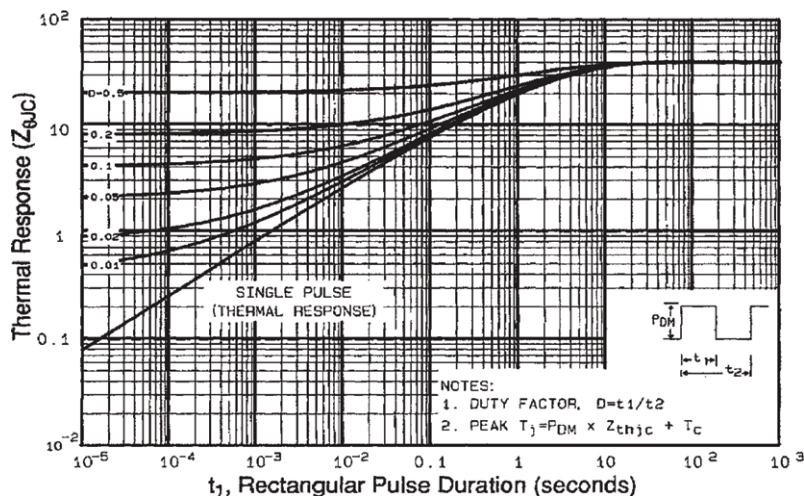
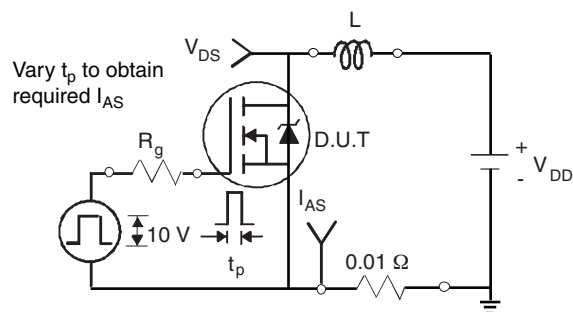
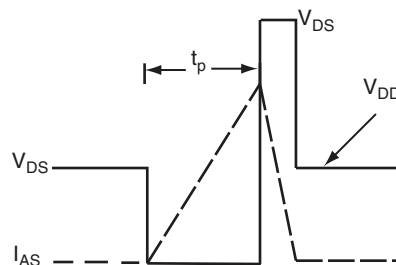
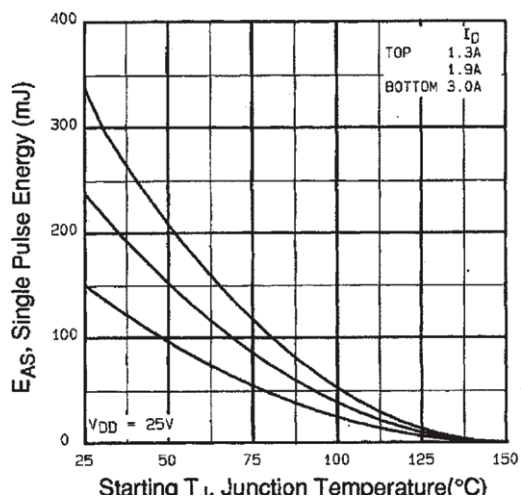
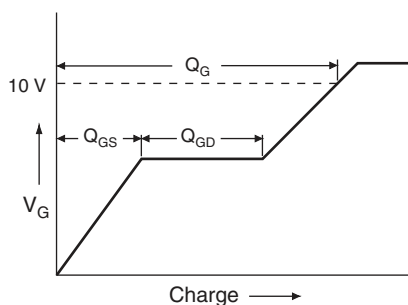
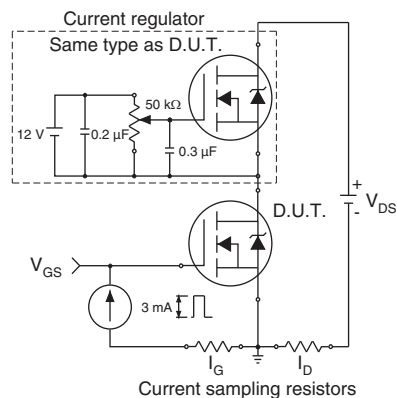
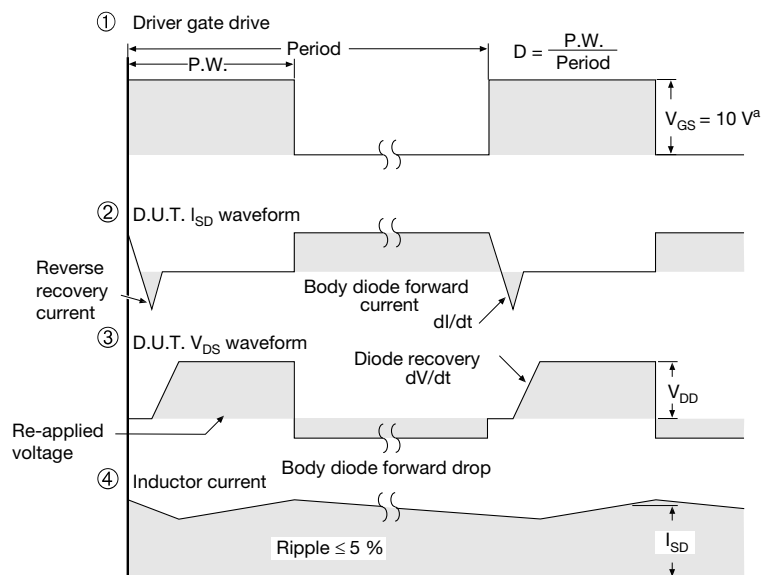
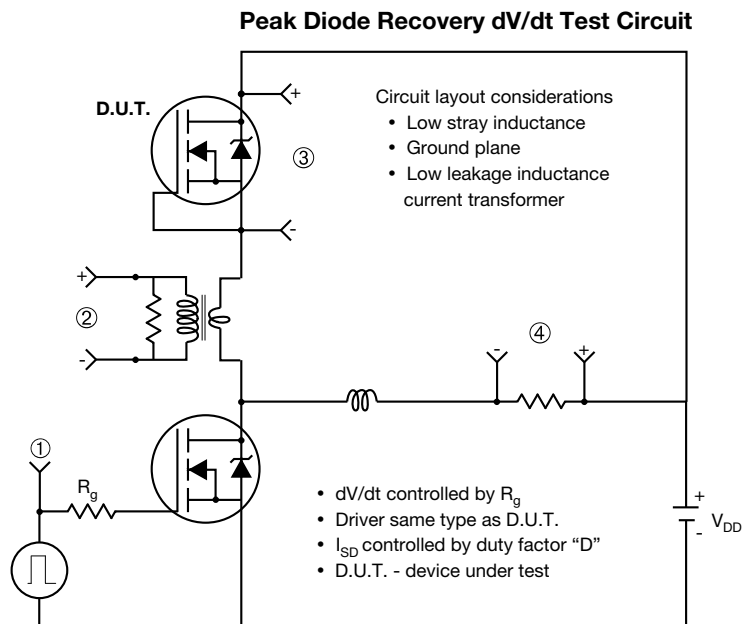


Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a -Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

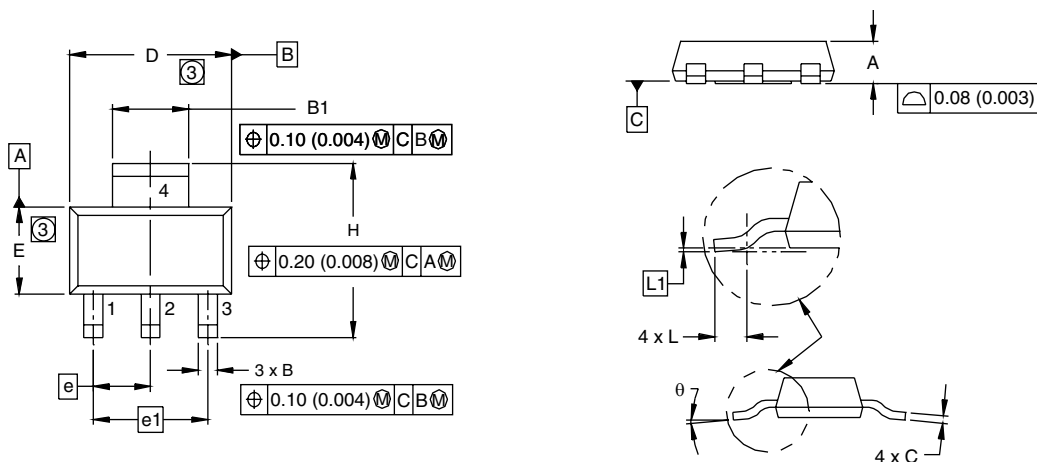

Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig.14 - For N-Channel

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SOT-223 (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|---|-------------|------|------------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 1.55 | 1.80 | 0.061 | 0.071 |
| B | 0.65 | 0.85 | 0.026 | 0.033 |
| B1 | 2.95 | 3.15 | 0.116 | 0.124 |
| C | 0.25 | 0.35 | 0.010 | 0.014 |
| D | 6.30 | 6.70 | 0.248 | 0.264 |
| E | 3.30 | 3.70 | 0.130 | 0.146 |
| e | 2.30 BSC | | 0.0905 BSC | |
| e1 | 4.60 BSC | | 0.181 BSC | |
| H | 6.71 | 7.29 | 0.264 | 0.287 |
| L | 0.91 | - | 0.036 | - |
| L1 | 0.061 BSC | | 0.0024 BSC | |
| θ | - | 10° | - | 10° |
| ECN: S-82109-Rev. A, 15-Sep-08 DWG: 5969 | | | | |

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.



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