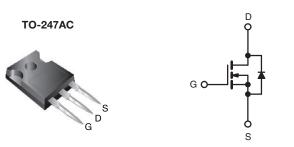
Vishay Siliconix

Power MOSFET



N-Channel MOSFET

PRODUCT SUMMARY				
V _{DS} (V) 400				
R _{DS(on)} (Ω)	V _{GS} = 10 V 0.30			
Q _g (Max.) (nC)	76			
Q _{gs} (nC)	20			
Q _{gd} (nC)	37			
Configuration	Single			

FEATURES

- Ultra low gate charge
- Reduced gate drive requirement
- Enhanced 30 V_{GS} rating
- Reduced C_{iss}, C_{oss}, C_{rss}
- Isolated central mounting hole
- Dynamic dV/dt rated
- Repetitive avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

This new series of low charge Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced MOSFETs technology the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability of MOSFETs offer the designer a new standard in power transistors for switching applications.

The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because of its isolated mounting hole.

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFP350LCPbF

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	400	V
Gate-source voltage		V_{GS}	± 30	7 °
Continuous drain current	V_{GS} at 10 V $T_C = 25 ^{\circ}C$	I-	16	
Continuous drain current V_{GS} at 10 V $T_{C} = 100 ^{\circ}\text{C}$		I _D	9.9	Α
Pulsed drain Current ^a		I _{DM}	64	
Linear derating factor			1.5	W/°C
Single pulse avalanche energy ^b		E _{AS}	390	mJ
Repetitive avalanche current a		I _{AR}	16	Α
Repetitive avalanche energy ^a		E _{AR}	19	mJ
Maximum power dissipation	T _C = 25 °C	P_{D}	190	W
Peak diode recovery dV/dt ^c	dV/dt	4.0	V/ns	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) d	for 10 s		300 ^d	
Mounting torque	6-32 or M3 screw		10	lbf ⋅ in
Woulding torque	0-02 of Wio sciew		1.1	N⋅m

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = 25 V, starting T_J = 25 °C, L = 2.7 mH, R_g = 25 Ω , I_{AS} = 16 A (see fig. 12)
- c. $I_{SD} \le 16$ A, $dI/dt \le 200$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C
- d. 1.6 mm from case



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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	40	
Case-to-sink, flat, greased surface	R _{thCS}	0.24	-	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	0.65	

SPECIFICATIONS (T _J = 25 $^{\circ}$ C, $_{\odot}$	nless otherw	rise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 2$	250 μΑ	400	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25	°C, I _D = 1 mA	-	0.49	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 1$	250 μΑ	2.0	-	4.0	V
Gate-source leakage	I _{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	$V_{DS} = 400 \text{ V}, V_{G}$		-	-	25	μA
			$_{S} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$	-	-	250	μ, ,
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 9.6 A ^b	-	-	0.30	Ω
Forward transconductance	9 _{fs}	$V_{DS} = 50 \text{ V}, I_{D} =$	9.6 A ^b	8.1	-	-	S
Dynamic							
Input capacitance	C_{iss}	V _{GS} = 0 V,		-	2200	-	
Output capacitance	C _{oss}	$V_{DS} = 25 \text{ V},$	V _{DS} = 25 V,		390	-	pF
Reverse transfer capacitance	C _{rss}	f = 1.0 MHz, see fig. 5		-	31	-	
Total Gate charge	Q_g			-	-	76	nC
Gate-source charge	Q_{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 16 \text{ A}, V_{DS} = 320 \text{ V}$ see fig. 6 and 13 b		-	20	
Gate-drain charge	Q _{gd}	1	occ lig. o and lo	-	-	37	1
Turn-on delay time	t _{d(on)}			-	14	-	ns ns
Rise time	t _r	$V_{DD} = 200 \text{ V}, I_{D}$	= 16 A,	-	54	-	
Turn-off delay time	t _{d(off)}	$R_g = 6.2 \Omega, R_D =$	= 12 Ω , see fig. 10 ^b	-	33	-	
Fall time	t _f	1		-	35	-	
Drain-Source Body Diode Characteristic	cs						
Continuous source-drain diode current	I _S	MOSFET symbo	ol	-	-	16	
Pulsed diode forward current ^a	I _{SM}	showing the integral reverse p - n junction diode		-	-	64	А
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 16 A, V _{GS} = 0 V ^b		-	-	1.6	V
Body diode reverse recovery time	t _{rr}	T 05.00 !	40 A .II/.II . 400 A / . b	-	440	660	ns
Body diode reverse recovery charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 16 \text{A}, dI/dt = 100 \text{A/} \mu \text{s}^{ \text{b}}$		-	4.1	6.2	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width $\leq 300~\mu s;~duty~cycle \leq 2~\%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

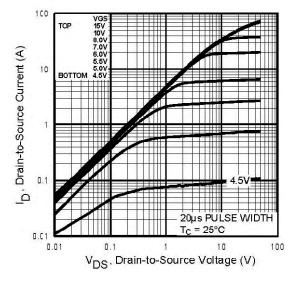


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

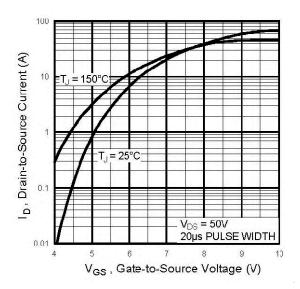


Fig. 3 - Typical Transfer Characteristics

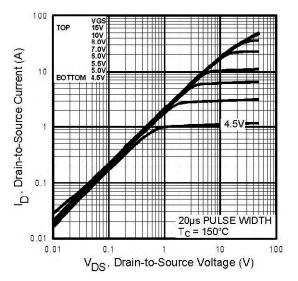


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

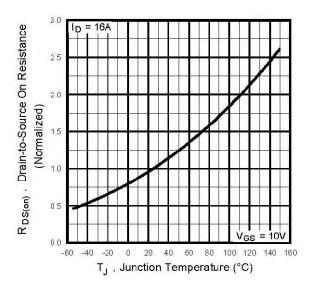


Fig. 4 - Normalized On-Resistance vs. Temperature



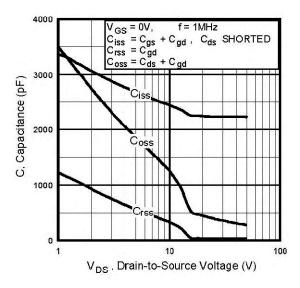


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

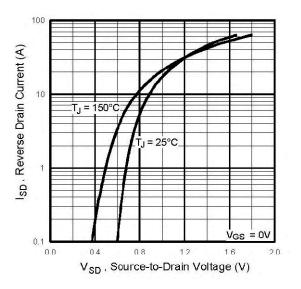


Fig. 7 - Typical Source-Drain Diode Forward Voltage

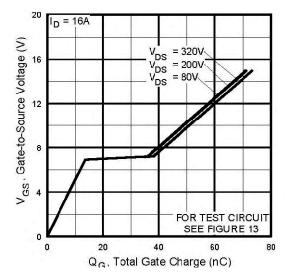


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

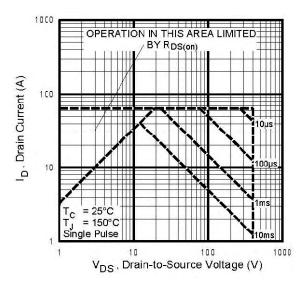


Fig. 8 - Maximum Safe Operating Area



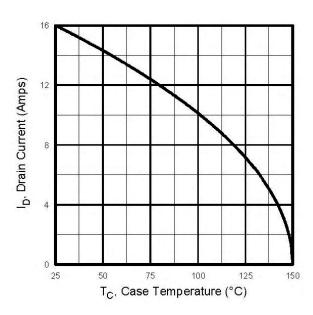


Fig. 9 - Maximum Drain Current vs. Case Temperature

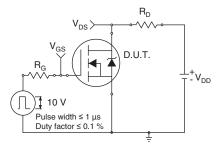


Fig. 10 - Switching Time Test Circuit

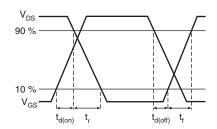


Fig. 11 - Switching Time Waveforms

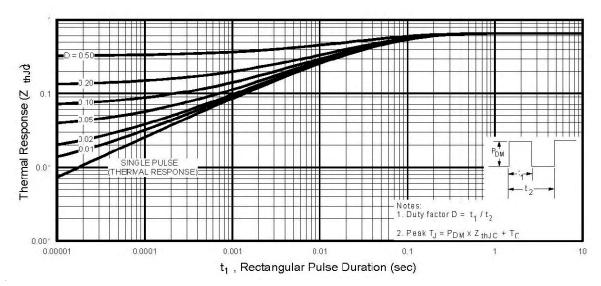


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



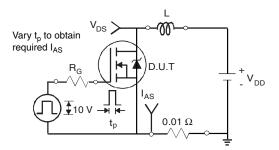


Fig. 13 - Unclamped Inductive Test Circuit

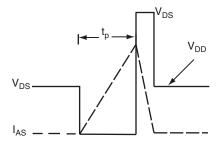


Fig. 14 - Unclamped Inductive Waveforms

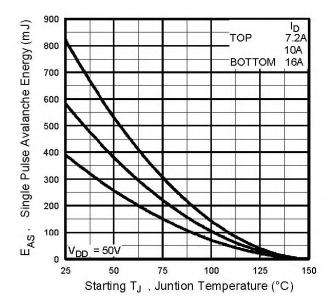


Fig. 15 - Maximum Avalanche Energy vs. Drain Current

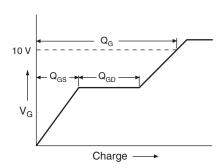


Fig. 16 - Basic Gate Charge Waveform

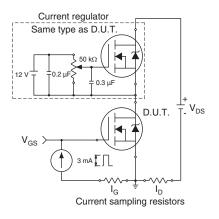
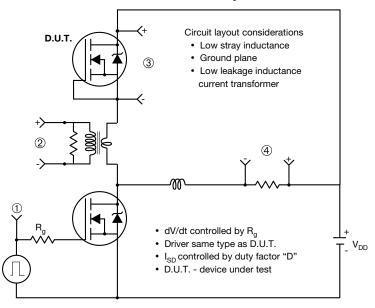


Fig. 17 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



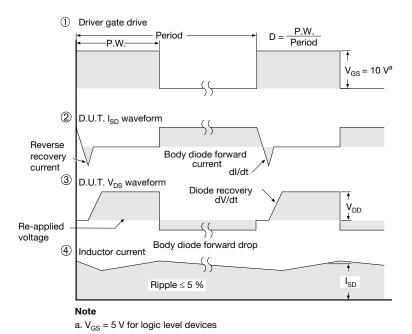


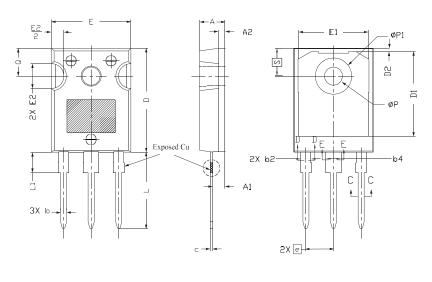
Fig. 18 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91224.



TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9







Section C--C,D-D,E-E

	MILLIMETERS				
DIM.	MIN.	NOM.	MAX.	NOTES	
Α	4.83	5.02	5.21		
A1	2.29	2.41	2.55		
A2	1.17	1.27	1.37		
b	1.12	1.20	1.33		
b1	1.12	1.20	1.28		
b2	1.91	2.00	2.39	6	
b3	1.91	2.00	2.34		
b4	2.87	3.00	3.22	6, 8	
b5	2.87	3.00	3.18		
С	0.40	0.50	0.60	6	
c1	0.40	0.50	0.56		
D	20.40	20.55	20.70	4	

	MILLIMETERS			
DIM.	MIN.	NOM.	MAX.	NOTES
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
Е	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
е		5.46 BSC		
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
ØΡ	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S		5.51 BSC		

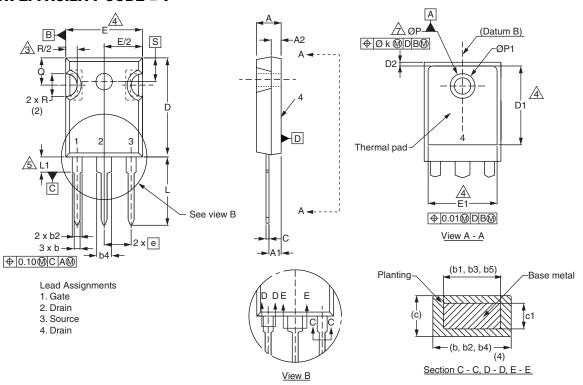
- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- $^{(7)}$ Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



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VERSION 2: FACILITY CODE = Y



	MILLIM		
DIM.	MIN.	MAX.	NOTES
Α	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
С	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

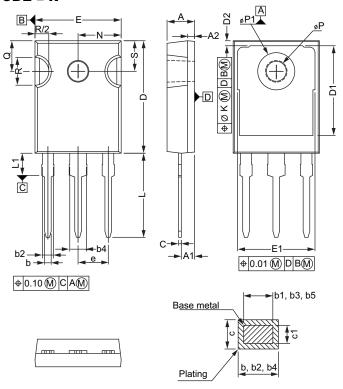
	MILLIN		
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
Е	15.29	15.87	
E1	13.72	-	
е	5.46	BSC	
Øk	0.2	254	
L	14.20	16.25	
L1	3.71	4.29	
ØР	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c

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VERSION 3: FACILITY CODE = N



	MILLIMETERS		
DIM.	MIN.	MAX.	
Α	4.65	5.31	
A1	2.21	2.59	
A2	1.17	1.37	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.65	2.39	
b3	1.65	2.34	
b4	2.59	3.43	
b5	2.59	3.38	
С	0.38	0.89	
c1	0.38	0.84	
D	19.71	20.70	
D1	13.08	-	

	MILLIMETERS		
DIM.	MIN.	MAX.	
D2	0.51	1.35	
E	15.29	15.87	
E1	13.46	-	
е	5.46	BSC	
k	0.254		
L	14.20	16.10	
L1	3.71	4.29	
N	7.62	BSC	
Р	3.56	3.66	
P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

ECN: E22-0452-Rev. G, 31-Oct-2022

DWG: 5971

- ⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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Vishay

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