

# Power MOSFET

**TO-220AB**


N-Channel MOSFET

## FEATURES

- Dynamic dV/dt rating
- 175 °C operating temperature
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

## DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

## PRODUCT SUMMARY

V <sub>DS</sub> (V)	60	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	0.10
Q <sub>g</sub> max. (nC)	25	
Q <sub>gs</sub> (nC)	5.8	
Q <sub>gd</sub> (nC)	11	
Configuration	Single	

## ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRFZ24PbF
Lead (Pb)-free and halogen-free	IRFZ24PbF-BE3

## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V <sub>DS</sub>	60	V
Gate-source voltage	V <sub>GS</sub>	± 20	
Continuous drain current	I <sub>D</sub>	T <sub>C</sub> = 25 °C	A
		T <sub>C</sub> = 100 °C	
Pulsed drain current <sup>a</sup>	I <sub>DM</sub>	68	
Linear derating factor		0.40	W/°C
Single pulse avalanche energy <sup>b</sup>	E <sub>AS</sub>	100	mJ
Maximum power dissipation	P <sub>D</sub>	60	W
Peak diode recovery dV/dt <sup>c</sup>	dV/dt	4.5	V/ns
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300	
Mounting torque	6-32 or M3 screw	10	
		1.1	N · m

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V<sub>DD</sub> = 25 V, starting T<sub>J</sub> = 25 °C, L = 403 μH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 17 A (see fig. 12)
- I<sub>SD</sub> ≤ 17 A, dI/dt ≤ 140 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 175 °C
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

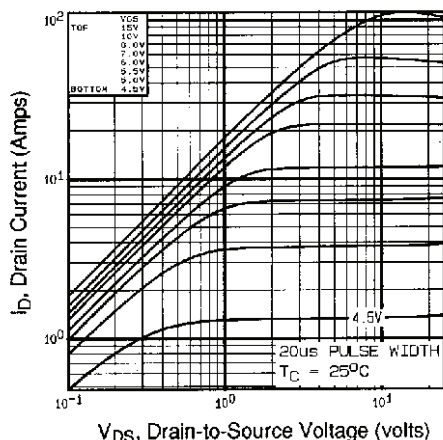
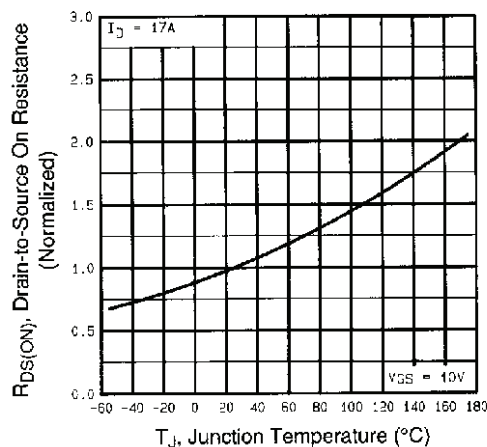
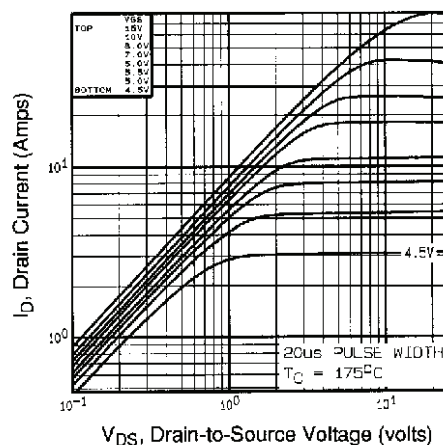
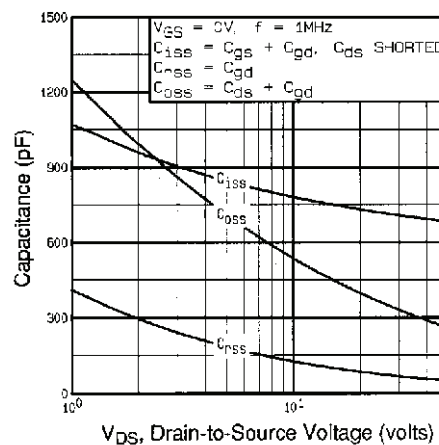
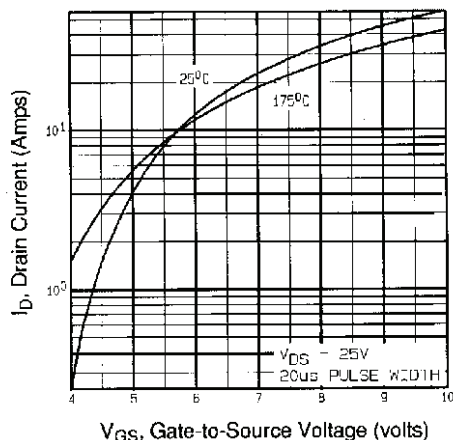
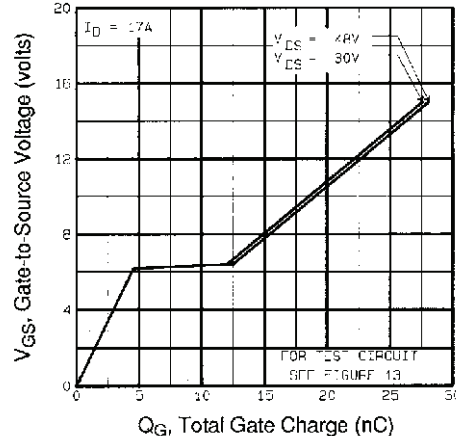
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	62	°C/W
Case-to-sink, flat, greased surface	$R_{thCS}$	0.50	-	
Maximum junction-to-case (drain)	$R_{thJC}$	-	2.5	

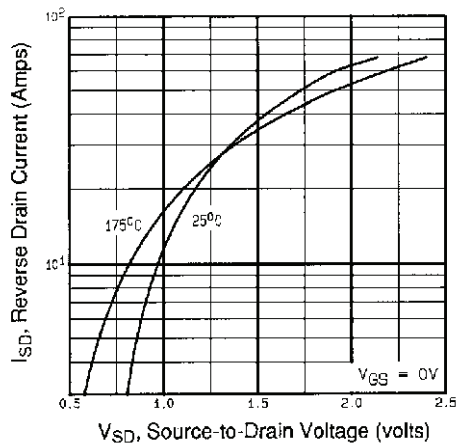
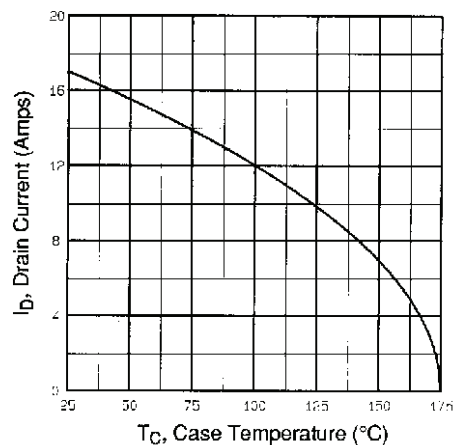
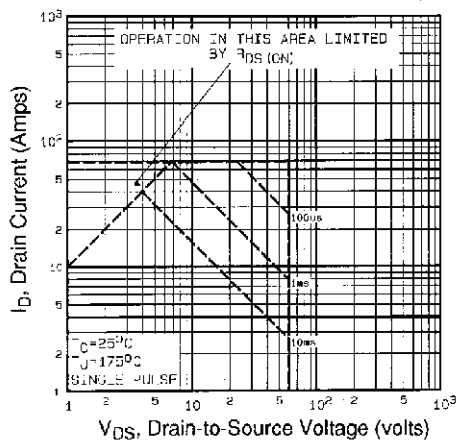
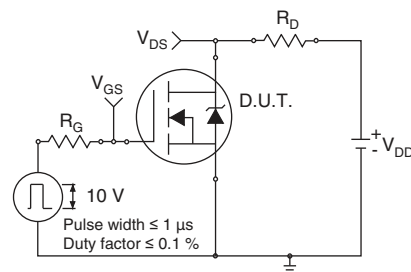
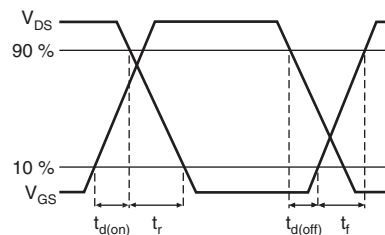
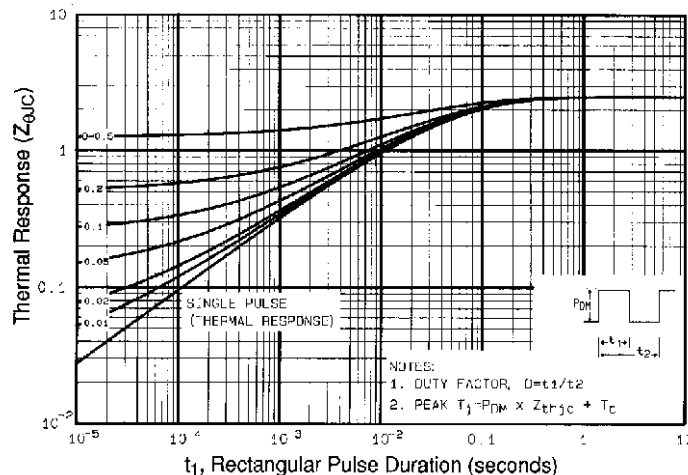
**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

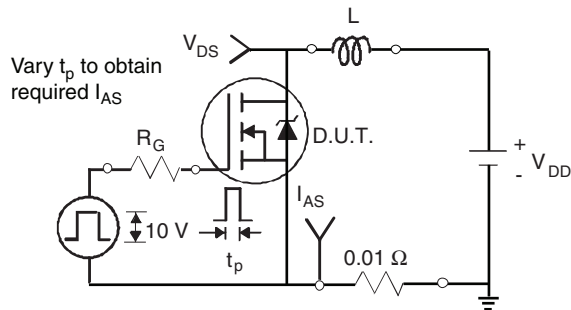
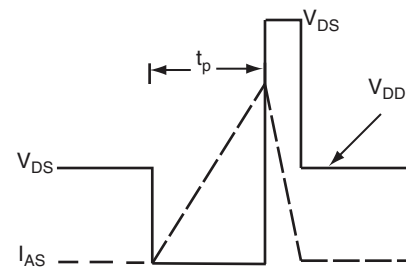
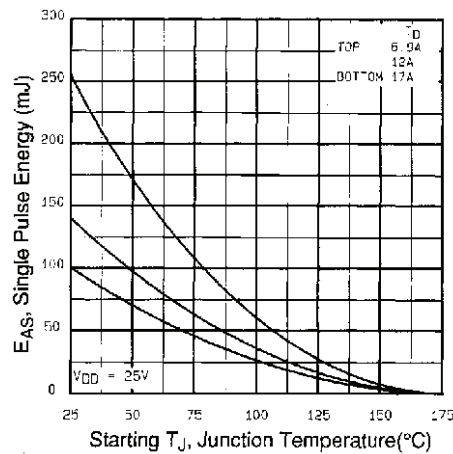
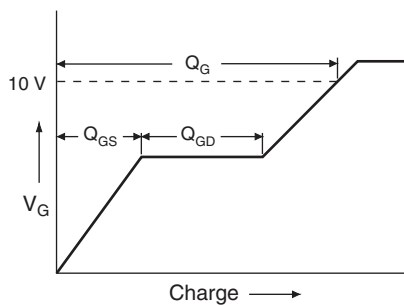
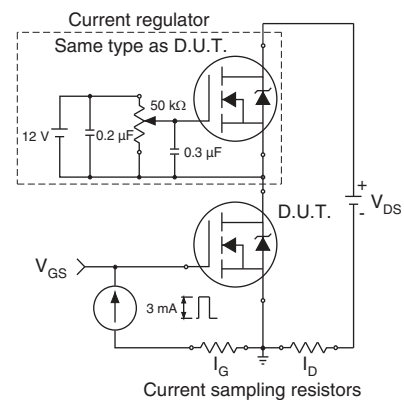
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$		60	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$ , $I_D = 1\text{ mA}$		-	0.061	-	V/ $^{\circ}\text{C}$
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 60\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 48\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 150\text{ }^{\circ}\text{C}$		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}^b$	-	-	0.10	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = 25\text{ V}$ , $I_D = 10\text{ A}$		5.5	-	-	S
Dynamic							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5		-	640	-	pF
Output capacitance	$C_{oss}$			-	360	-	
Reverse transfer capacitance	$C_{rss}$			-	79	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 17\text{ A}$ , $V_{DS} = 48\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	25	nC
Gate-source charge	$Q_{gs}$			-	-	5.8	
Gate-drain charge	$Q_{gd}$			-	-	11	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30\text{ V}$ , $I_D = 17\text{ A}$ , $R_g = 18\text{ }\Omega$ , $R_D = 1.7\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	13	-	ns
Rise time	$t_r$			-	58	-	
Turn-off delay time	$t_{d(off)}$			-	25	-	
Fall time	$t_f$			-	42	-	
Internal drain inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	$L_S$			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	17	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$			-	-	68	
Body diode voltage	$V_{SD}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_S = 17\text{ A}$ , $V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_F = 17\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$		-	88	180	ns
Body diode reverse recovery charge	$Q_{rr}$			-	0.29	0.64	$\mu\text{C}$
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

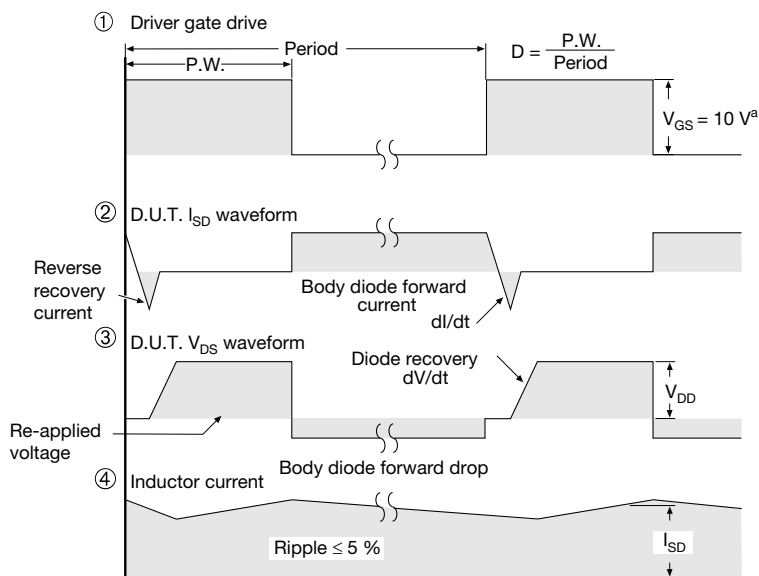
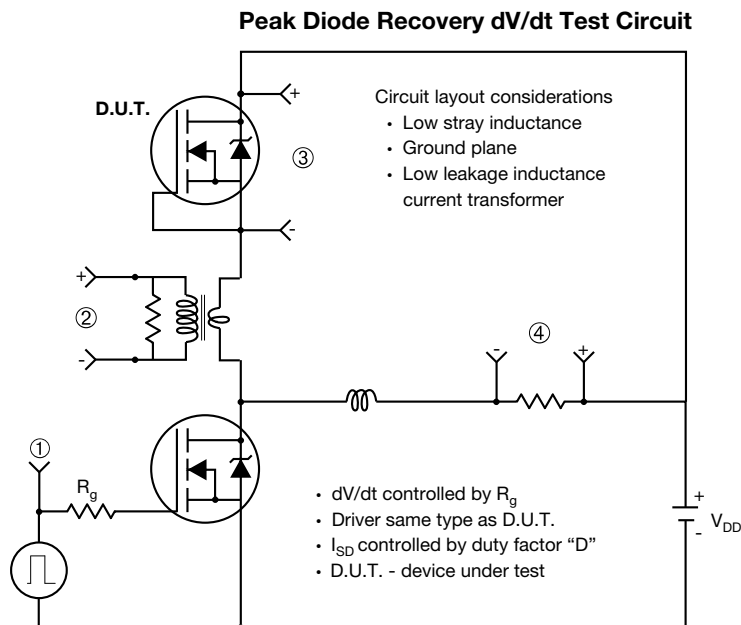
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics,  $T_C = 175^\circ\text{C}$** 

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

**Fig. 9 - Maximum Drain Current vs. Case Temperature**

**Fig. 8 - Maximum Safe Operating Area**

**Fig. 10a - Switching Time Test Circuit**

**Fig. 10b - Switching Time Waveforms**


**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig. 12a - Unclamped Inductive Test Circuit**

**Fig. 12b - Unclamped Inductive Waveforms**

**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

**Fig. 13a - Basic Gate Charge Waveform**

**Fig. 13b - Gate Charge Test**


**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

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