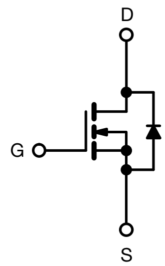
Power MOSFET

DPAK (TO-252)



N-Channel MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	50	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.20
Q_g (Max.) (nC)	10	
Q_{gs} (nC)	2.6	
Q_{gd} (nC)	4.8	
Configuration	Single	

FEATURES

- Low drive current
- Surface-mount
- Fast switching
- Ease of paralleling
- Excellent temperature stability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS
COMPLIANT

DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dV/dt capability.

The power MOSFET transistors also feature all of the well established advantages of MOSFET'S such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The DPAK (TO-252) surface-mount package brings the advantages of power MOSFET's to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR9012, SiHFR9012 is provided on 16 mm tape. The straight lead option IRFU9012, SiHFU9012 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, dc-to-dc converters, and a wide range of consumer products.

ORDERING INFORMATION				
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)
Lead (Pb)-free and halogen-free	SiHFR010-GE3	SiHFR010TR-GE3	SiHFR010TRL-GE3	IRFR010PbF-BE3
Lead (Pb)-free	IRFR010PbF	IRFR010TRPbF	IRFR010TRLPbF	IRFR010TRRPbF

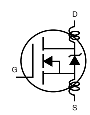
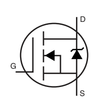
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	50	V
Gate-source voltage			V_{GS}	± 20	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	8.2	A
		T_C = 100 °C		5.2	
Pulsed drain current [a]			I_{DM}	33	
Avalanche current [b]			I_{AS}	1.5	
Linear derating factor				0.20	W/°C
Maximum power dissipation	T_C = 25 °C		P_D	25	W
Peak diode recovery dV/dt [c]			dV/dt	2.0	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d]	For 10 s			300	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 100 μH, R_g = 25 Ω
c. $I_{SD} \leq 8.2$ A, dI/dt ≤ 130 A/μs, $V_{DD} \leq 40$ V, $T_J \leq 150$ °C
d. 1.6 mm from case
e. When mounted on 1" square PCB (FR-4 or G-10 material)

THERMAL RESISTANCE RATINGS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	-	110	°C/W
Case-to-sink	R_{thCS}	-	1.7	-	
Maximum junction-to-case (drain)	R_{thJC}	-	-	5.0	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	50	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 500	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 50 V, V_{GS} = 0 V	-	-	250	μA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125 °C	-	-	1000	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 4.6 A[b]	-	0.16	0.20	Ω
Forward transconductance	g_{fs}	V_{DS} ≥ 50 V, I_D = 3.6 A	2.1	3.1	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 10	-	250	-	pF
Output capacitance	C_{oss}		-	150	-	
Reverse transfer capacitance	C_{rss}		-	29	-	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 7.3 A, V_{DS} = 40 V, see fig. 6 and 13[b]	-	6.7	10	nC
Gate-source charge	Q_{gs}		-	1.8	2.6	
Gate-drain charge	Q_{gd}		-	3.2	4.8	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 25 V, I_D = 7.3 A, R_g = 24 Ω, R_D = 3.3 Ω, see fig. 10[b]	-	11	17	ns
Rise time	t_r		-	33	50	
Turn-off delay time	$t_{d(off)}$		-	12	18	
Fall time	t_f		-	23	35	
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact[c] 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	8.2	A
Pulsed diode forward current [a]	I_{SM}		-	-	33	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 8.2 A, V_{GS} = 0 V[b]	-	-	1.6	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = 7.3 A, dI/dt = 100 A/μs[b]	41	86	190	ns
Body diode reverse recovery charge	Q_{rr}		0.15	0.33	0.78	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

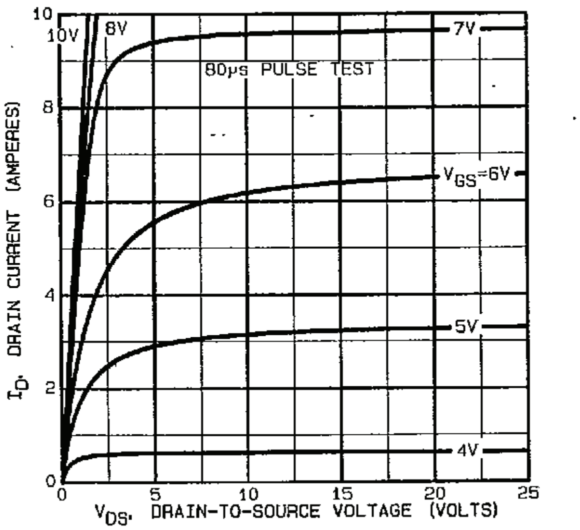


Fig. 1 - Typical Output Characteristics

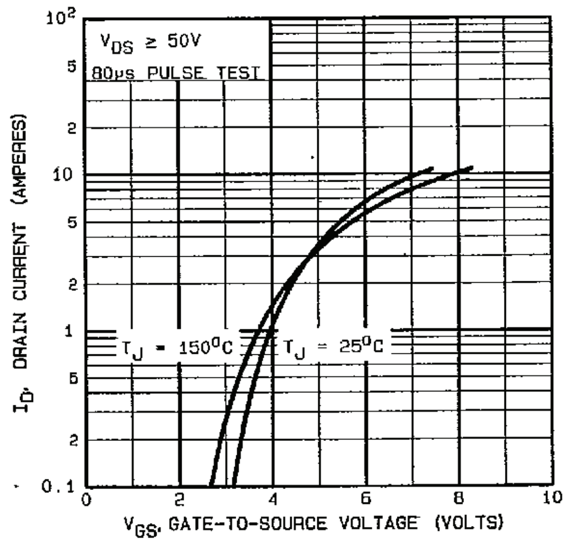


Fig. 2 - Typical Transfer Characteristics

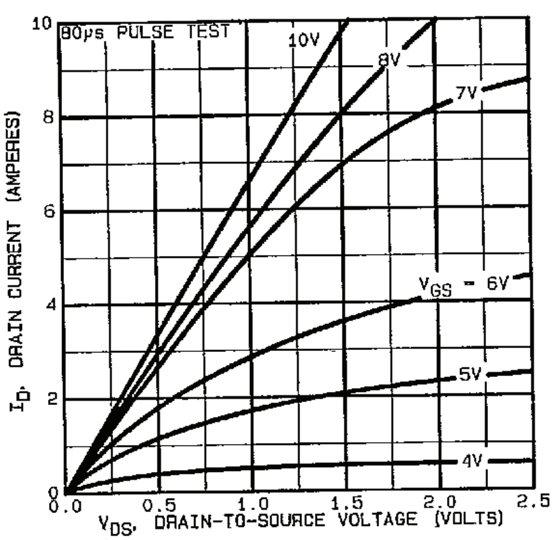


Fig. 1 - Typical Output Characteristics

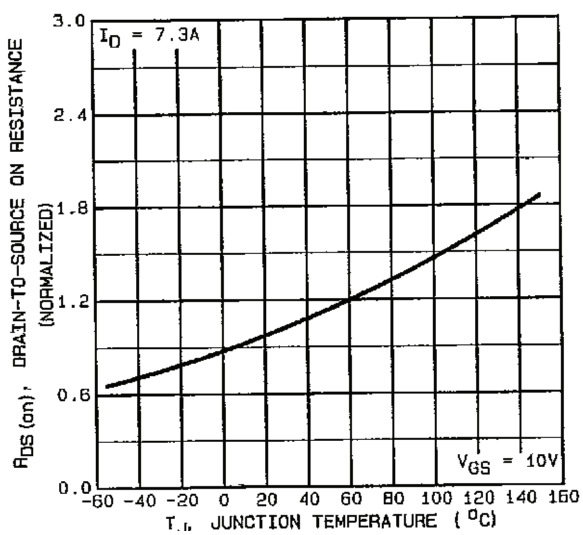


Fig. 3 - Normalized On-Resistance vs. Temperature

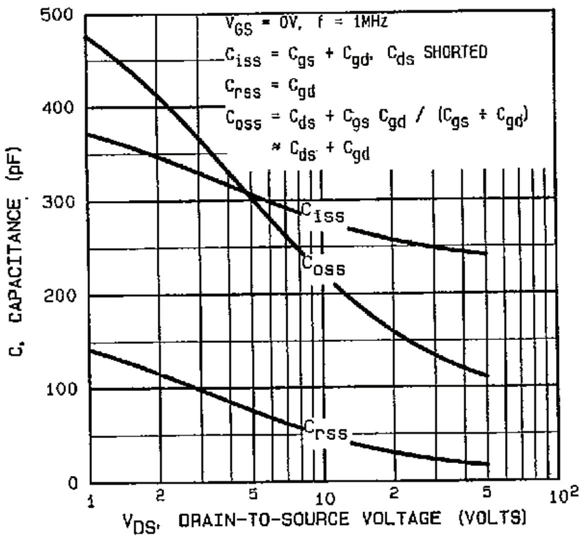


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

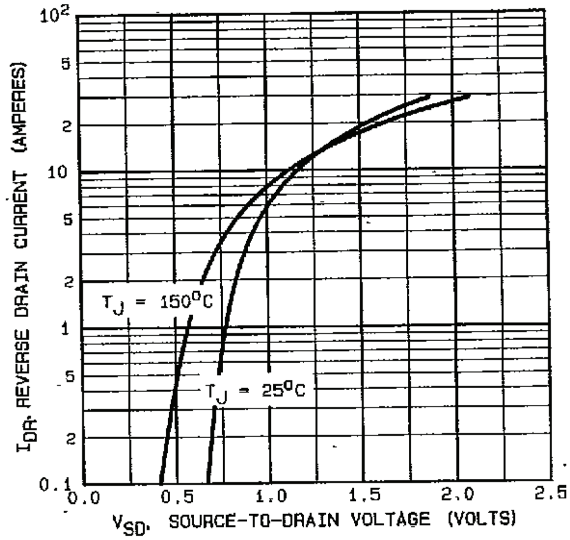


Fig. 6 - Typical Source-Drain Diode Forward Voltage

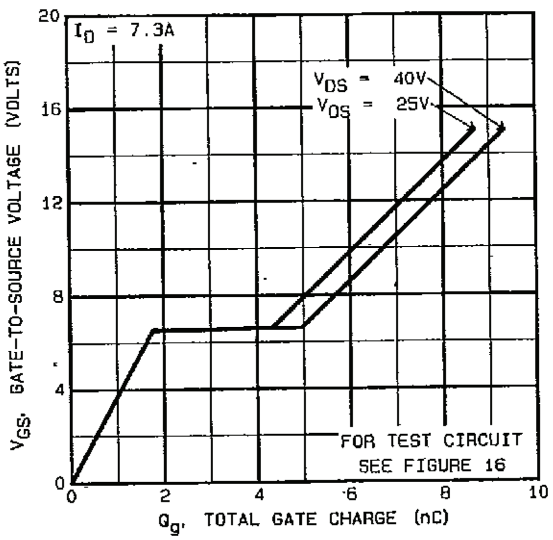


Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

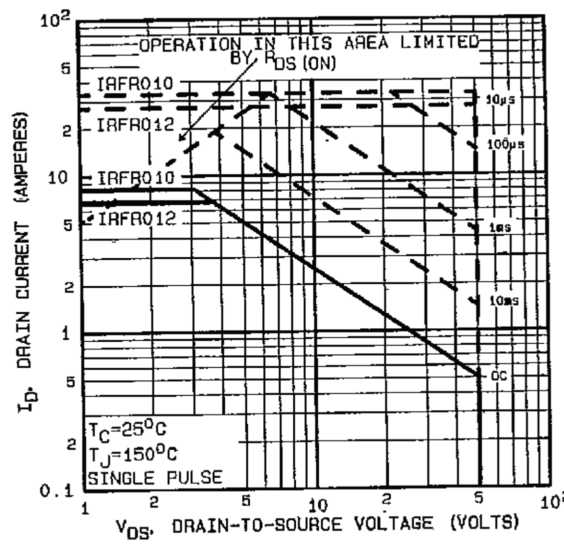


Fig. 7 - Maximum Safe Operating Area

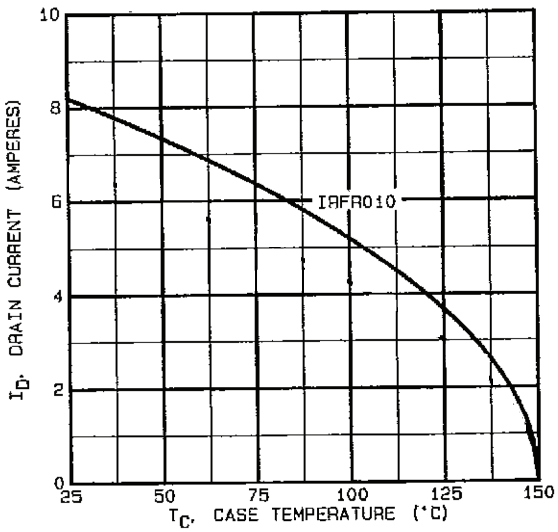


Fig. 8 - Maximum Drain Current vs. Case Temperature

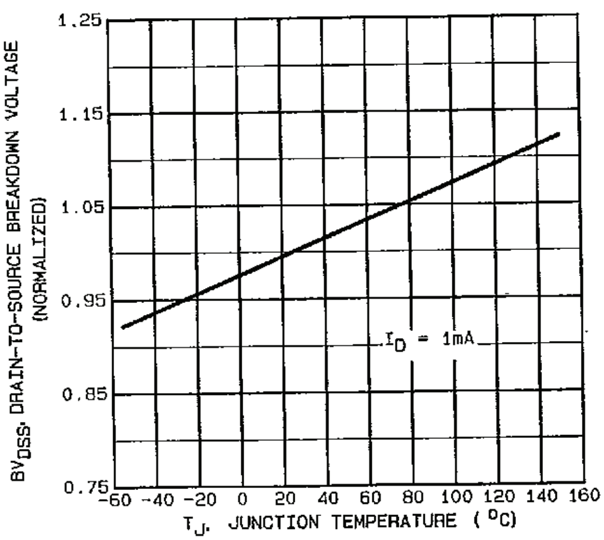


Fig. 9 - Breakdown Voltage vs. Temperature

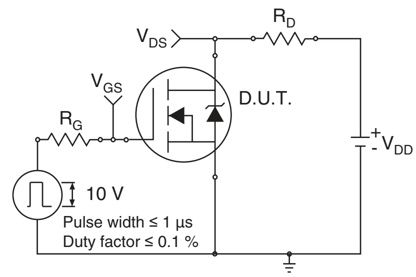


Fig. 10a - Switching Time Test Circuit

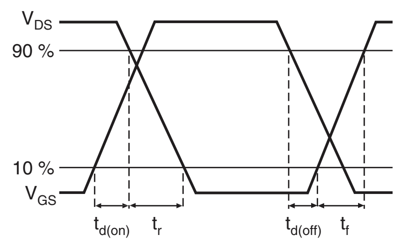


Fig. 10b - Switching Time Waveforms

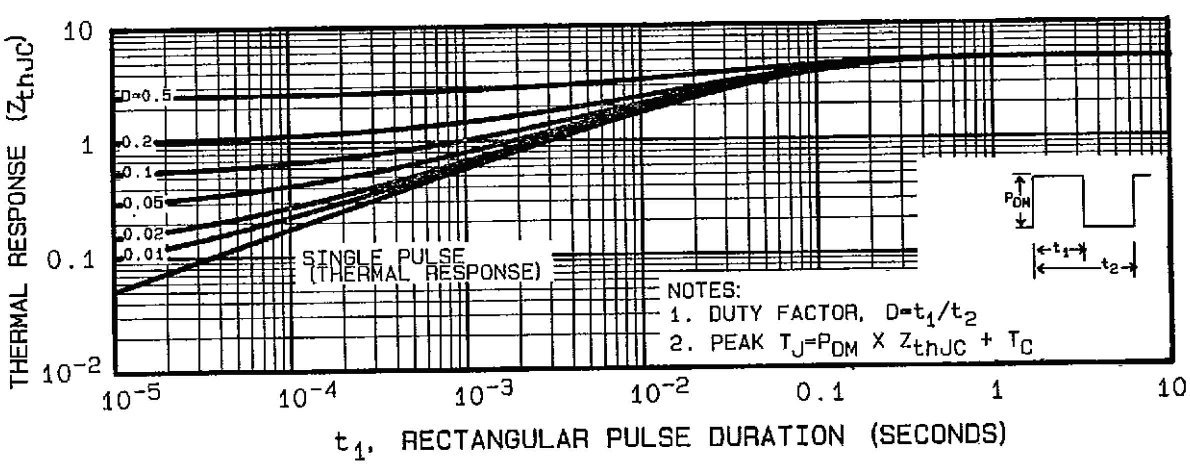


Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

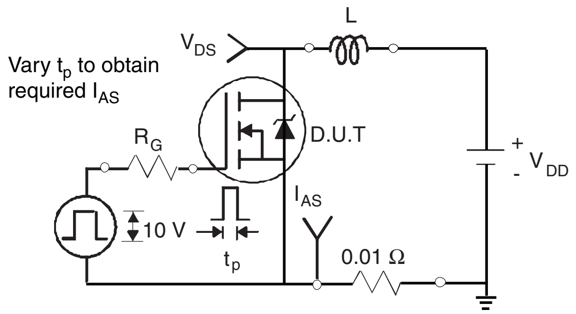


Fig. 12a - Unclamped Inductive Test Circuit

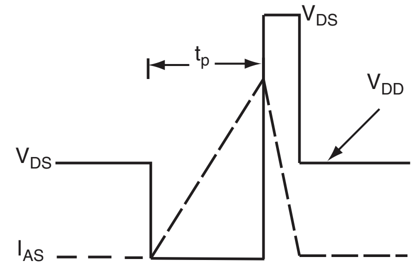


Fig. 12b - Unclamped Inductive Waveforms

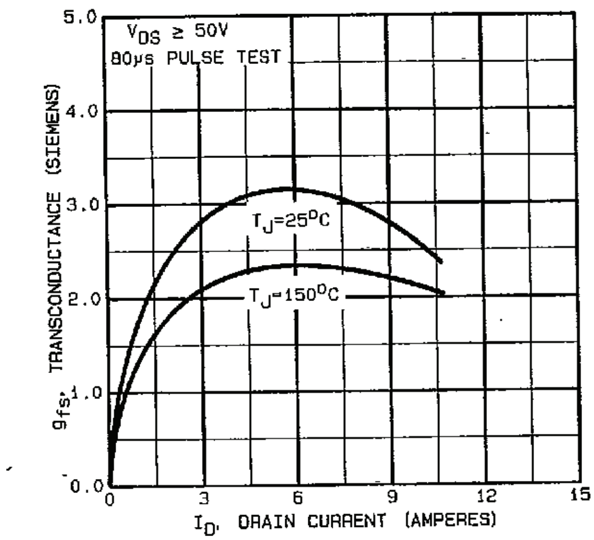


Fig. 12c - Typical Transconductance vs. Drain Current

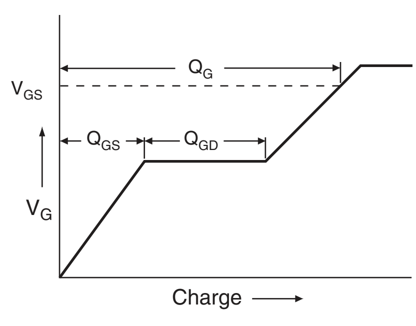


Fig. 13a - Basic Gate Charge Waveform

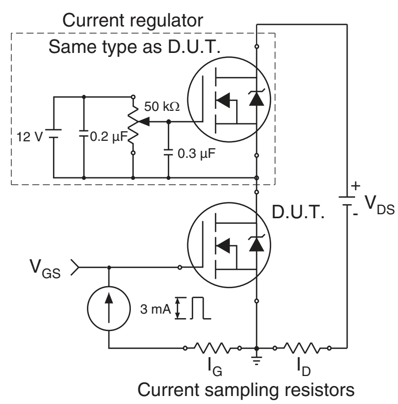
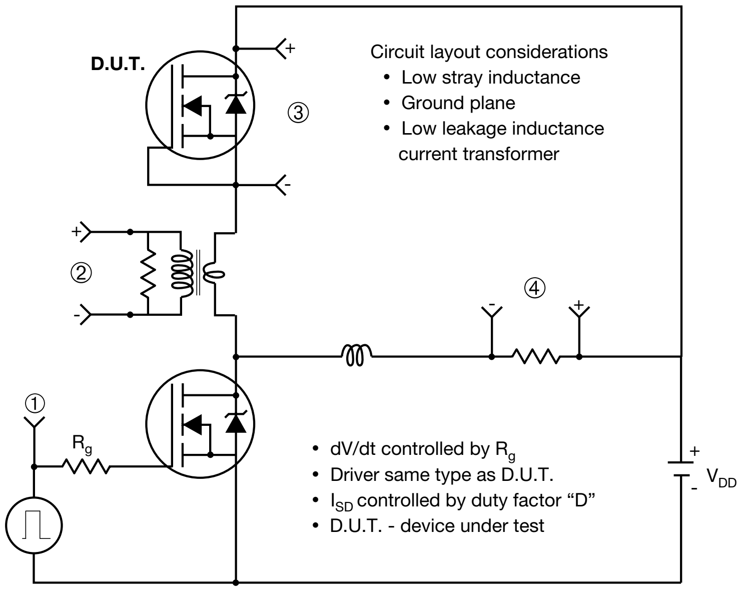
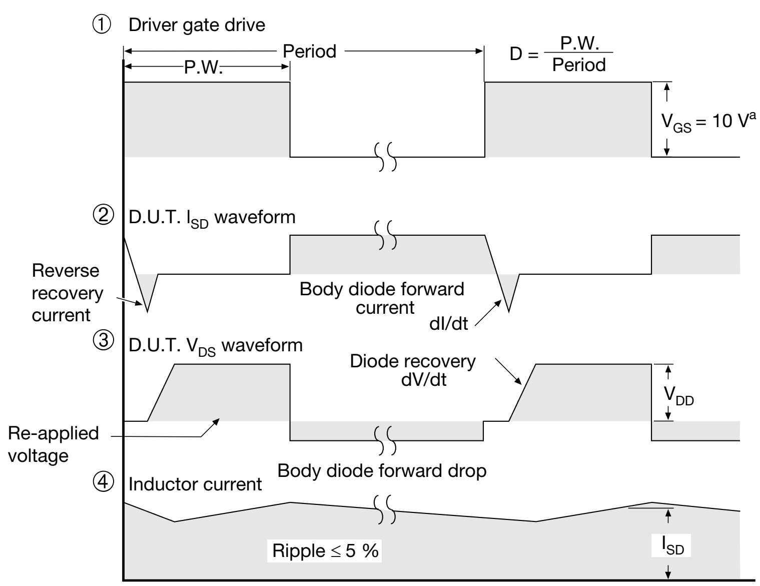


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





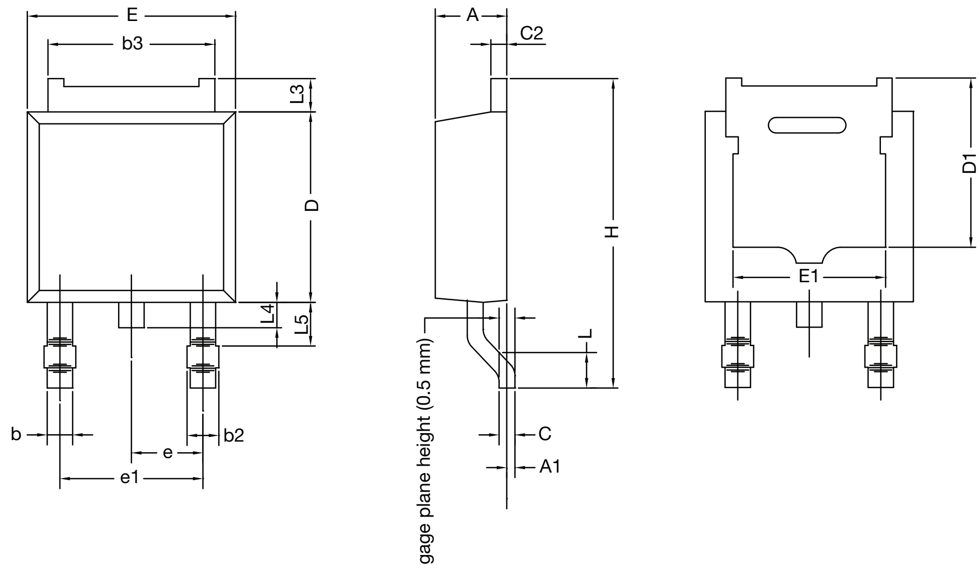
Note

a. V_{GS} = 5 V for logic level devices

Fig. 11 - For N-Channel

TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y

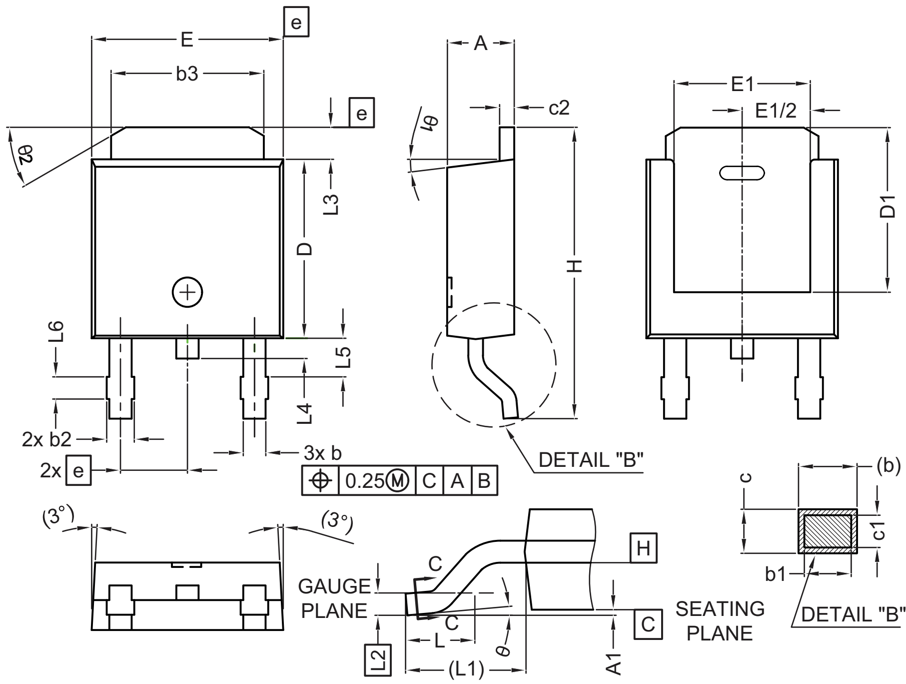


	MILLIMETERS	
DIM.	**MIN.**	**MAX.**
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only

VERSION 2: FACILITY CODE = N



	MILLIMETERS	
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

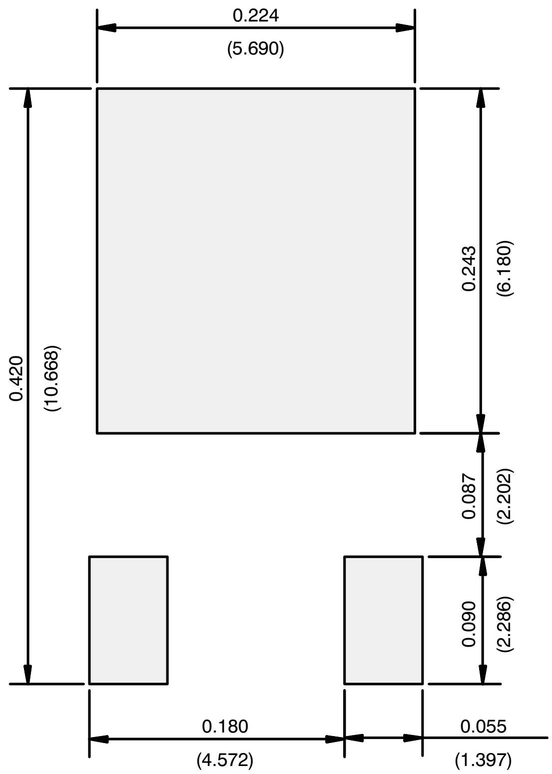
	MILLIMETERS	
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022
DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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