# Two-Switch Forward Converter: Operation, FOM, and MOSFET Selection Guide 

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The two-switch forward converter is a widely used topology and considered to be one of the most reliable converters ever. Its benefits include the following:

- Bullet proof operation: no timing issues or dead time requirements, and no chance of "shoot-through"
- No MOSFET body diode conduction under any condition
- No snubber circuitry required
- MOSFET voltage stress is limited to maximum supply voltage
- Simplicity of operation over a wide range of input voltages and load conditions
- Ability to handle multiple isolated outputs

A few drawbacks are:

- It is unable to do zero-voltage switching (ZVS), which limits its frequency of operation
- It requires two transistors and two fast recovery diodes
- Being a single ended converter, it requires a larger transformer and output inductor


## TWO-SWITCH FORWARD CONVERTER OPERATION

The two-switch forward converter is quite popular with ATX power supplies/silver boxes in the 150 W to 750 W output power levels and also competes with ZVS LLC topologies. It is a hard-switched topology and does not operate in ZVS mode. But for that very reason it has the benefit of having no body diode conduction. The input voltage seen by the MOSFETs used in this power range is the output voltage of a power factor correction (PFC) converter as required for any supply with an output power of equal to or greater than 65 W . This voltage is typically 380 V to 400 V . During turn-off, the MOSFETs may see an additional spike coming from leakage inductance energy, though it is clamped by the fast recovery diodes.
The basic operation is as follows. Fig. 1a shows transistors $Q_{1}$ and $Q_{2}$, which turn on together, transferring energy through the transformer primary into the secondary. On the secondary, the forward rectifying diode conducts, transferring the energy into the output filter and load.
When transistors $Q_{1}$ and $Q_{2}$ are turned off, the transformer magnetizing current flows through the now forward-biased diodes $D_{1}$ and $D_{2}$ and then back into the source as shown in fig. 1 b . The diodes conduct until all the magnetizing energy in the primary, along with the energy stored in the leakage inductances, is returned to the input supply. Since diodes $D_{1}$ and $D_{2}$ clamp the input voltage, no snubber circuit is required. Any overshoot beyond the input voltage needs to be managed with a proper circuit layout to minimize stray inductances. On the secondary, the freewheeling diode conducts as shown, transferring the output inductor energy to the load.
During the non-power delivery cycle of the primary, proper transformer reset time is achieved when the ON time is less than its OFF time (duty cycle is less than $50 \%$ ). In other words, the primary winding itself acts as the reset winding. Having the OFF time longer than the ON time will always reset the transformer.

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Fig. 1a) Power Transfer Stage of Operation


Fig. 1b) Power Flow from Output Cap to Power Load

## DUAL SWITCH VS. PFC CONVERTER, FOM, AND POWER LOSS

Fig. 2 compares power losses of the two-switch forward converter to the single switch PFC front-end converter in a 400 W power stage. The MOSFETs in the two-switch forward converter carry half the current, and switch at twice the frequency ( 125 kHz versus 65 kHz typical). With this doubling of the frequency, the switching losses become a more dominant factor in the overall figure of merit (FOM) and power loss measurement.


Fig. 2 Power Factor Correction Converter vs. a Two-Switch Forward Converter
To illustrate further, consider a TO-220 or TO-220F device with a maximum power loss of 8 W . Assume that this is an optimum choice for a PFC application. By "optimum" we mean that conduction losses are between $40 \%$ and $50 \%$ of the total losses at the rated power. But it does not follow that this would be an optimum solution a two-switch converter. In the two-switch topology the $\mathrm{C}_{\text {oss }} / \mathrm{Q}_{\text {oss }}$ and $\mathrm{Q}_{\mathrm{sw}}$ would contribute approximately $87 \%$ of the total losses and the remaining will be conduction losses. Such unbalance between conduction and switching losses is highly undesirable for efficiency and cost. Why are the conduction losses less than what would be seen in a single switch PFC converter? Because each MOSFET used will have half the current of a single-switch PFC circuit while switching at twice the frequency.

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In any switching circuit there are two kinds of switching losses. The first is due to the $V_{D S} \times I_{D S}$ crossover that happens during turn-on and turn-off. These losses are weighted to what we call " $Q_{s w}$," which is the combination of $Q_{g d}$ and the $Q_{g s}$, and represents the effective switching charge of the MOSFET. The crossover-related switching losses are a function of both load and switching frequency.
The second switching loss is that associated with charging and discharging of the MOSFET output capacitance $\mathrm{C}_{\text {oss. }}$. In ATX power supplies, the popular two-switch forward converter follows the PFC converter having an input voltage $\sim 400 \mathrm{~V}$. As a result, the output switching loss can be a significant portion of the total losses. The $\mathrm{C}_{\text {oss }} / \mathrm{Q}_{\mathrm{oss}}$ of the device is a very important loss, especially at light loads where switching losses trump conduction losses. This loss is essentially independent of load and $Q_{o s s}$, which along with $Q_{s w}$ needs to be taken into account when selecting the appropriate MOSFET. An application-specific FOM based on loss contributions will look like:

Conduction losses $\left(\mathbf{R}_{\mathrm{DS}(o n)}\right)+$ Switching losses $\left(\mathrm{Q}_{\text {switch }}\right)+$ Output losses $\left(\mathrm{Q}_{\text {oss }}\right)$

The $\mathrm{C}_{\text {oss }}$ of a high-voltage MOSFET varies considerably with the applied $\mathrm{V}_{\mathrm{DS}}$. This variation is much wider for high-voltage Super Junction power MOSFETs (fig. 3a) than for planar types (fig. 3b). To account for the non-linearity of the output capacitor, $P_{\text {oss }}=1 / 2 C_{o(e r)} \times \mathrm{V}^{2} \times \mathrm{F}_{\text {sw }}$ may be used as an approximate loss equation. The energy related capacitance $\mathrm{C}_{\mathrm{o}}$ (er) is the effective capacitance that has the same stored energy and same losses as the integrated $\mathrm{C}_{\text {oss }}$ of the MOSFET ( 0 V to $\mathrm{V}_{\mathrm{DS}}$ ) and is provided in product datasheets. Note that the inclusion of output capacitor related losses as part of the FOM, in addition to the conduction and switching losses, is a Vishay innovation that has yet to become a standard for the industry.


Fig. 3a) Super Junction Technology Capacitive Plot


Fig. 3b) Planar Technology Capacitive Plot

With this enhanced FOM in mind, and to help our customers develop the most efficient design possible, we have developed a list of components aimed at achieving the highest efficiency for a two-switch forward converter based on typical operating conditions. Each MOSFET has a target loss of less than $0.5 \%$ of the total converter loss. So, for a 400 W ATX power supply, the losses would be no more than 2 W per device. Table 1 illustrates operating conditions assumed for such a power supply.

## TABLE 1 - TWO-SWITCH FORWARD CONVERTER OPERATING CONDITIONS

| Input Voltage | 400 V |  |
| :--- | :---: | :---: |
| Input Power | 450 W |  |
| PFC Switching Frequency | 125 kHz |  |
| Duty Cycle | $3 / 8$ |  |
| MOSFET Drive Voltage | 12 V |  |
| On/Off Gate Current Range | $0.5 \mathrm{~A} \mathrm{(100} \mathrm{W)} \mathrm{to} 1 \mathrm{~A} \mathrm{(750} \mathrm{W)}$ |  |
|  |  |  |
| Revision: 14-Jan-14 | $\mathbf{3}$ |  |

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The list of recommended devices includes an " $x$ " in the "Package" location. For the same set of electrical characteristics, a number of package options may be available per device. The packages used will depend on the power level as well as what MOSFET real estate is allowed.
Fig. 4 defines the packages, current rating, voltage, and device technology of the different part numbers ${ }^{(1)}$

## Note

${ }^{(1)}$ Definition: Vishay High Voltage MOSFET Part Number: SiHxDDNFFG


Fig. 4 Part Numbers Definition
With many package options available, table 2 lists the recommended maximum power rating for the different package offerings.

| TABLE 2 - RECOMMENDED POWER LEVELS BASED ON PACKAGE TYPE |  |
| :--- | :---: |
| PACKAGES | RECOMMENDED MAXIMUM RATINGS |
| DPAK (TO-252) / IPAK | up to 150 W |
| D2PAK (TO-263) / TO-220 | up to 200 W |
| TO-220 | up to 350 W |
| TO-220F/Thin Lead TO-220F | up to 350 W |
| TO-247AC | up to 1000 W |
| Super TO-247 | up to 1500 W |

With the design conditions, device part number understanding, and maximum recommended per package type, table 3 shows the respective devices for the different power levels.
This list shows many different devices. Depending on whether voltage, efficiency, or price is a higher concern, you can pick and

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| OUTPUT POWER |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 100 W | 125 W to 250 W | 275 W | 300W | 325 W | 350 W to 450 W | 475 W to 575 W | 600 W to 750 W |
| 500 V | 500 V | 500 V | 500 V | 500 V | 500 V | 500 V | 500 V |
| SiHx8N50D | SiHx8N50D | SiHx8N50C | SiHx8N50D | SiHx14N50D | SiHx14N50D | SiHS20N50C | SiHx25N50E ${ }^{(1)}$ |
| SiHx5N50D | SiHx12N50C | SiHx16N50C | SiHx14N50C | SiHx16N50C | SiHS20N50C | SiHx14N50D | SiHF18N50D |
| OUTPUT POWER |  |  |  |  |  |  |  |
| 100 W to 250 W |  | 275 W to 450 W |  | 475 W to 725 W |  | 750 W |  |
| 600 V |  | 600 V |  | 600 V |  | 600 V |  |
| SiHx7N60E |  | SiHx12N60E |  | SiHx12N60E |  | SiHx23N60E |  |
| SiHx12N60E |  | SiHx15N60E ${ }^{(2)}$ |  | SiHx15N60E |  | SiHx15N60E |  |
| OUTPUT POWER |  |  |  |  |  |  |  |
| 100 W to 300 W |  | 325 W to 550 W |  | 475 W to 750 W |  | - |  |
| 650 V |  | 650 V |  | 650 V |  | - |  |
| SiHx6N65E |  | SiHx12N65E |  | SiHx12N65E |  | - |  |
| SiHx12N65E |  | $\mathrm{SiHx15N65E}{ }^{(3)}$ |  | SiHx15N65E |  | - |  |

Table 3: Device selection tool based on PFC output power levels

## Notes

- Devices with "x" can use multiple packages; 500 V devices use conventional planar technology, whereas the 600 V and 650 V devices are built on Super Junction technology.
${ }^{(1)}$ This is our first 500 V superjunction device that will be sampling in Q2/2014
(2) For a lower cost solution, try the $\mathrm{SiH} \times 7 \mathrm{~N} 60 \mathrm{E}$ as the performance should be similar
${ }^{(3)}$ For a lower cost solution, try the SiHx 6 N 65 E as the performance should be similar

