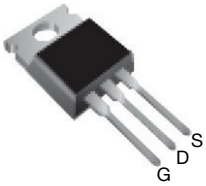
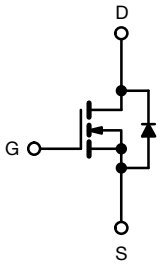
E Series Power MOSFET

TO-220AB





N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM): R_{on} x Q_g
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

HALOGEN FREE Available

APPLICATONS

- Hard switched topologies
- Power factor correction power supplies (PFC)
- Switch mode power supplies (SMPS)
- Computing
  - PC silver box / ATX power supplies
- Lighting
  - Two stage LED lighting

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. at 25 °C (Ω)	V_{GS} = 10 V	0.145
Q_g (Max.) (nC)	86	
Q_{gs} (nC)	14	
Q_{gd} (nC)	25	
Configuration	Single	

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free and halogen-free	SiHP25N50E-BE3 [a]
	SiHP25N50E-GE3

Note

a. "-BE3" denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-source voltage			V_{DS}	500	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	26	A
		T_C = 100 °C		16	
Pulsed drain current [a]			I_{DM}	50	
Linear derating factor				0.2	W/°C
Single pulse avalanche energy [b]			E_{AS}	273	mJ
Maximum power dissipation			P_D	250	W
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	T_J = 125 °C		dV/dt	65	V/ns
Reverse diode dV/dt [d]				25	
Soldering recommendations (peak temperature) [c]	For 10 s			300	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 4.4 A
c. 1.6 mm from case
d. $I_{SD} \leq I_D$, dI/dt = 100 A/µs, starting T_J = 25 °C

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THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.5	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	500	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.59	-	V/°C
Gate-source threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
		V_{GS} = ± 30 V	-	-	± 1	µA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	25	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 12 A	-	0.125	0.145	Ω
Forward transconductance	g_{fs}	V_{DS} = 30 V, I_D = 12 A	-	6.6	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	1980	-	pF
Output capacitance	C_{oss}		-	105	-	
Reverse transfer capacitance	C_{rss}		-	8	-	
Effective output capacitance, energy related [a]	$C_{o(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	105	-	
Effective output capacitance, time related [b]	$C_{o(tr)}$		-	285	-	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 12 A, V_{DS} = 400 V	-	57	86	nC
Gate-source charge	Q_{gs}		-	14	-	
Gate-drain charge	Q_{gd}		-	25	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 400 V, I_D = 12 A, R_g = 9.1 Ω, V_{GS} = 10 V	-	19	38	ns
Rise time	t_r		-	36	72	
Turn-off delay time	$t_{d(off)}$		-	57	86	
Fall time	t_f		-	29	58	
Gate input resistance	R_g	f = 1 MHz, open drain	-	0.56	-	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	12	A
Pulsed diode forward current	I_{SM}		-	-	50	
Diode forward voltage	V_{SD}	T_J = 25 °C, I_S = 16.5 A, V_{GS} = 0 V	-	-	1.2	V
Reverse recovery time	t_{rr}	T_J = 25 °C, I_F = I_S, dI/dt = 100 A/µs, V_R = 25 V	-	338	-	ns
Reverse recovery charge	Q_{rr}		-	5.3	-	µC
Reverse recovery current	I_{RRM}		-	29	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

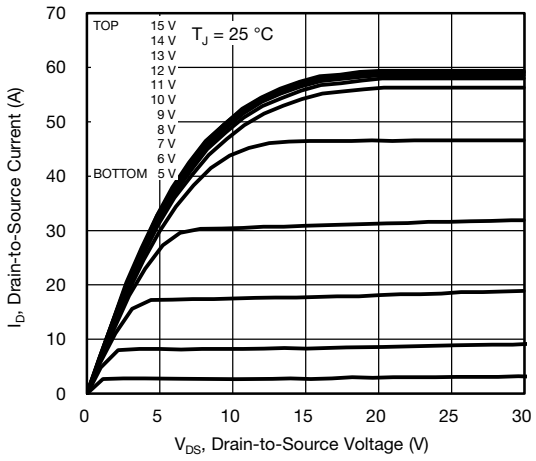


Fig. 1 - Typical Output Characteristics

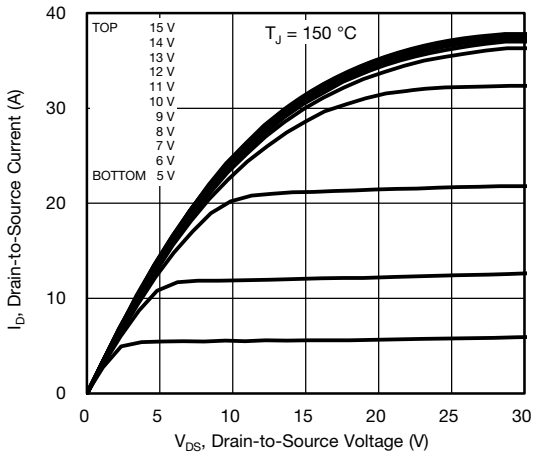


Fig. 2 - Typical Output Characteristics

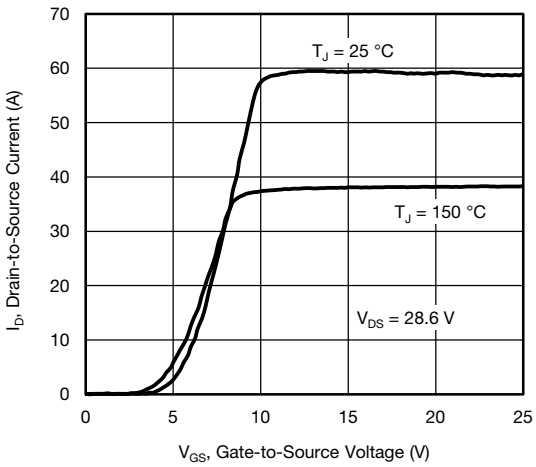


Fig. 3 - Typical Transfer Characteristics

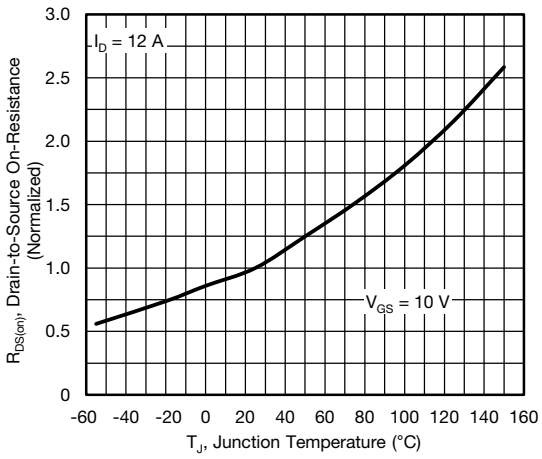


Fig. 4 - Normalized On-Resistance vs. Temperature

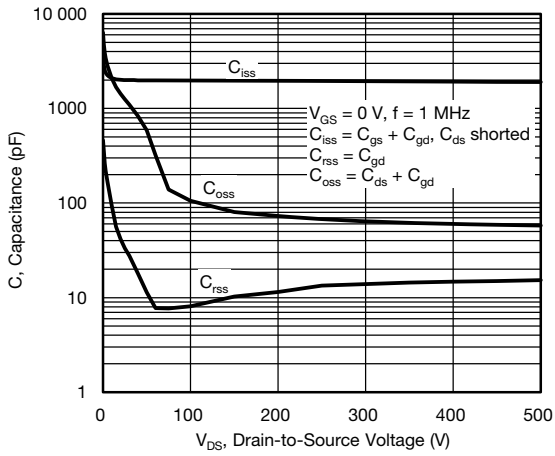


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

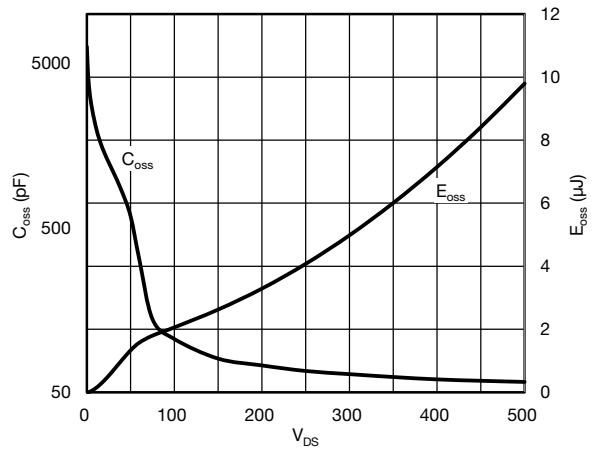


Fig. 6 - C_{OSS} and E_{OSS} vs. V_{DS}

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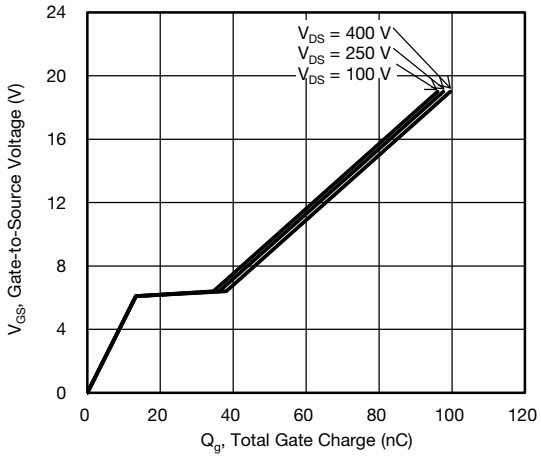


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

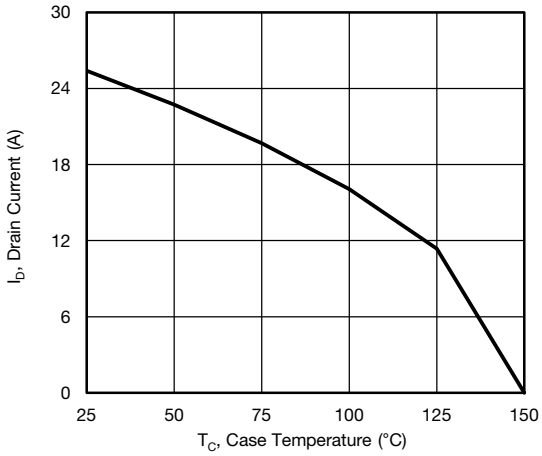


Fig. 10 - Maximum Drain Current vs. Case Temperature

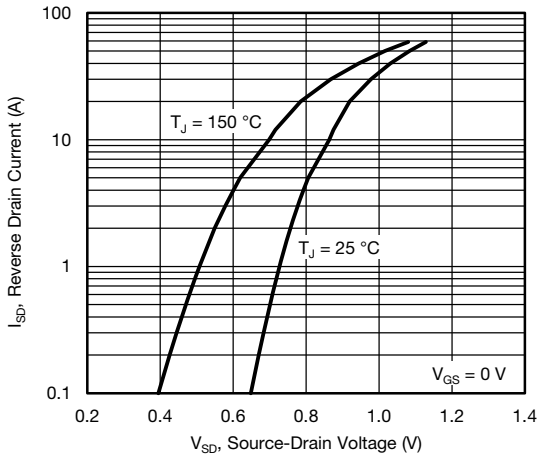


Fig. 8 - Typical Source-Drain Diode Forward Voltage

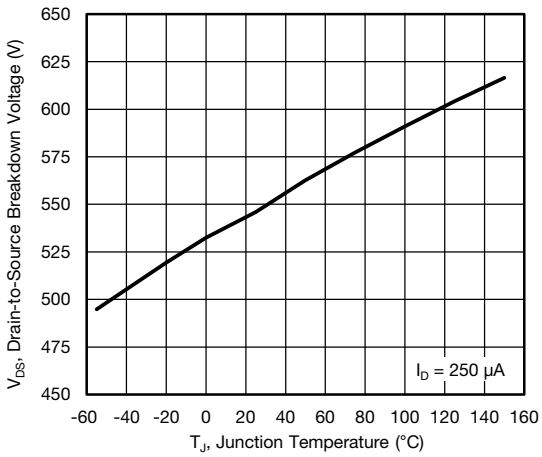


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature

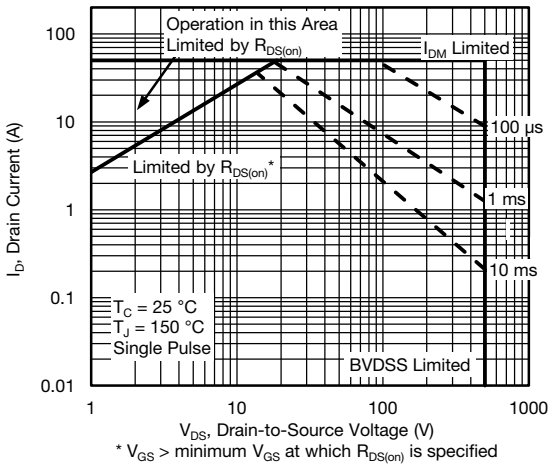


Fig. 9 - Maximum Safe Operating Area

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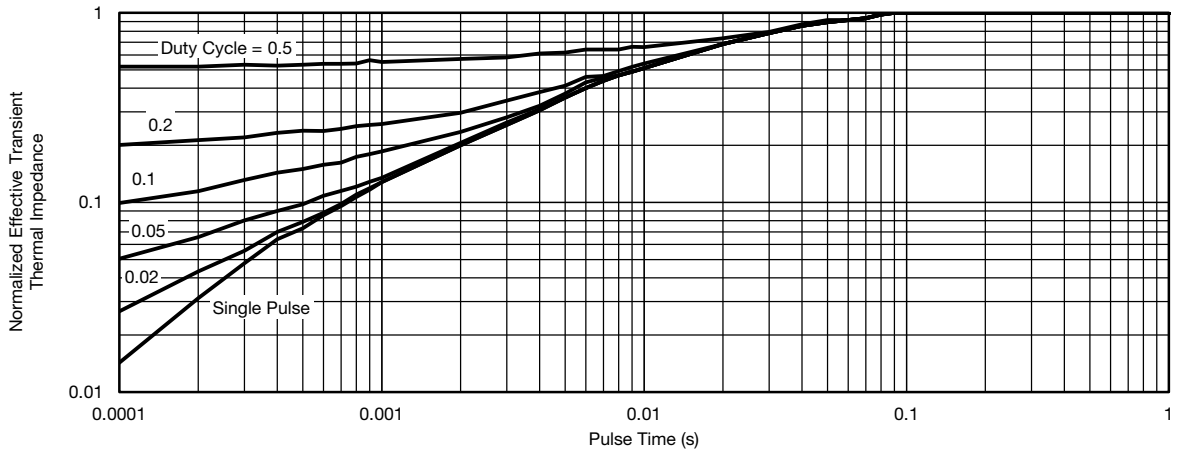


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

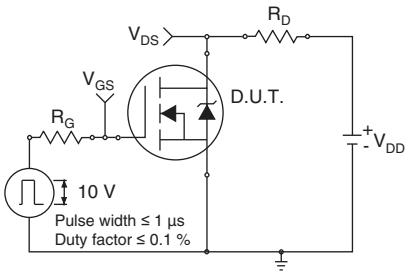


Fig. 13 - Switching Time Test Circuit

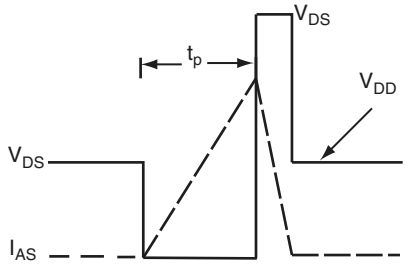


Fig. 16 - Unclamped Inductive Waveforms

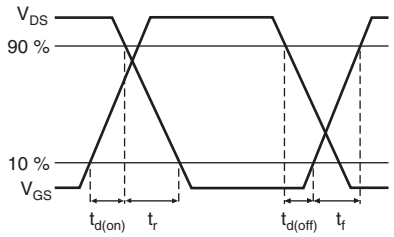


Fig. 14 - Switching Time Waveforms

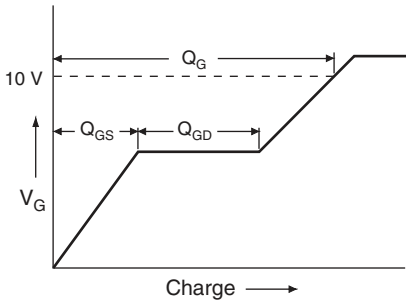


Fig. 17 - Basic Gate Charge Waveform

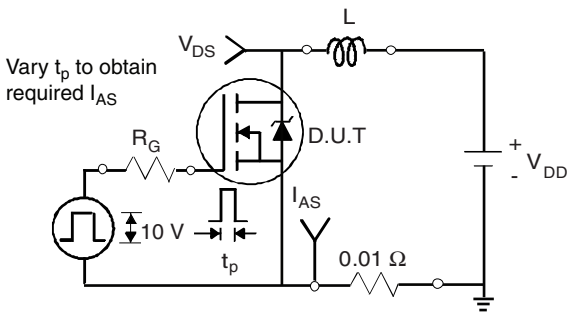


Fig. 15 - Unclamped Inductive Test Circuit

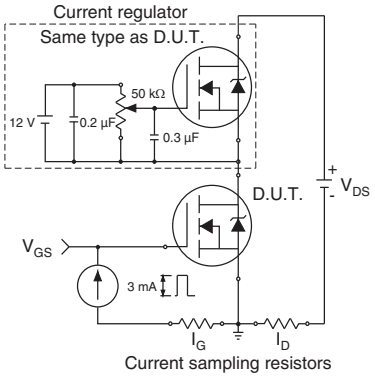
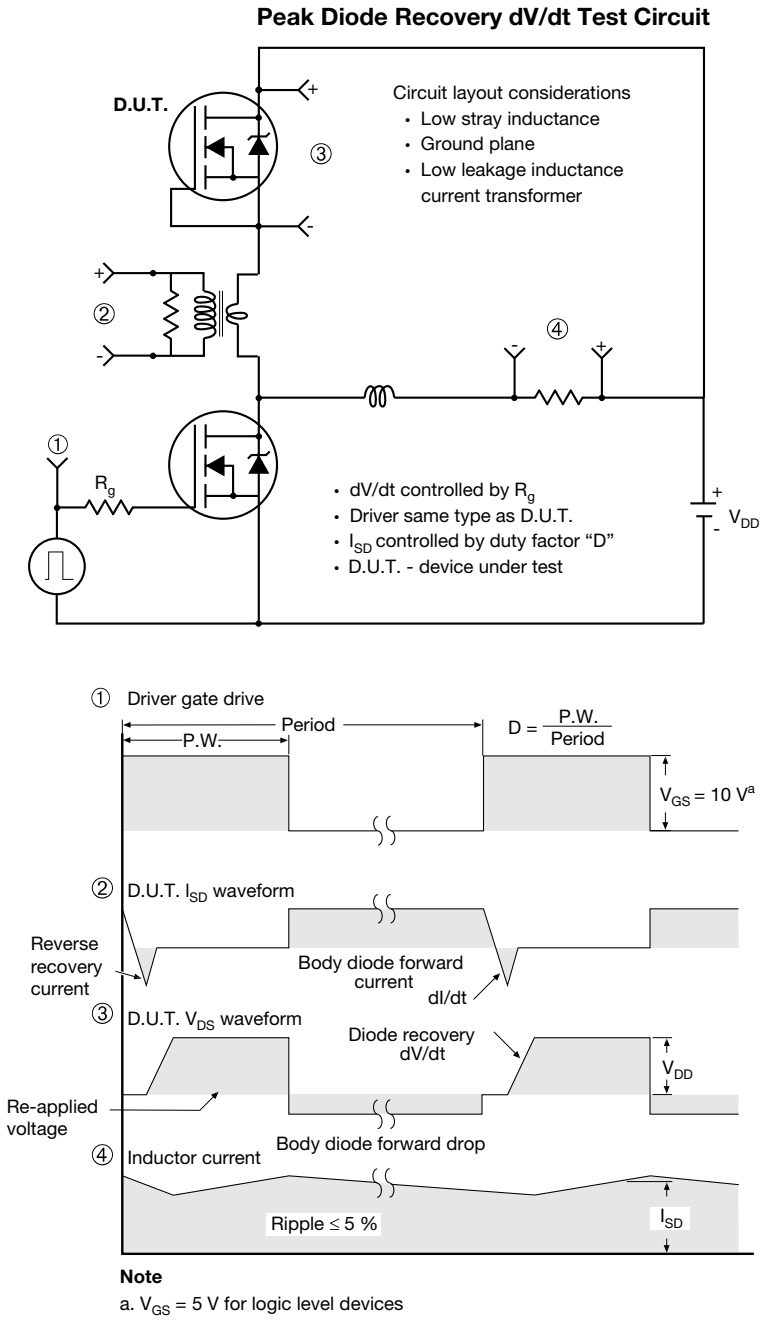


Fig. 18 - Gate Charge Test Circuit

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Note

a. V_{GS} = 5 V for logic level devices

Fig. 19 - For N-Channel

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