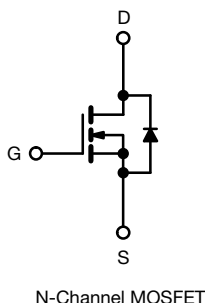


## E Series Power MOSFET

Thin-Lead TO-220 FULLPAK



### FEATURES

- 4<sup>th</sup> generation E series technology
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low effective capacitance ( $C_{o(er)}$ )
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Solar (PV inverters)

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	650	
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.60
$Q_g$ max. (nC)	12	
$Q_{gs}$ (nC)	3	
$Q_{gd}$ (nC)	3	
Configuration	Single	

### ORDERING INFORMATION

Package	Thin-Lead TO-220 FULLPAK
Lead (Pb)-free and halogen-free	SiHA690N60E-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V <sub>DS</sub>	600	V
Gate-source voltage			V <sub>GS</sub>	± 30	
Continuous drain current (T <sub>J</sub> = 150 °C) <sup>e</sup>	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	4.3	A
		T <sub>C</sub> = 100 °C		2.7	
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	11	
Linear derating factor				0.23	W/°C
Single pulse avalanche energy <sup>b</sup>			E <sub>AS</sub>	9	mJ
Maximum power dissipation			P <sub>D</sub>	29	W
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Drain-source voltage slope		T <sub>J</sub> = 125 °C	dv/dt	70	V/ns
Reverse diode dv/dt <sup>d</sup>				17	
Soldering recommendations (peak temperature) <sup>c</sup>		For 10 s		260	°C
Mounting torque, M3 screw				0.6	Nm


#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 0.8$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $di/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C
- Limited by maximum junction temperature

**THERMAL RESISTANCE RATINGS**

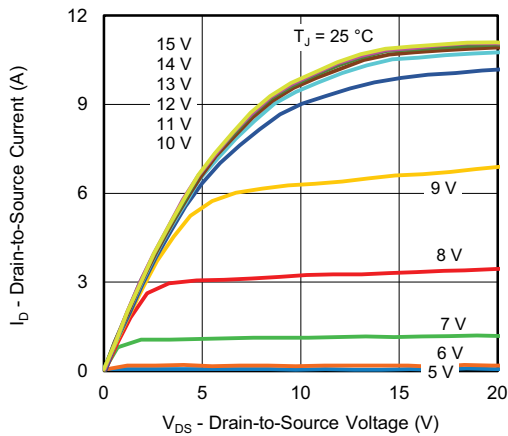
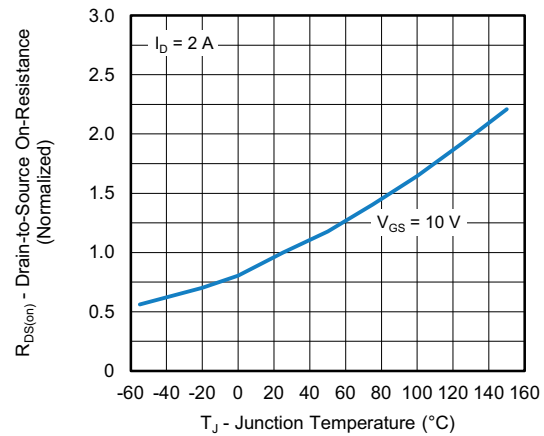
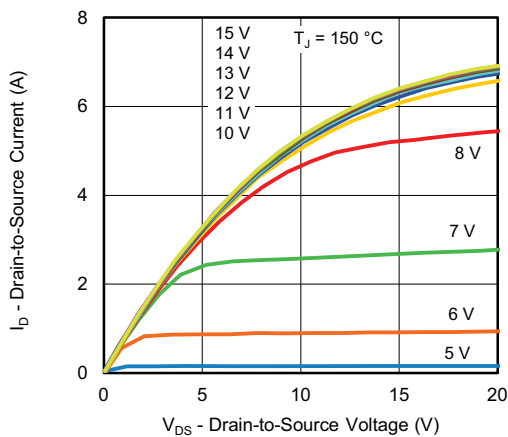
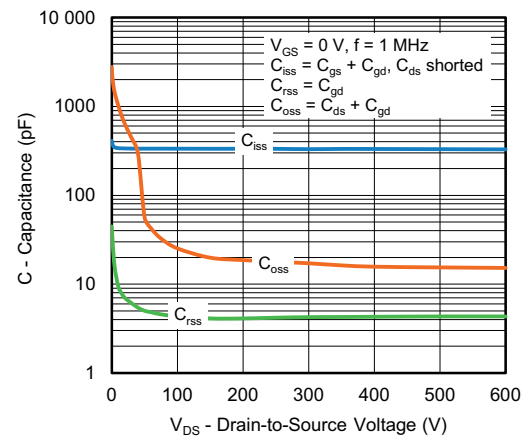
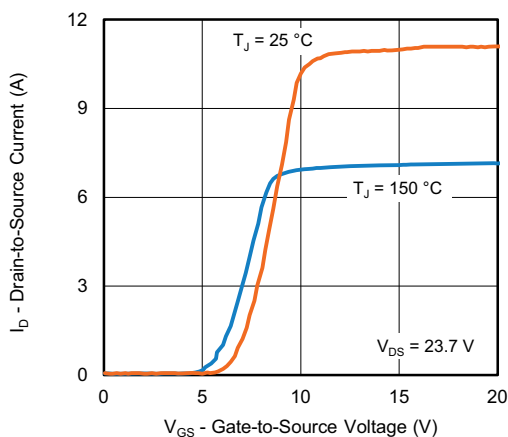
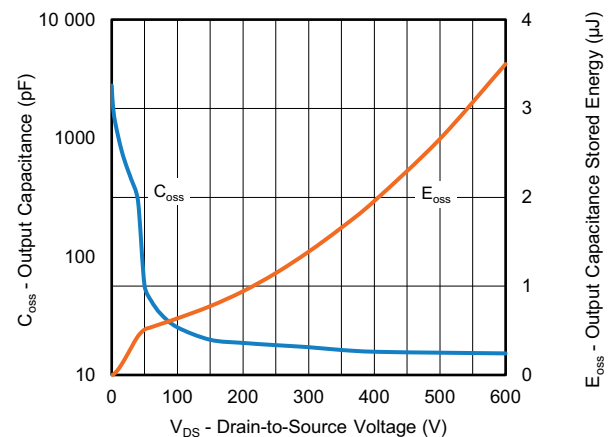
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	65	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	4.3	

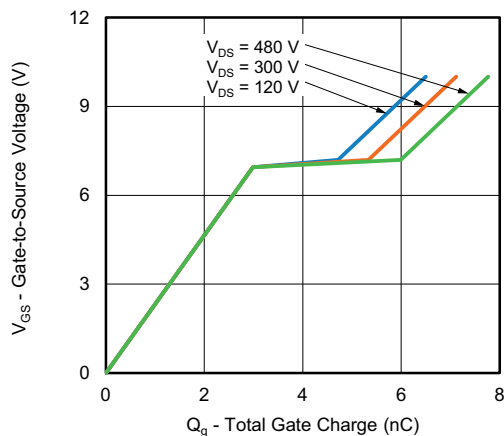
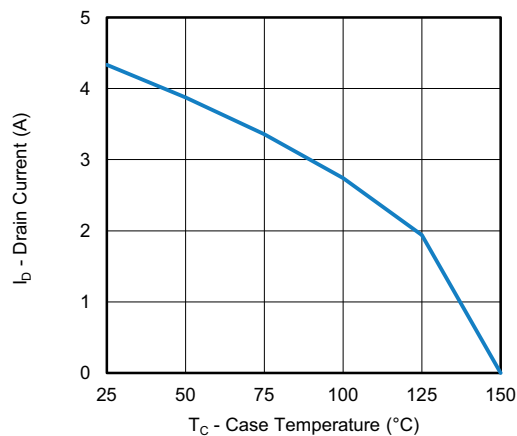
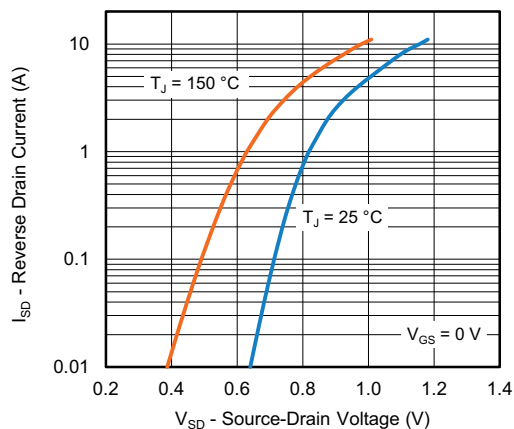
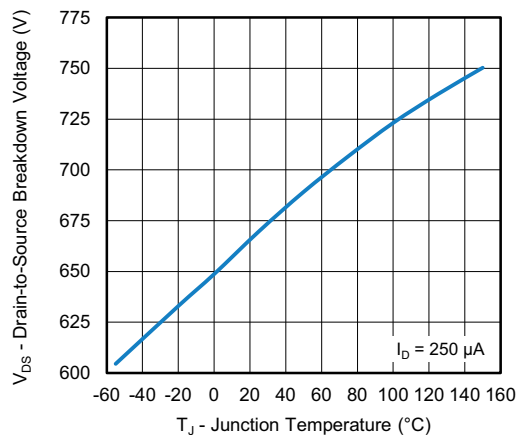
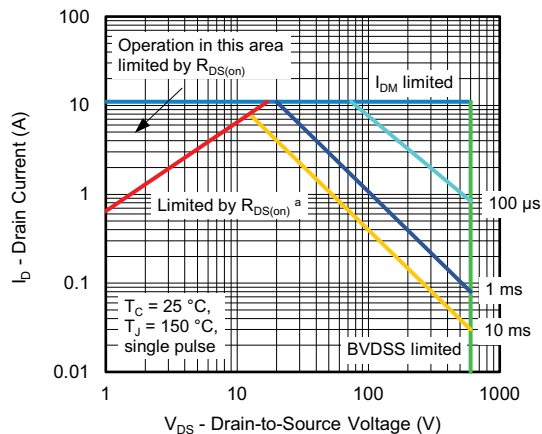
**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	600	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ °C}$ , $I_D = 1\text{ mA}$	-	0.73	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 600\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ °C}$	-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 2.0\text{ A}$	-	0.60	0.70	$\Omega$
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 20\text{ V}$ , $I_D = 2.0\text{ A}$	-	1.2	-	S
<b>Dynamic</b>						
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$	-	347	-	pF
Output capacitance	$C_{oss}$		-	24	-	
Reverse transfer capacitance	$C_{rss}$		-	4	-	
Effective output capacitance, energy related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	17	-	
Effective output capacitance, time related <sup>b</sup>	$C_{o(tr)}$		-	86	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}$ , $I_D = 2.0\text{ A}$ , $V_{DS} = 480\text{ V}$	-	8	12	nC
Gate-source charge	$Q_{gs}$		-	3	-	
Gate-drain charge	$Q_{gd}$		-	3	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 480\text{ V}$ , $I_D = 2.0\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_g = 9.1\text{ }\Omega$	-	12	24	ns
Rise time	$t_r$		-	9	18	
Turn-off delay time	$t_{d(off)}$		-	19	38	
Fall time	$t_f$		-	22	44	
Gate input resistance	$R_g$	$f = 1\text{ MHz}$ , open drain	1.1	2.3	4.6	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	6.4	A
Pulsed diode forward current	$I_{SM}$		-	-	11	
Diode forward voltage	$V_{SD}$	$T_J = 25\text{ °C}$ , $I_S = 2.0\text{ A}$ , $V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse recovery time	$t_{rr}$	$T_J = 25\text{ °C}$ , $I_F = I_S = 2.0\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_R = 25\text{ V}$	-	146	292	ns
Reverse recovery charge	$Q_{rr}$		-	1.0	2.0	$\mu\text{C}$
Reverse recovery current	$I_{RRM}$		-	13	-	A

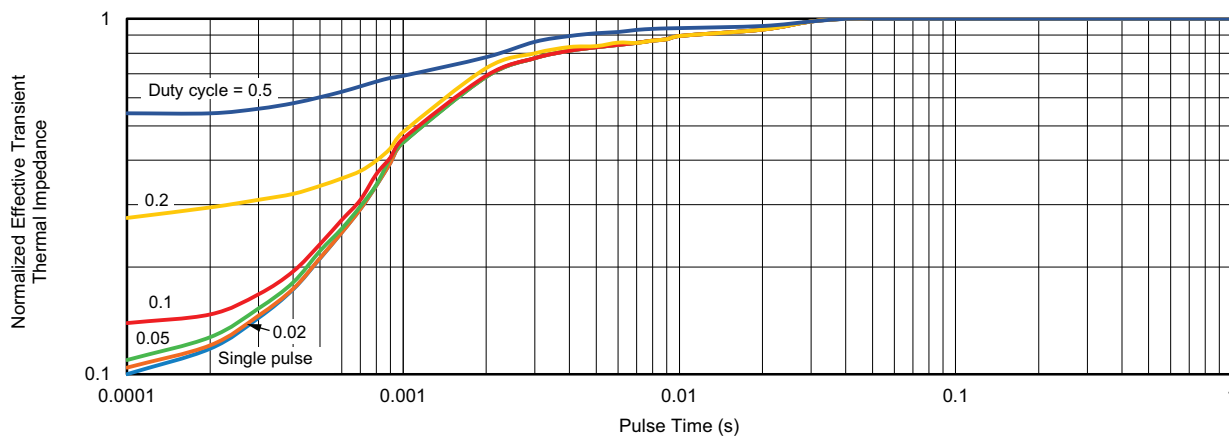
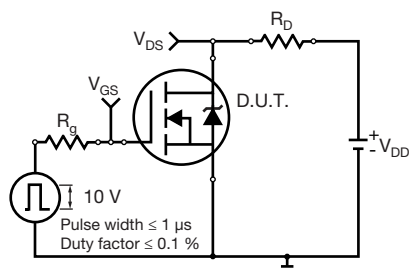
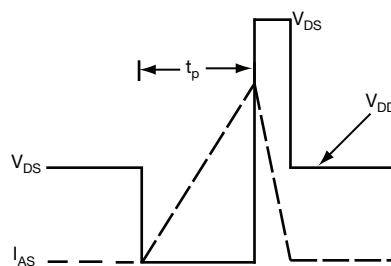
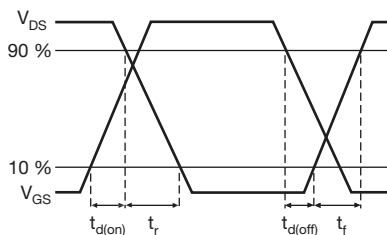
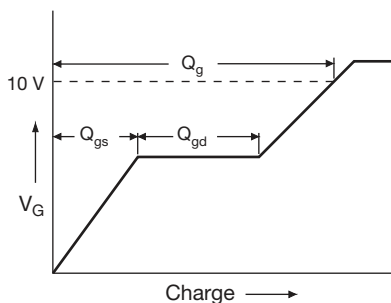
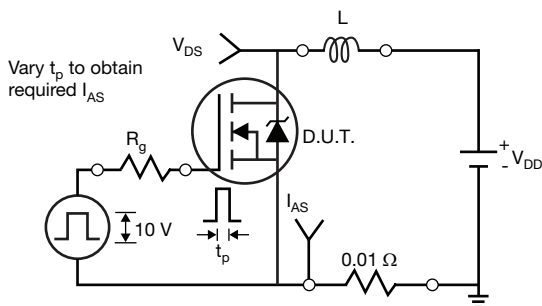
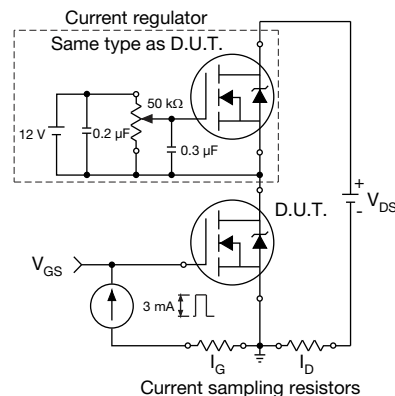
**Notes**

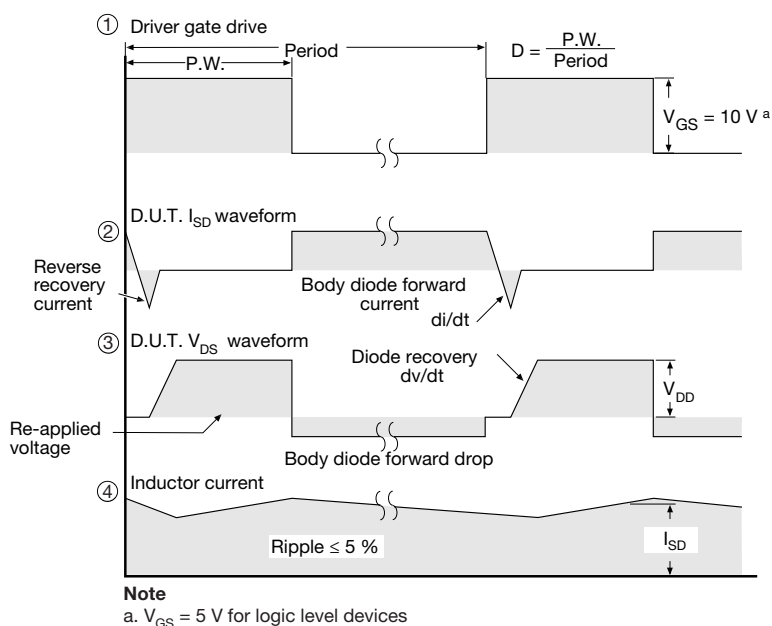
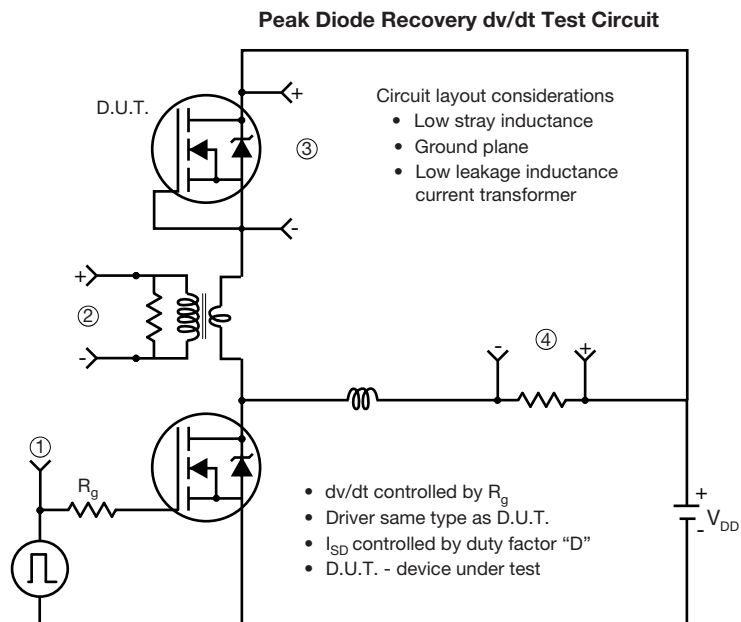
- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$
- b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**


**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 10 - Maximum Drain Current vs. Case Temperature**

**Fig. 8 - Typical Source-Drain Diode Forward Voltage**

**Fig. 11 - Temperature vs. Drain-to-Source Voltage**

**Fig. 9 - Maximum Safe Operating Area**
**Note**

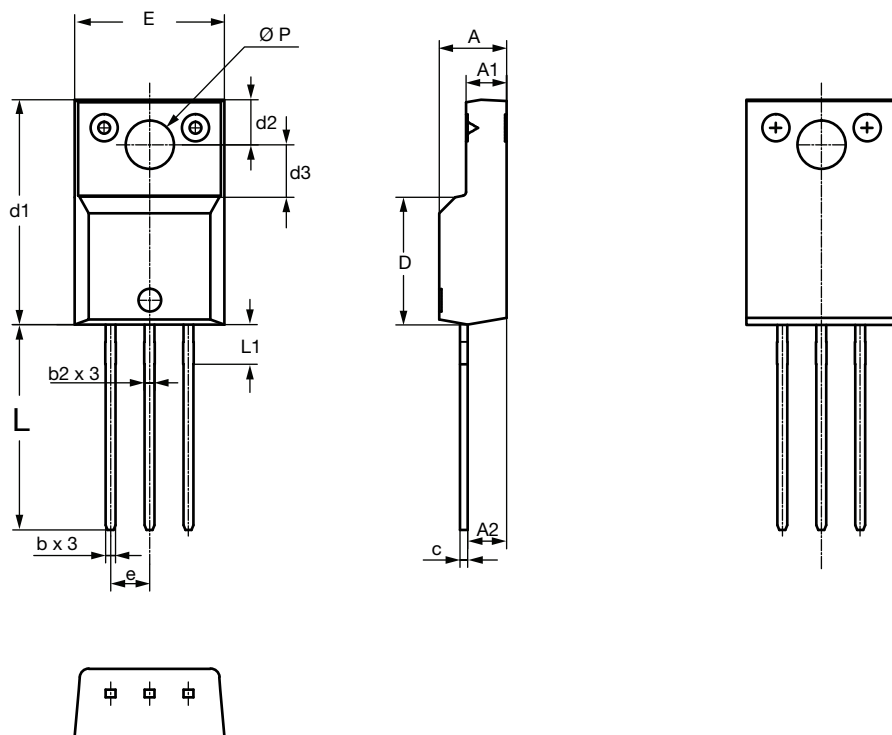
a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified


**Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case**

**Fig. 13 - Switching Time Test Circuit**

**Fig. 16 - Unclamped Inductive Waveforms**

**Fig. 14 - Switching Time Waveforms**

**Fig. 17 - Basic Gate Charge Waveform**

**Fig. 15 - Unclamped Inductive Test Circuit**

**Fig. 18 - Gate Charge Test Circuit**


**Fig. 19 - For N-Channel**

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## TO-220 FULLPAK Thin Lead



SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.30	4.70	0.169	0.185
A1	2.50	2.90	0.098	0.114
A2	2.40	2.80	0.094	0.110
b	0.60	0.80	0.024	0.031
b2	0.60	0.90	0.024	0.035
c	-	0.60	-	0.024
D	8.30	8.70	0.327	0.342
d1	14.70	15.30	0.579	0.602
d2	2.90	3.10	0.114	0.122
d3	3.30	3.70	0.130	0.146
E	9.70	10.30	0.382	0.406
e	2.50	2.70	0.098	0.106
L	13.40	13.80	0.528	0.543
L1	1.00	2.80	0.039	0.110
Ø P	3.00	3.40	0.118	0.134
ECN: E20-0684-Rev. D, 28-Dec-2020 DWG: 6021				



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