



## Phase Control Thyristors (Hockey PUK Version), 1745 A



K-PUK (A-24)

### FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case K-PUK (A-24)
- High profile hockey PUK
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

RoHS  
COMPLIANT

### TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

### PRIMARY CHARACTERISTICS

$I_{T(AV)}$	1745 A
$V_{DRM}/V_{RRM}$	800 V, 1200 V, 1400 V, 1600 V
$V_{TM}$	1.62 V
$I_{GT}$	100 mA
$T_J$	-40 °C to +125 °C
Package	K-PUK (A-24)
Circuit configuration	Single SCR

### MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		1745	A
	$T_{hs}$	55	°C
$I_{T(RMS)}$		3200	A
	$T_{hs}$	25	°C
$I_{TSM}$	50 Hz	33 500	A
	60 Hz	35 100	
$I^2t$	50 Hz	5615	kA <sup>2</sup> s
	60 Hz	5126	
$V_{DRM}/V_{RRM}$		800 to 1600	V
$t_q$	Typical	200	μs
$T_J$		-40 to +125	°C

### ELECTRICAL SPECIFICATIONS

#### VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	$V_{DRM}/V_{RRM}$ , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$I_{DRM}/I_{RRM}$ MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST1230C..K	08	800	900	100
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled		1745 (700)	A
				55 (85)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 °C heatsink temperature double side cooled		3200	
Maximum peak, one-cycle non-repetitive surge current	$I_{TSM}$	t = 10 ms	No voltage reapplied	33 500	A
		t = 8.3 ms	No voltage reapplied	35 100	
		t = 10 ms	100 % $V_{RRM}$ reapplied	28 200	
		t = 8.3 ms	100 % $V_{RRM}$ reapplied	29 500	
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reapplied	5615	kA <sup>2</sup> s
		t = 8.3 ms	No voltage reapplied	5126	
		t = 10 ms	100 % $V_{RRM}$ reapplied	3971	
		t = 8.3 ms	100 % $V_{RRM}$ reapplied	3625	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied		56 150	kA <sup>2</sup> √s
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ ), $T_J = T_J$ maximum		0.93	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > $\pi \times I_{T(AV)}$ ), $T_J = T_J$ maximum		1.02	
Low level value of on-state slope resistance	$r_{t1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ ), $T_J = T_J$ maximum		0.17	mΩ
High level value of on-state slope resistance	$r_{t2}$	(I > $\pi \times I_{T(AV)}$ ), $T_J = T_J$ maximum		0.16	
Maximum on-state voltage	$V_{TM}$	$I_{pk} = 4000$ A, $T_J = T_J$ maximum, $t_p = 10$ ms sine pulse		1.62	V
Maximum holding current	$I_H$	$T_J = 25$ °C, anode supply 12 V resistive load		600	mA
Typical latching current	$I_L$			1000	

**SWITCHING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	$di/dt$	Gate drive 20 V, 20 Ω, $t_r \leq 1$ μs $T_J = T_J$ maximum, anode voltage $\leq 80$ % $V_{DRM}$	1000	A/μs
Typical delay time	$t_d$	Gate current 1 A, $di_g/dt = 1$ A/μs $V_d = 0.67$ % $V_{DRM}$ , $T_J = 25$ °C	1.9	μs
Typical turn-off time	$t_q$	$I_{TM} = 550$ A, $T_J = T_J$ maximum, $di/dt = 40$ A/μs, $V_R = 50$ V, $dV/dt = 20$ V/μs, gate 0 V 100 Ω, $t_p = 500$ μs	200	

**BLOCKING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	$dV/dt$	$T_J = T_J$ maximum linear to 80 % rated $V_{DRM}$	500	V/μs
Maximum peak reverse and off-state leakage current	$I_{RRM}$ , $I_{DRM}$	$T_J = T_J$ maximum, rated $V_{DRM}/V_{RRM}$ applied	100	mA



TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNITS
			typ.	Max.	
Maximum peak gate power	$P_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	16		W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	3		
Maximum peak positive gate current	$I_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	3.0		A
Maximum peak positive gate voltage	$+V_{GM}$		20		V
Maximum peak negative gate voltage	$-V_{GM}$		5.0		
DC gate current required to trigger	$I_{GT}$	$T_J = -40$ °C	200	-	mA
		$T_J = 25$ °C	100	200	
		$T_J = 125$ °C	50	-	
DC gate voltage required to trigger	$V_{GT}$	$T_J = -40$ °C	1.4	-	V
		$T_J = 25$ °C	1.1	3.0	
		$T_J = 125$ °C	0.9	-	
DC gate current not to trigger	$I_{GD}$	$T_J = T_J$ maximum	10		mA
DC gate voltage not to trigger	$V_{GD}$		0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	$T_J$		-40 to 125	°C
Maximum storage temperature range	$T_{Stg}$		-40 to 150	
Maximum thermal resistance, junction to heatsink	$R_{thJ-hs}$	DC operation single side cooled	0.042	K/W
		DC operation double side cooled	0.021	
Maximum thermal resistance, case to heatsink	$R_{thC-hs}$	DC operation single side cooled	0.006	
		DC operation double side cooled	0.003	
Mounting force, $\pm 10$ %			24 500 (2500)	N (kg)
Approximate weight			425	g
Case style		See dimensions - link at the end of datasheet	K-PUK (A-24)	

$\Delta R_{thJC}$ CONDUCTION						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.003	0.003	0.002	0.002	T <sub>J</sub> = T <sub>J</sub> maximum	K/W
120°	0.004	0.004	0.004	0.004		
90°	0.005	0.005	0.005	0.005		
60°	0.007	0.007	0.007	0.007		
30°	0.012	0.012	0.012	0.012		

**Note**

- The table above shows the increment of thermal resistance  $R_{thJC}$  when devices operate at different conduction angles than DC

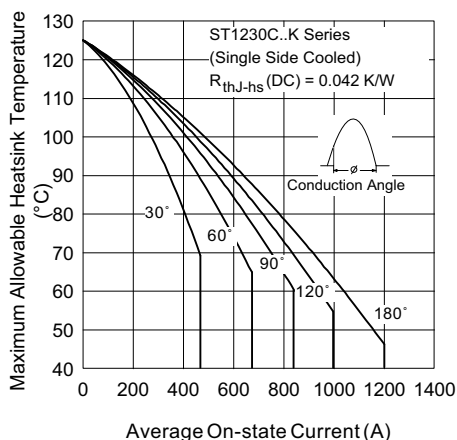


Fig. 1 - Current Ratings Characteristics

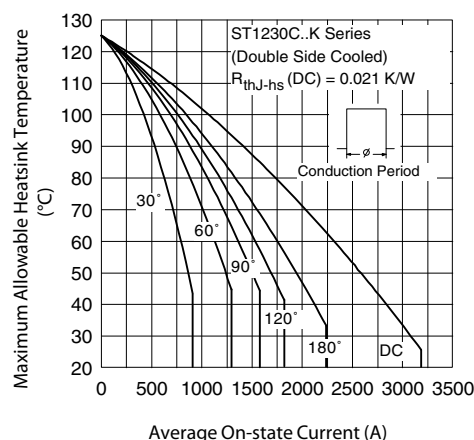


Fig. 4 - Current Ratings Characteristics

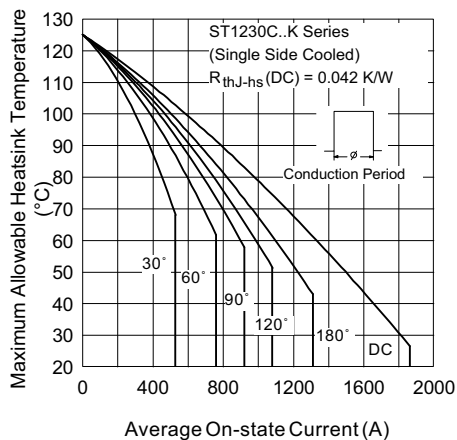


Fig. 2 - Current Ratings Characteristics

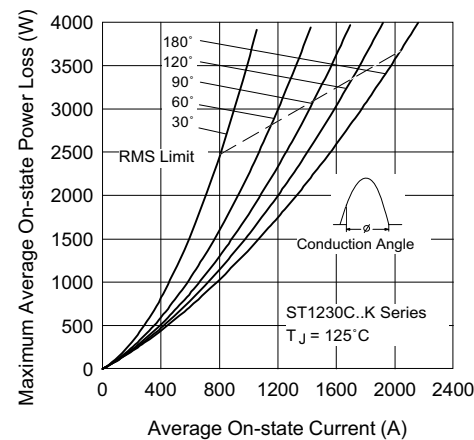


Fig. 5 - On-State Power Loss Characteristics

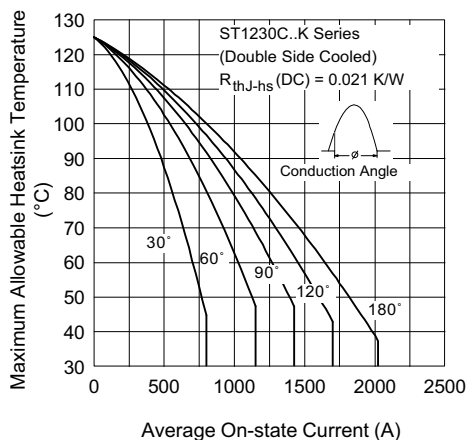


Fig. 3 - Current Ratings Characteristics

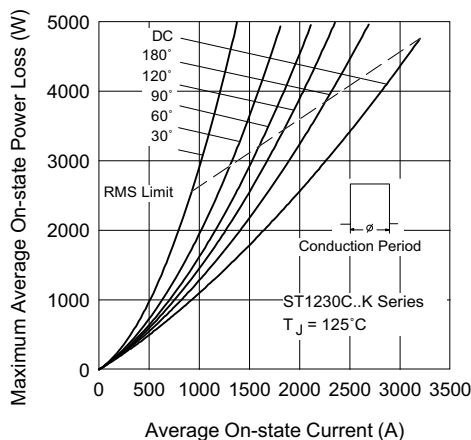


Fig. 6 - On-State Power Loss Characteristics

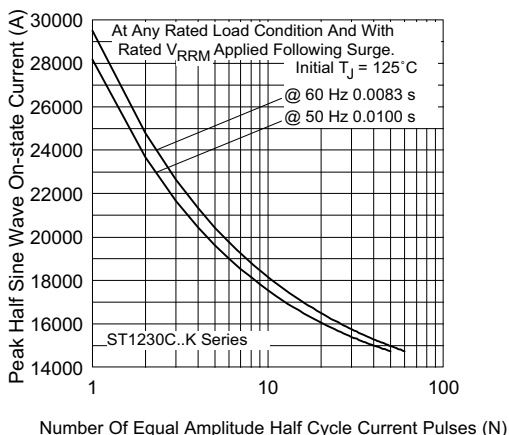


Fig. 7 - Maximum Non-Repetitive Surge Current  
Single and Double Side Cooled

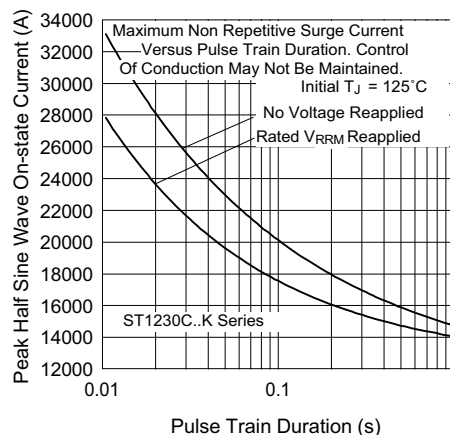


Fig. 8 - Maximum Non-Repetitive Surge Current  
Single and Double Side Cooled

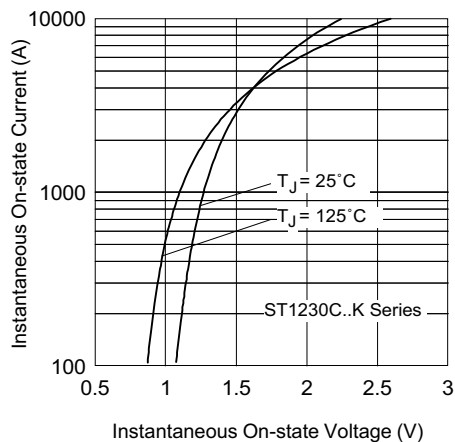


Fig. 9 - On-State Voltage Drop Characteristics

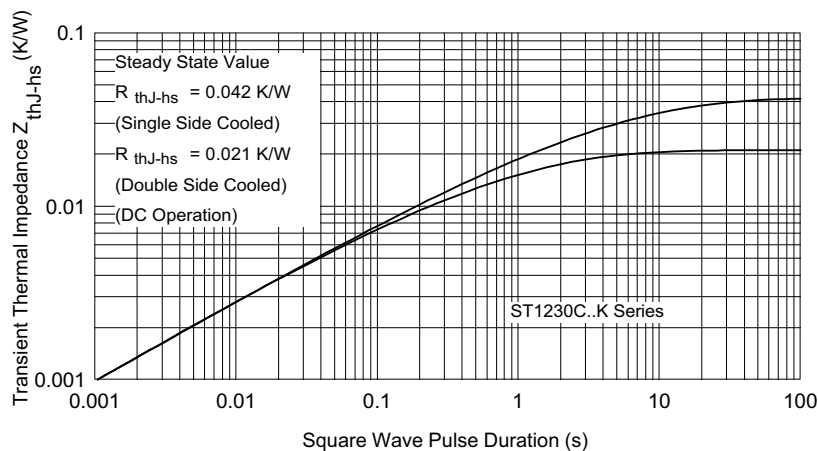


Fig. 10 - Thermal Impedance  $Z_{thJ-hs}$  Characteristics

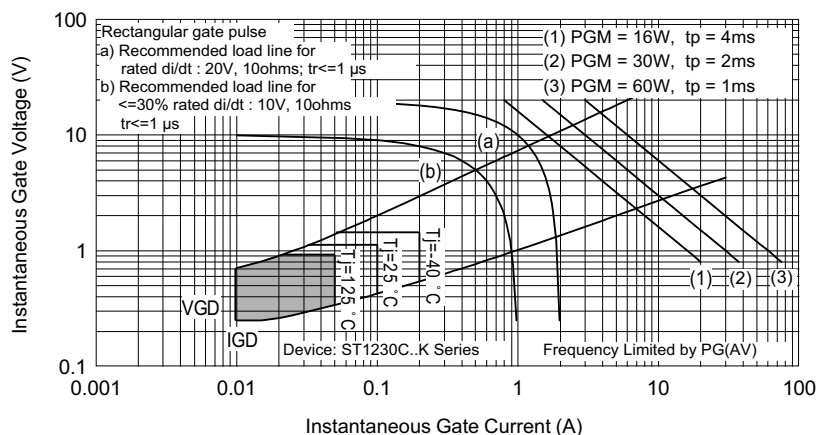


Fig. 11 - Gate Characteristics

## ORDERING INFORMATION TABLE

Device code	VS-	ST	123	0	C	16	K	1	-
	1	2	3	4	5	6	7	8	9
1	Vishay Semiconductors product								
2	Thyristor								
3	Essential part number								
4	0 = converter grade								
5	C = ceramic PUK								
6	Voltage code x 100 = $V_{RRM}$ (see Voltage Ratings table)								
7	K = PUK case K-PUK (A-24)								
8	0 = eyelet terminals (gate and auxiliary cathode unsoldered leads) 1 = fast-on terminals (gate and auxiliary cathode unsoldered leads) 2 = eyelet terminals (gate and auxiliary cathode soldered leads) 3 = fast-on terminals (gate and auxiliary cathode soldered leads)								
9	Critical $dV/dt$ : • None = 500 V/ $\mu s$ (standard selection) • L = 1000 V/ $\mu s$ (special selection)								

## LINKS TO RELATED DOCUMENTS

Dimensions

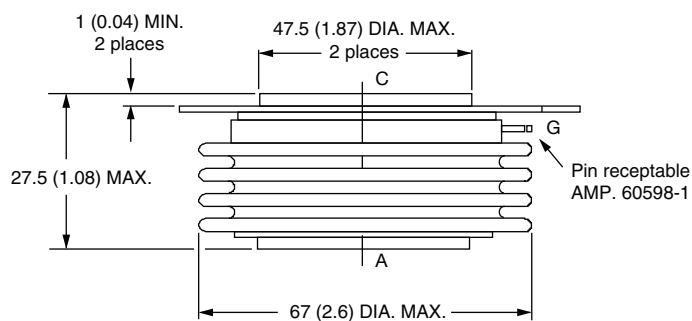
[www.vishay.com/doc?95081](http://www.vishay.com/doc?95081)



## K-PUK (A-24)

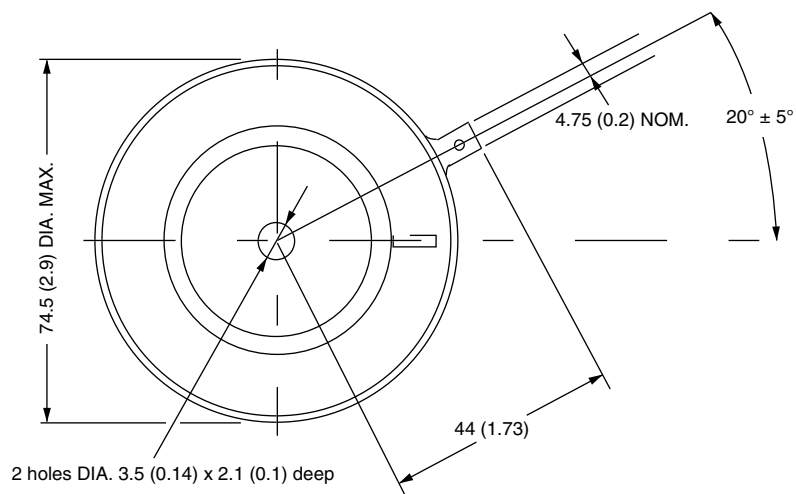
### DIMENSIONS in millimeters (inches)

Creepage distance: 28.88 (1.137) minimum  
Strike distance: 17.99 (0.708) minimum



#### Note:

A = Anode  
C = Cathode  
G = Gate



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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