

Phase Control Thyristors (Hockey PUK Version), 500 A



A-PUK (TO-200AB)

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case A-PUK (TO-200AB)
- Extended temperature range
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

PRIMARY CHARACTERISTICS

$I_{T(AV)}$	500 A
V_{DRM}/V_{RRM}	400 V, 600 V
V_{TM}	1.35 V
I_{GT}	90 mA
T_J	-40 °C to +150 °C
Package	A-PUK (TO-200AB)
Circuit configuration	Single SCR

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		500	A
	T_{hs}	80	°C
$I_{T(RMS)}$		1130	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	7200	A
	60 Hz	7500	
I^2t	50 Hz	260	kA ² s
	60 Hz	230	
V_{DRM}/V_{RRM}		400 to 600	V
t_q	Typical	100	μs
T_J		-40 to 150	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST280CH..C	04	400	500	75
	06	600	700	



ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled	500 (185)	A
			80 (110)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 °C heatsink temperature double side cooled	1130	
Maximum peak, one-cycle non-repetitive surge current	I_{TSM}	t = 10 ms	7200	A
		t = 8.3 ms	7500	
		t = 10 ms	6000	
		t = 8.3 ms	6300	
Maximum I^2t for fusing	I^2t	t = 10 ms	260	kA ² s
		t = 8.3 ms	235	
		t = 10 ms	180	
		t = 8.3 ms	165	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied	2600	kA ² √s
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$, $T_J = T_J$ maximum	0.84	V
High level value of threshold voltage	$V_{T(TO)2}$	($I > \pi \times I_{T(AV)}$, $T_J = T_J$ maximum	0.88	
Low level value of on-state slope resistance	r_{t1}	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$, $T_J = T_J$ maximum	0.50	mΩ
High level value of on-state slope resistance	r_{t2}	($I > \pi \times I_{T(AV)}$, $T_J = T_J$ maximum	0.47	
Maximum on-state voltage	V_{TM}	$I_{pk} = 1000$ A, $T_J = T_J$ maximum, $t_p = 10$ ms sine pulse	1.35	V
Maximum holding current	I_H	$T_J = 25$ °C, anode supply 12 V resistive load	600	mA
Maximum (typical) latching current	I_L		1000 (300)	

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ μs $T_J = T_J$ maximum, anode voltage ≤ 80 % V_{DRM}	1000	A/μs
Typical delay time	t_d	Gate current 1 A, $di_g/dt = 1$ A/μs $V_d 0.67$ % V_{DRM} , $T_J = 25$ °C	1.0	μs
Typical turn-off time	t_q	$I_{TM} = 300$ A, $T_J = T_J$ maximum, $di/dt = 20$ A/μs, $V_R = 50$ V, $dV/dt = 20$ V/μs, gate 0 V 100 Ω, $t_p = 500$ μs	100	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT S
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/μs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	75	mA



TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES		UNITS
				TYP.	MAX.	
Maximum peak gate power	P _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		10.0		W
Maximum average gate power	P _{G(AV)}	T _J = T _J maximum, f = 50 Hz, d% = 50		2.0		
Maximum peak positive gate current	I _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		3.0		A
Maximum peak positive gate voltage	+ V _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		20		V
Maximum peak negative gate voltage	- V _{GM}			5.0		
DC gate current required to trigger	I _{GT}	T _J = - 40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	180	-	mA
		T _J = 25 °C		90	150	
		T _J = 150 °C		30	-	
DC gate voltage required to trigger	V _{GT}	T _J = - 40 °C		2.9	-	V
		T _J = 25 °C		1.8	3.0	
		T _J = 150 °C		1.0	-	
DC gate current not to trigger	I _{GD}	T _J = T _J maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V _{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V _{GD}			0.30		V

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum operating junction and storage temperature range	T_J, T_{Stg}			- 40 to 150	°C
Maximum thermal resistance, junction to heatsink	R_{thJ-hs}	DC operation single side cooled		0.17	K/W
		DC operation double side cooled		0.08	
Maximum thermal resistance, case to heatsink	R_{thC-hs}	DC operation single side cooled		0.033	
		DC operation double side cooled		0.017	
Mounting force, ± 10 %				4900 (500)	N (kg)
Approximate weight				50	g
Case style		See dimensions - link at the end of datasheet		A-PUK (TO-200AB)	

ΔR_{thJ-hs} CONDUCTION						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.016	0.017	0.011	0.011	T _J = T _J maximum	K/W
120°	0.019	0.019	0.019	0.019		
90°	0.024	0.024	0.026	0.026		
60°	0.035	0.035	0.036	0.037		
30°	0.060	0.060	0.060	0.061		

Note

- The table above shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC

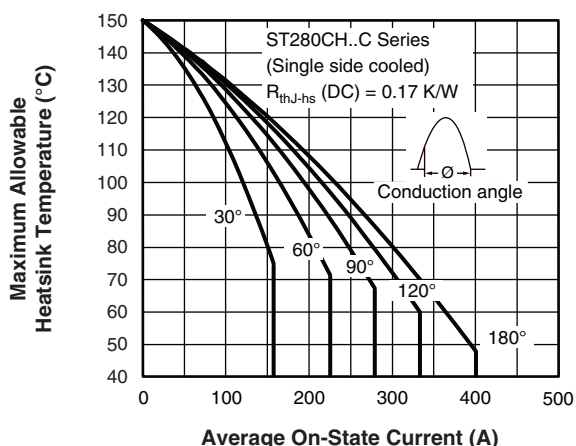


Fig. 1 - Current Ratings Characteristics

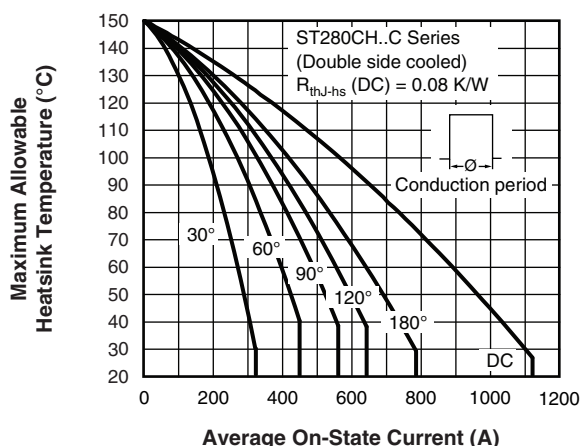


Fig. 4 - Current Ratings Characteristics

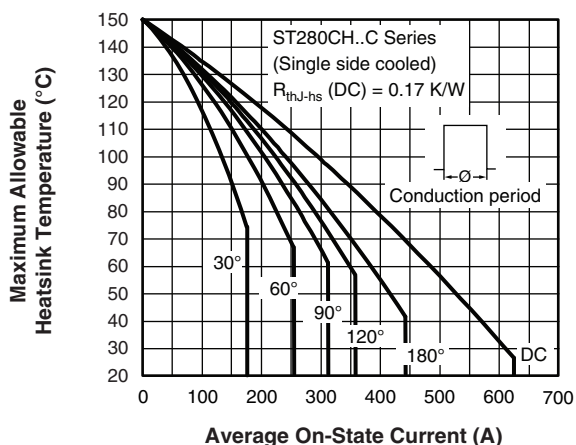


Fig. 2 - Current Ratings Characteristics

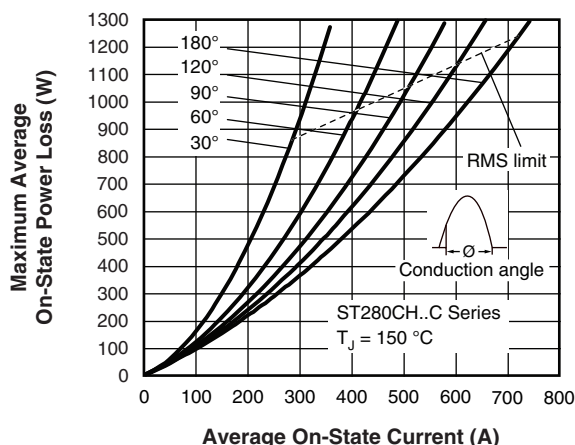


Fig. 5 - On-State Power Loss Characteristics

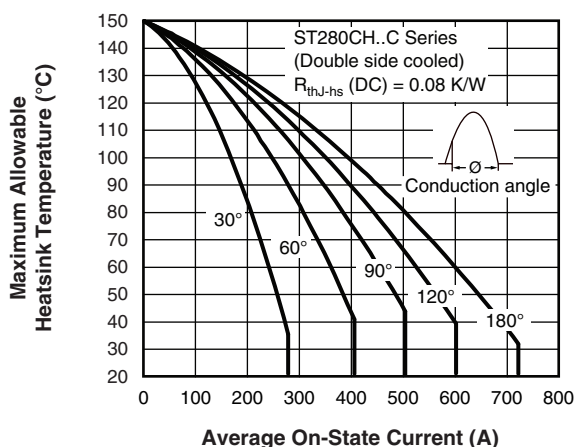


Fig. 3 - Current Ratings Characteristics

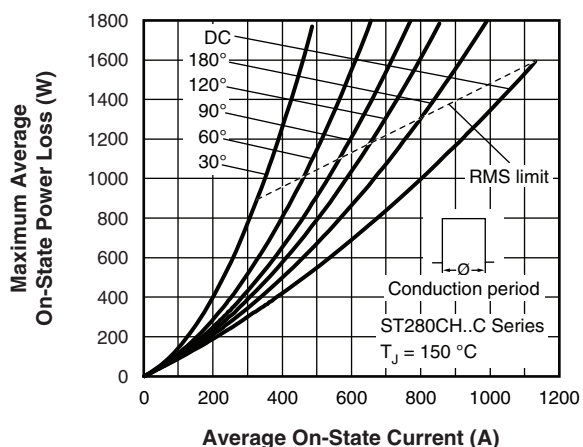


Fig. 6 - On-State Power Loss Characteristics

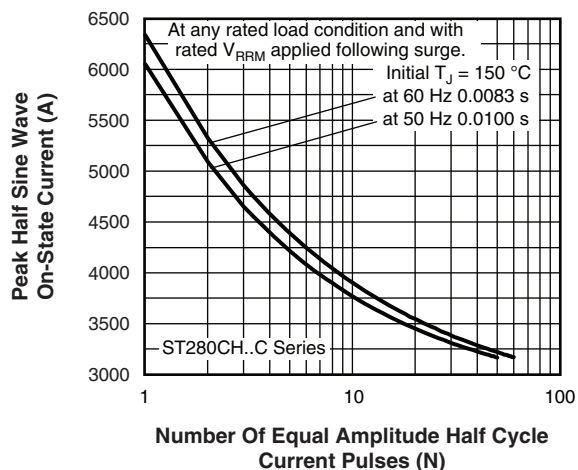


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

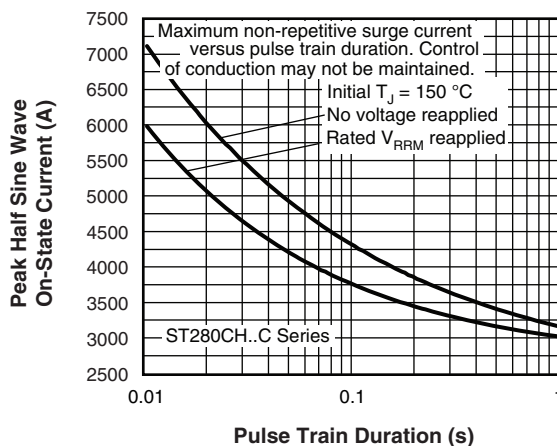


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

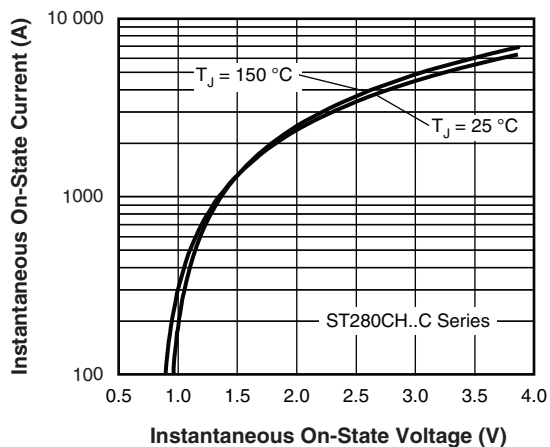


Fig. 9 - On-State Voltage Drop Characteristics

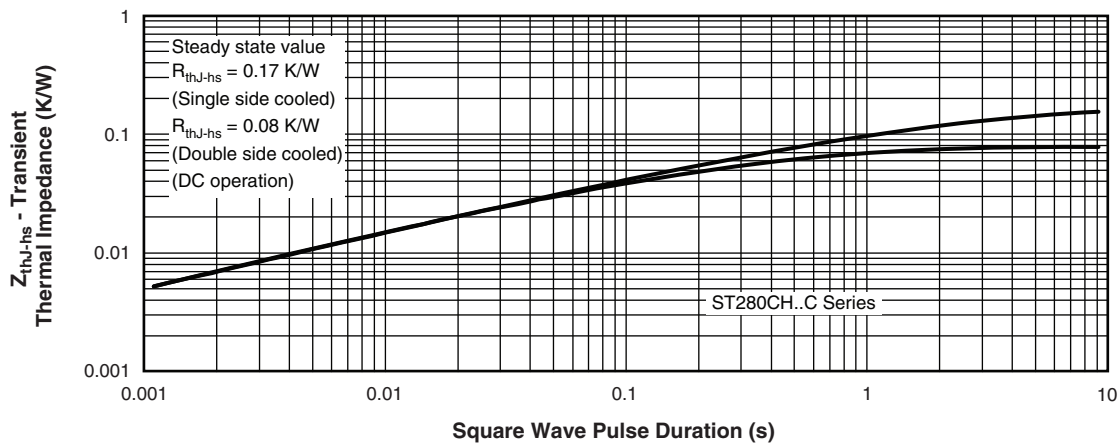


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

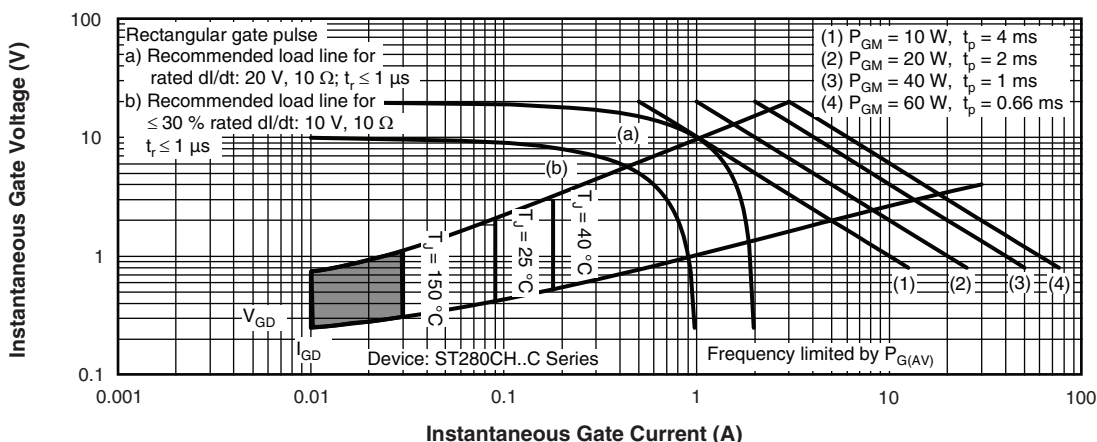


Fig. 11 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code	VS-	ST	28	0	CH	06	C	1	-
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)

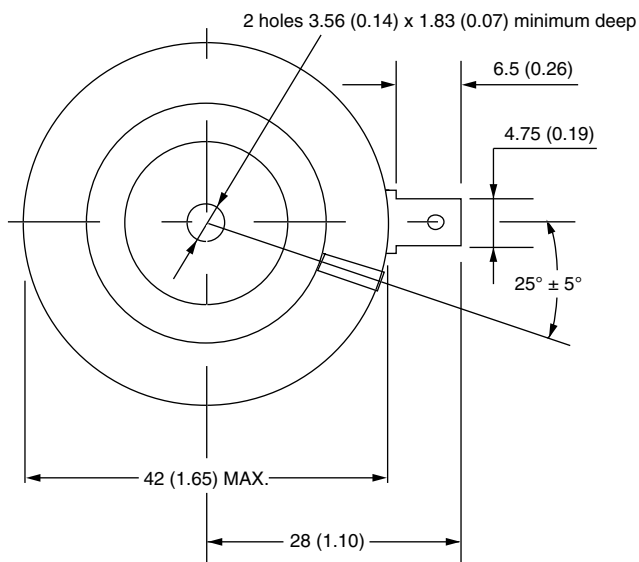
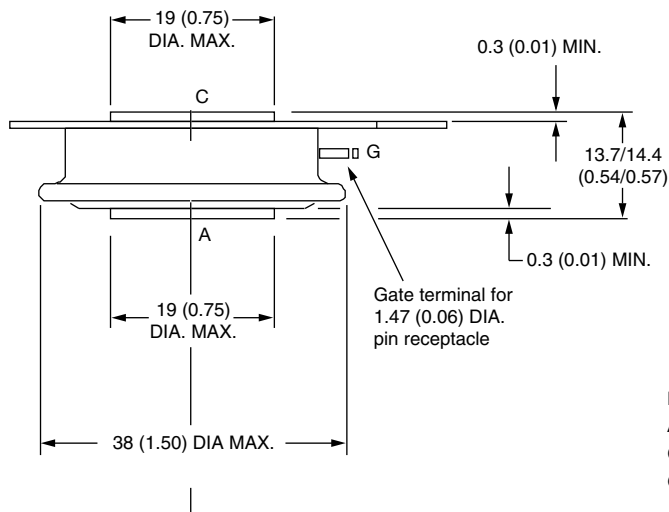
- | | |
|---|--|
| 1 | - Vishay Semiconductors product |
| 2 | - Thyristor |
| 3 | - Essential part number |
| 4 | - 0 = converter grade |
| 5 | - CH = ceramic PUK, high temperature |
| 6 | - Voltage code x 100 = V_{RRM} (see Voltage Ratings table) |
| 7 | - C = PUK case A-PUK (TO-200AB) |
| 8 | - 0 = eyelet terminals (gate and auxiliary cathode unsoldered leads)
1 = fast-on terminals (gate and auxiliary cathode unsoldered leads)
2 = eyelet terminals (gate and auxiliary cathode soldered leads)
3 = fast-on terminals (gate and auxiliary cathode soldered leads) |
| 9 | - Critical dV/dt : • None = 500 V/ μs (standard selection)
• L = 1000 V/ μs (special selection) |

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95074

A-PUK (TO-200AB)

DIMENSIONS in millimeters (inches)

Anode to gate
Creepage distance: 7.62 (0.30) minimum
Strike distance: 7.12 (0.28) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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