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Vishay Semiconductors

## SCR/Diode (MAGN-A-PAK Power Modules), 320 A



PRIMARY CHARACTERISTICS					
$I_{T(AV)}$ or $I_{F(AV)}$	320 A				
Type	Modules - thyristor, standard				
Package	MAGN-A-PAK				

### **FEATURES**

- High voltage
- · Electrically isolated base plate
- 3500 V<sub>RMS</sub> isolating voltage
- · Industrial standard package
- · Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- · Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912">www.vishav.com/doc?99912</a>

#### **DESCRIPTION**

This VSK series of MAGN-A-PAK modules uses high voltage power thyristor/thyristor and thyristor / diode in seven basic configurations. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase or three phase bridges or as AC-switches when modules are connected in anti-parallel mode. These modules are intended for general purpose applications such as battery chargers, welders, motor drives, UPS, etc.

MAJOR RATINGS AND CHARACTERISTICS							
SYMBOL	CHARACTERISTICS	VALUES	UNITS				
I <sub>T(AV)</sub> /I <sub>F(AV)</sub>	70 °C	320					
I <sub>T(RMS)</sub>		502	^				
1 /	50 Hz	9000	A				
I <sub>TSM</sub> /I <sub>FSM</sub>	60 Hz	9420					
l <sup>2</sup> t	50 Hz	405	kA <sup>2</sup> s				
1-1	60 Hz	370	KA-S				
I <sup>2</sup> √t		4050	kA²√s				
V <sub>DRM</sub> /V <sub>RRM</sub>		1600	V				
$T_J$	Range	-40 to +130	°C				

### **ELECTRICAL SPECIFICATIONS**

VOLTAGE RATINGS							
TYPE NUMBER	VOLTAGE CODE	V <sub>RRM</sub> /V <sub>DRM</sub> , MAXIMUM REPETITIVE PEAK REVERSE AND OFF-STATE BLOCKING VOLTAGE V	V <sub>RSM</sub> , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I <sub>RRM</sub> /I <sub>DRM</sub> AT 130 °C MAXIMUM mA			
VS-VSKH320-	16	1600	1700	50			



ON-STATE CONDUCTION							
PARAMETER	SYMBOL		TEST CONDITIONS			UNITS	
Maximum average on-state current at case temperature (thyristor)	I <sub>T(AV)</sub>	180° conduction, half sine wave		320	А		
Maximum average forward current (diode)	I <sub>F(AV)</sub>	180 Conduction	i, riali Sirie wave		70	°C	
Maximum RMS on-state current	I <sub>O(RMS)</sub>	As AC switch ⊶	I <sub>RMS</sub>		704		
		t = 10 ms	No voltage		9000		
Maximum peak, one-cycle on-state		t = 8.3 ms	reapplied		9420	Α	
non-repetitive, surge current	I <sub>TSM</sub>	t = 10 ms	100 % V <sub>BBM</sub>	0:	7570		
		t = 8.3 ms	reapplied	Sinusoidal half wave,	7920	7 1	
		t = 10 ms	No voltage	initial T <sub>J</sub> = T <sub>J</sub> maximum	405	kA <sup>2</sup> s	
Maximum 12t fax fusing	l <sup>2</sup> t	t = 8.3 ms	reapplied		370		
Maximum I <sup>2</sup> t for fusing		t = 10 ms	100 % V <sub>BBM</sub>		287		
		t = 8.3 ms			262		
Maximum l²√t for fusing	I²√t	t = 0.1 ms to 10	ms, no voltage rea	applied	4050	kA²√s	
Low level value or threshold voltage	V <sub>T(TO)1</sub>	(16.7 % x $\pi$ x I <sub>T(</sub> T <sub>J</sub> = T <sub>J</sub> maximus	$f_{AV} < I < \pi \times I_{T(AV)},$ m		0.80	V	
High level value of threshold voltage	V <sub>T(TO)2</sub>	$(I > \pi \times I_{T(AV)} < I$	$<\pi \times I_{T(AV)}$ , $T_J = T_V$	<sub>I</sub> maximum	1.03		
Low level value on-state slope resistance	r <sub>t1</sub>		(16.7 % x $\pi$ x $I_{T(AV)}$ < $I$ < $\pi$ x $I_{T(AV)}$ ), $I_J = I_J$ maximum			mΩ	
High level value on-state slope resistance	r <sub>t2</sub>	$(I > \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$			0.53		
Maximum on-state voltage drop	$V_{TM}, V_{FM}$	$I_{TM} = \pi \times I_{T(AV)}, I_{FM} = \pi \times I_{F(AV)}, T_J = T_J$ maximum, 180° conduction			1.50	V	
Maximum holding current	I <sub>H</sub>	Anode supply =	12 V, initial I <sub>T</sub> = 30	A, T <sub>J</sub> = 25 °C	500		
Maximum latching current	ΙL		12 V, resistive load, 100 $\mu$ s, T <sub>J</sub> = 25 °		1000	mA	

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VS-VSKH320	UNITS
Typical delay time	t <sub>d</sub>	T <sub>J</sub> = 25 °C, gate current = 1 A dl <sub>g</sub> /dt = 1 A/μs	1.0	
Typical rise time	t <sub>r</sub>	$V_{d} = 0.67 \% V_{DRM}$	2.0	us
Typical turn-off time	t <sub>q</sub>	$I_{TM}$ = 300 A; dI/dt = 15 A/μs; $T_J$ = $T_J$ maximum; $V_R$ = 50 V; dV/dt = 20 V/μs; gate 0 V, 100 $\Omega$	200 to 350	<b>,</b>

BLOCKING							
PARAMETER	SYMBOL	TEST CONDITIONS	VS-VSKH320	UNITS			
Maximum peak reverse and off-state leakage current	I <sub>RRM,</sub> I <sub>DRM</sub>	$T_J = T_J$ maximum	50	mA			
RMS insulation voltage	V <sub>INS</sub>	50 Hz, circuit to base, all terminals shorted, 25 °C, 1 s	3000	V			
Critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, exponential to 67 % rated $V_{DRM}$	1000	V/µs			

## VS-VSKH320-16PbF Series

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TRIGGERING					
PARAMETER	SYMBOL	TEST CO	ONDITIONS	VS-VSKH320	UNITS
Maximum peak gate power	$P_{GM}$	$t_p \le 5 \text{ ms}, T_J = T_J \text{ m}$	aximum	10.0	w
Maximum average gate power	P <sub>G(AV)</sub>	$f = 50 Hz, T_J = T_J m$	aximum	2.0	] vv
Maximum peak gate current	+ I <sub>GM</sub>	$t_p \le 5 \text{ ms}, T_J = T_J \text{ m}$	aximum	3.0	Α
Maximum peak negative gate voltage	- V <sub>GT</sub>	$t_p \le 5 \text{ ms}, T_J = T_J \text{ m}$	aximum	5.0	
		T <sub>J</sub> = - 40 °C	Anode supply = $12 \text{ V}$ , resistive load; $R_a = 1$	4.0	V
Maximum required DC gate voltage to trigger	V <sub>GT</sub>	T <sub>J</sub> = 25 °C		3.0	V
		T <sub>J</sub> = T <sub>J</sub> maximum	Ω	2.0	
		T <sub>J</sub> = - 40 °C	Anode supply = 12 V,	350	
Maximum required DC gate current to trigger	I <sub>GT</sub>	T <sub>J</sub> = 25 °C	resistive load; R <sub>a</sub> = 1	200	mA
		T <sub>J</sub> = T <sub>J</sub> maximum	Ω	100	
Maximum gate voltage that will not trigger	$V_{GD}$	$T_J = T_J$ maximum, rated $V_{DRM}$ applied		0.25	V
Maximum gate current that will not trigger	$I_{GD}$	$T_J = T_J$ maximum, rated $V_{DRM}$ applied		10.0	mA
Maximum rate of rise of turned-on current	dl/dt	$T_J = T_J \text{ maximum, I-}$ applied	<sub>TM</sub> = 400 A, rated V <sub>DRM</sub>	500	A/µs

THERMAL AND MECHANICAL SPECIFICATIONS							
PARAMETER	3	SYMBOL	TEST CONDITIONS	VS-VSKH320	UNITS		
Junction oper temperature r	rating and storage range	T <sub>J</sub> , T <sub>Stg</sub>		-40 to +130	°C		
	Maximum thermal resistance, junction to case per junction		DC operation	0.125	K/W		
Typical thermal resistance, case to heatsink per module		R <sub>thCS</sub>	Mounting surface flat, smooth, and greased	0.02	- NVV		
Mounting torque	MAGN-A-PAK to heatsink		A mounting compound is recommended and the torque should be rechecked after a	4 to 6	Nm		
± 10 %	busbar to MAGN-A-PAK		period of about 3 hours to allow for the spread of the compound.	4 10 0	INIII		
Approximate weight				500	g		
				17.8	oz.		
Case style				MAGN-A-PA	K		

△R CONDUCTION PER JUNCTION											
DEVICES	SINUS	SINUSOIDAL CONDUCTION AT T <sub>J</sub> MAXIMUM					RECTANGULAR CONDUCTION AT T <sub>J</sub> MAXIMUM				UNITS
DEVICES	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	UNITS
VS-VSKH320-	0.009	0.010	0.014	0.020	0.032	0.007	0.011	0.015	0.020	0.033	K/W

#### Note

• Table shows the increment of thermal resistance R<sub>thJC</sub> when devices operate at different conduction angles than DC

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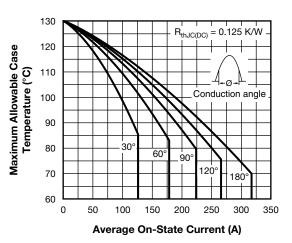


Fig. 1 - Current Ratings Characteristics

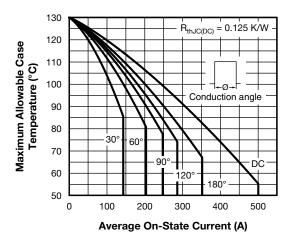


Fig. 2 - Current Ratings Characteristics

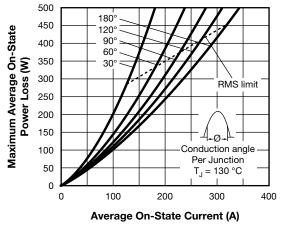


Fig. 3 - On-State Power Loss Characteristics

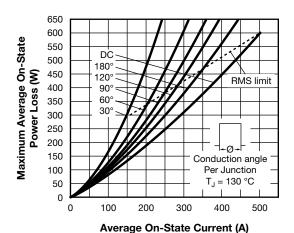


Fig. 4 - On-State Power Loss Characteristics

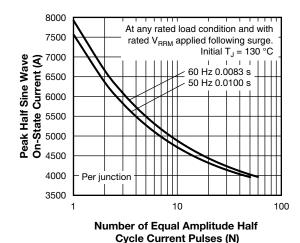


Fig. 5 - Maximum Non-Repetitive Surge Current

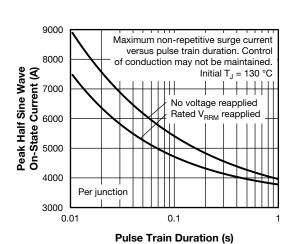


Fig. 6 - Maximum Non-Repetitive Surge Current

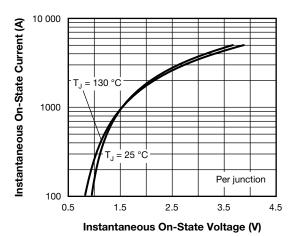


Fig. 7 - On-State Voltage Drop Characteristics

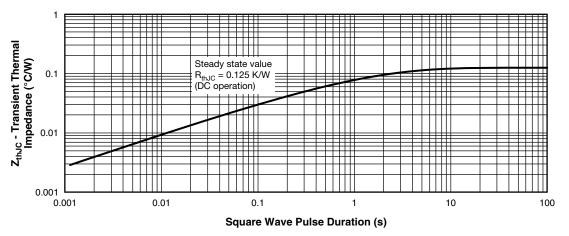
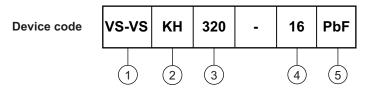


Fig. 8 - Thermal Impedance  $Z_{thJC}$  Characteristics

### **ORDERING INFORMATION TABLE**



- Vishay Semiconductors product
- Circuit configuration (see end of datasheet)
- Current rating
- Voltage code x 100 = V<sub>RRM</sub> (see Voltage Ratings table)
- 5 • None = Standard production
  - PbF = Lead (Pb)-free

#### Note

To order the optional hardware go to <a href="https://www.vishay.com/doc?95172">www.vishay.com/doc?95172</a>



# VS-VSKH320-16PbF Series

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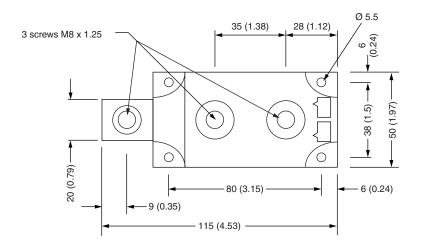
CIRCUIT CONFIGURATION						
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING				
SCR/diode doubler circuit, positive control	КН	VSKH				

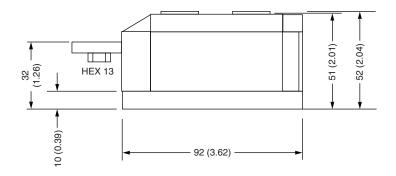
LINKS TO RELATED DOCUMENTS					
Dimensions <u>www.vishay.com/doc?95086</u>					
Application Note	www.vishay.com/doc?95557				



## **MAGN-A-PAK**

### **DIMENSIONS** in millimeters (inches)





#### Notes

- Dimensions are nominal
- Full engineering drawings are available on request
- UL identification number for gate and cathode wire: UL 1385
- UL identification number for package: UL 94 V-0



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