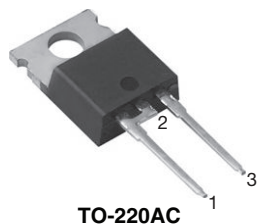
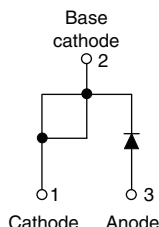


High Performance Schottky Rectifier, 18 A


TO-220AC


FEATURES

- 175 °C T_J operation
- Low forward voltage drop
- High frequency operation
- High purity, high temperature epoxy encapsulation for enhanced mechanical strength and moisture resistance
- Guard ring for enhanced ruggedness and long term reliability
- AEC-Q101 qualified meets JESD 201 class 2 whisker test
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

PRIMARY CHARACTERISTICS

$I_{F(AV)}$	18 A
V_R	35 V, 40 V, 45 V
V_F at I_F	0.53 V
I_{RM} max.	25 mA at 125 °C
T_J max.	175 °C
E_{AS}	24 mJ
Package	TO-220AC
Circuit configuration	Single

DESCRIPTION

The VS-18TQ... Schottky rectifier series has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature. Typical applications are in switching power supplies, converters, freewheeling diodes, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	18	A
V_{RRM}	Range	35 to 45	V
I_{FSM}	$t_p = 5 \mu s$ sine	1800	A
V_F	18 A _{pk} , $T_J = 125$ °C	0.53	V
T_J	Range	-55 to +175	°C

VOLTAGE RATINGS

PARAMETER	SYMBOL	VS-18TQ035HN3	VS-18TQ040HN3	VS-18TQ045HN3	UNITS
Maximum DC reverse voltage	V_R	35	40	45	V
Maximum working peak reverse voltage	V_{RWM}				

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current See fig. 5	$I_{F(AV)}$	50 % duty cycle at $T_C = 149$ °C, rectangular waveform	18	A
Maximum peak one cycle non-repetitive surge current See fig. 7	I_{FSM}	5 μs sine or 3 μs rect. pulse	1800	
		10 ms sine or 6 ms rect. pulse	390	
Non-repetitive avalanche energy	E_{AS}	$T_J = 25$ °C, $I_{AS} = 3.6$ A, $L = 3.7$ mH	24	mJ
Repetitive avalanche current	I_{AR}	Current decaying linearly to zero in 1 μs Frequency limited by T_J maximum $V_A = 1.5 \times V_R$ typical	3.6	A

**ELECTRICAL SPECIFICATIONS**

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop See fig. 1	V _{FM} ⁽¹⁾	18 A	T _J = 25 °C	0.60	V
		36 A		0.72	
		18 A	T _J = 125 °C	0.53	
		36 A		0.67	
Maximum reverse leakage current See fig. 2	I _{RM} ⁽¹⁾	T _J = 25 °C	V _R = Rated V _R	2.5	mA
		T _J = 125 °C		25	
Maximum junction capacitance	C _T	V _R = 5 V _{DC} (test signal range 100 kHz to 1 MHz) 25 °C		1400	pF
Typical series inductance	L _S	Measured lead to lead 5 mm from package body		8	nH
Maximum voltage rate of change	dV/dt	Rated V _R		10 000	V/μs

Note

⁽¹⁾ Pulse width < 300 μ s, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	T _J , T _{Stg}		-55 to 175	°C
Maximum thermal resistance, junction to case	R _{thJC}	DC operation See fig. 4	1.50	°C/W
Typical thermal resistance, case to heatsink	R _{thCS}	Mounting surface, smooth and greased	0.50	
Approximate weight			2	g
			0.07	oz.
Mounting torque	minimum		6 (5)	kgf · cm (lbf · in)
	maximum		12 (10)	
Marking device		Case style TO-220AC	18TQ035H	
			18TQ040H	
			18TQ045H	

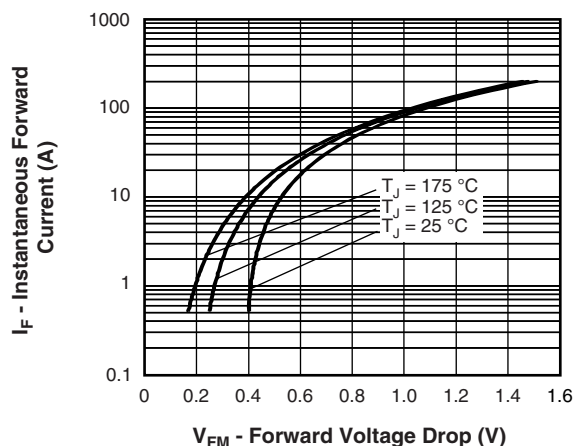


Fig. 1 - Maximum Forward Voltage Drop Characteristics

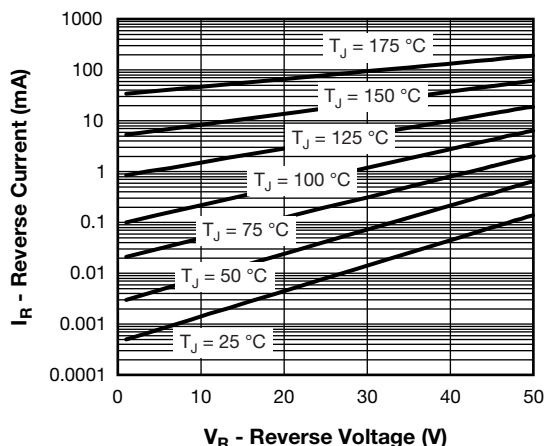


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

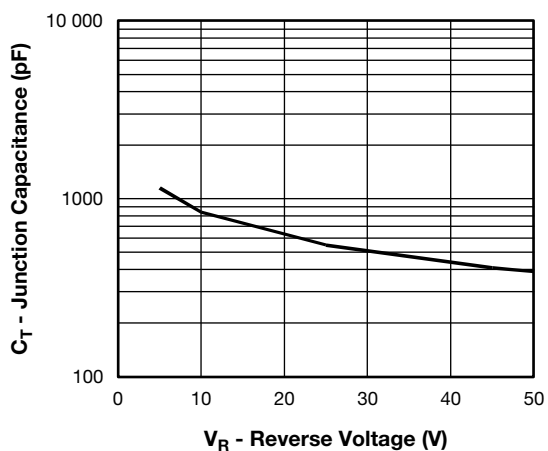
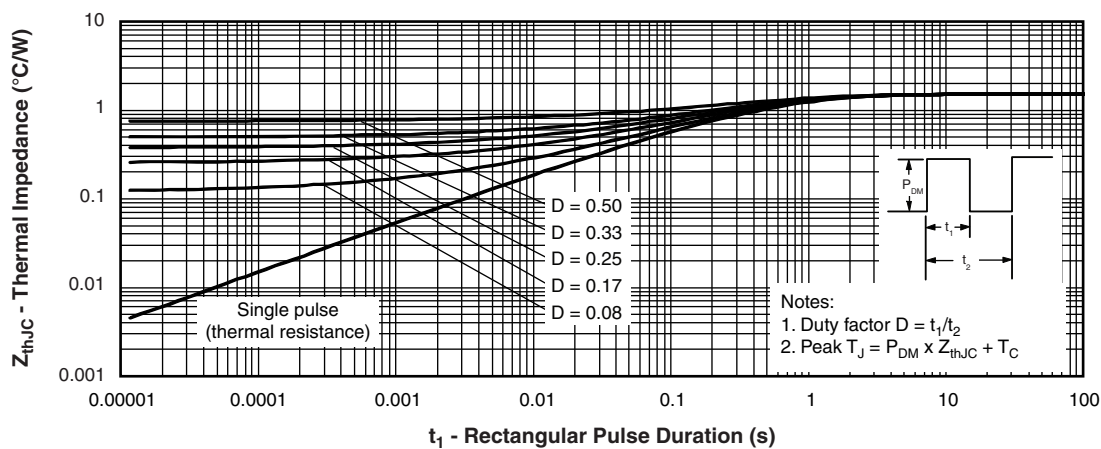


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

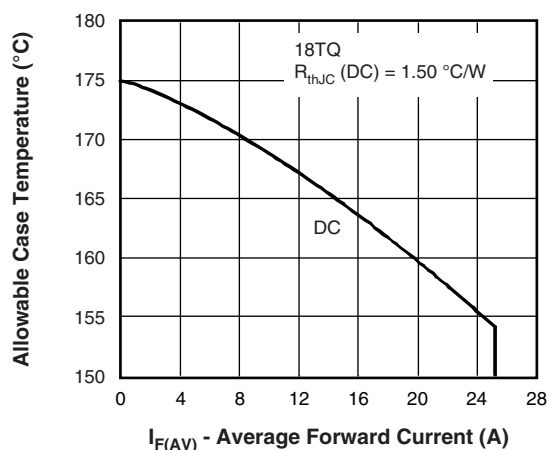


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

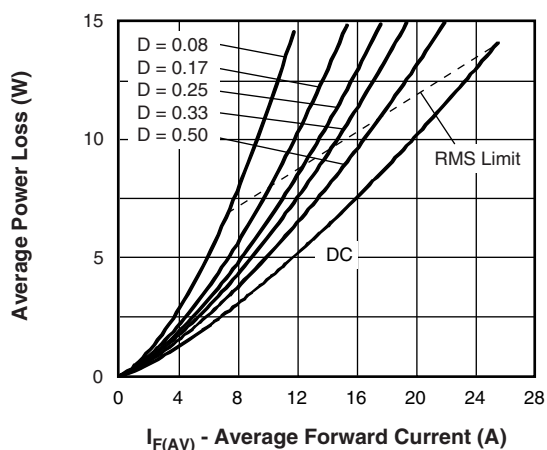


Fig. 6 - Forward Power Loss Characteristics

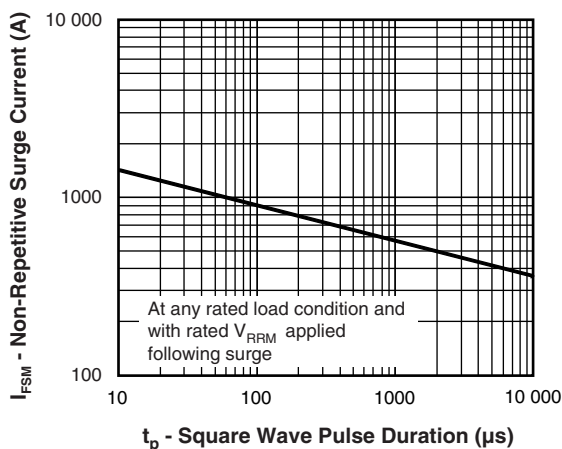


Fig. 7 - Maximum Non-Repetitive Surge Current



Fig. 8 - Unclamped Inductive Test Circuit

**ORDERING INFORMATION TABLE**

Device code	VS-	18	T	Q	045	H	N3
	①	②	③	④	⑤	⑥	⑦

- | | | | |
|----------|---|---|------------|
| 1 | - | Vishay Semiconductors product | |
| 2 | - | Current rating (18 = 18 A) | |
| 3 | - | Package: | |
| | | T = TO-220 | |
| 4 | - | Schottky "Q" series | 035 = 35 V |
| 5 | - | Voltage ratings | 040 = 40 V |
| | | | 045 = 45 V |
| 6 | - | H = AEC-Q101 qualified | |
| 7 | - | Environmental digit | |
| | | • N3 = Halogen-free, RoHS-compliant, and totally lead (Pb)-free | |

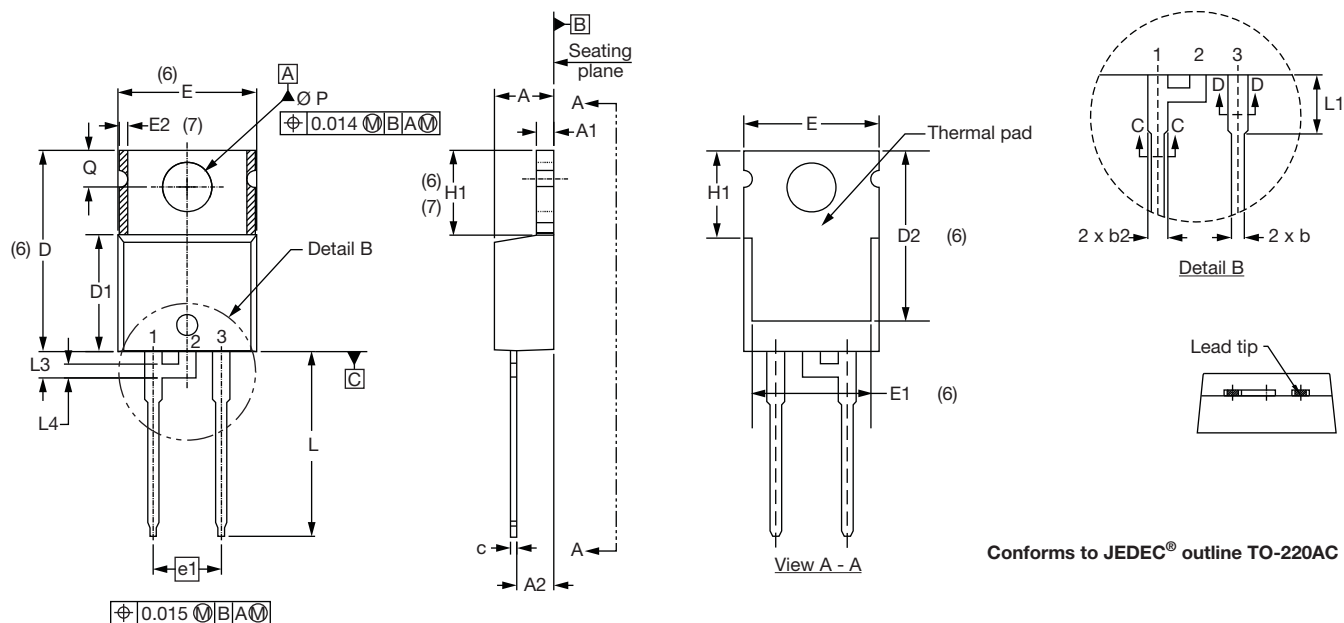
ORDERING INFORMATION (Example)			
PREFERRED P/N	QUANTITY PER T/R	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION
VS-18TQ035HN3	50	1000	Antistatic plastic tube
VS-18TQ040HN3	50	1000	Antistatic plastic tube
VS-18TQ045HN3	50	1000	Antistatic plastic tube

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95221
Part marking information	TO-220AC-N3 www.vishay.com/doc?95068
SPICE model	www.vishay.com/doc?96209



TO-220AC

DIMENSIONS in millimeters and inches



Conforms to JEDEC® outline TO-220AC

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
c	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6
E	10.11	10.51	0.398	0.414	3, 6

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
E1	6.86	8.89	0.270	0.350	6
E2	-	0.76	-	0.030	7
e1	4.88	5.28	0.192	0.208	
H1	5.84	6.86	0.230	0.270	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
L3	1.78	2.13	0.070	0.084	
L4	0.76	1.27	0.030	0.050	2
Ø P	3.54	3.73	0.139	0.147	
Q	2.60	3.00	0.102	0.118	

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimension: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimension E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, D2 (minimum) where dimensions are derived from the actual package outline



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