

1200 V Power SiC Gen 3 Merged PIN Schottky Diode, 20 A



LINKS TO ADDITIONAL RESOURCES



PRIMARY CHARACTERISTICS					
I _F 20 A					
V_R	1200 V				
V _F at I _F at 25 °C, typ.	1.35 V				
T _J max.	175 °C				
I _R at V _R at 175 °C	12 µA				
$Q_{C} (V_{R} = 800 V)$	107 nC				
Package	TO-220AC 2L				
Circuit configuration	Single				

FEATURES

· Majority carrier diode using Schottky technology on SiC wide band gap material



 Improved V_F and efficiency by thin wafer RoHS technology

HALOGEN **FREE**

 Positive V_F temperature coefficient for easy paralleling

- Virtually no recovery tail and no switching losses
- Temperature invariant switching behavior
- 175 °C maximum operating junction temperature
- · MPS structure for high ruggedness to forward current surge events
- Meets JESD 201 class 1A whisker test
- Solder bath temperature 275 °C maximum, 10 s per JESD 22-B106
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION / APPLICATIONS

Wide band gap SiC based 1200 V Schottky diode, designed for high performance and ruggedness.

Optimum choice for high speed hard switching and efficient operation over a wide temperature range, it is also recommended for all applications suffering from Silicon ultrafast recovery behavior.

Typical applications include AC/DC PFC and DC/DC ultra high frequency output rectification in FBPS and LLC

MECHANICAL DATA

Case: TO-220AC 2L

Molding compound meets UL 94 V-0 flammability rating

Base P/N-M3 - halogen-free, RoHS-compliant

Terminals: matte tin plated leads, solderable per J-STD-002 and JESD 22-B102

Mounting torque: 10 in-lbs maximum

MAXIMUM RATINGS (T _A = 25 °C unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS		
Peak repetitive reverse voltage	V_{RRM}		1200	V		
Continuous forward current	I _F ⁽¹⁾	$T_C = 132 ^{\circ}C (DC)$	00	Α		
Continuous forward current	I _F ⁽²⁾	$T_C = 145 ^{\circ}C (DC)$	20	4		
DC blocking voltage	V_{DC}		1200	V		
Repetitive peak forward current	I _{FRM}	T_C = 25 °C, f = 50 Hz, square wave, DC = 25 %	75	Α		
Non-repetitive peak forward surge current	I _{FSM}	$T_C = 25$ °C, $t_p = 10$ ms, half sine wave	180	Α		
Non-repetitive peak forward surge current		$T_C = 110$ °C, $t_p = 10$ ms, half sine wave	145	A		
	P _{tot} (1)	$T_C = 25 ^{\circ}C$	130	W		
Dower discipation		T _C = 110 °C	57	۷V		
Power dissipation	P _{tot} (2)	$T_C = 25 ^{\circ}C$	188	w		
		T _C = 110 °C	81			
I ² t value	∫i ² dt	T _C = 25 °C	162	A ² s		
i-t value		T _C = 110 °C	105	K-8		
Operating junction and storage temperatures	T _J ⁽³⁾ , T _{Stg}		-55 to +175	°C		

Notes

- (1) Based on maximum Rth
- (2) Based on typical Rth
- (3) The heat generated must be less than the thermal conductivity from junction-to-ambient: $dP_D/dT_J < 1/R_{\theta,JA}$



ELECTRICAL SPECIFICATIONS (T _J = 25 °C unless otherwise specified)							
PARAMETER SYMBOL		TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS	
		I _F = 20 A	-	1.35	1.5		
Forward voltage	V_{F}	I _F = 20 A, T _J = 150 °C	-	1.73	2.0	V	
		I _F = 20 A, T _J = 175 °C	-	1.85	-		
		$V_R = V_R$ rated	-	1.5	110		
Reverse leakage current	I _R	V _R = V _R rated, T _J = 150 °C	-	7	250	μΑ	
		V _R = V _R rated, T _J = 175 °C	-	12	=.		
Tatal conscitores	С	V _R = 1 V, f = 1 MHz	-	1200	-	~F	
Total capacitance		V _R = 800 V, f = 1 MHz	-	73	-	pF	
Total capacitive charge	Q _C	V _R = 800 V, f = 1 MHz	-	107	-	nC	

THERMAL - MECHANICAL SPECIFICATIONS (T _A = 25 °C unless otherwise specified)							
PARAMETER SYMBOL TEST CONDITIONS MIN. TYP. MAX. UNITS							
Thermal resistance, junction-to-case	R _{thJC}		-	0.8	1.15	°C/W	
Marking device	3C20ET12T						

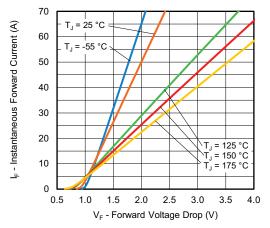


Fig. 1 - Typical Forward Voltage Drop Characteristics

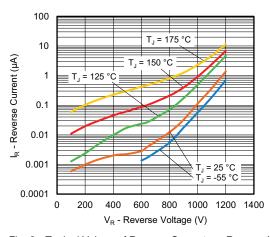


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

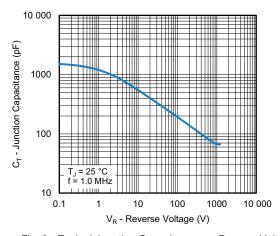


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

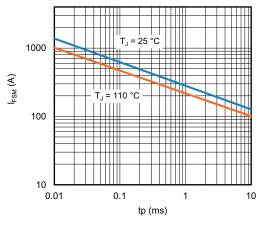


Fig. 4 - Non-Repetitive Peak Forward Surge Current vs. Pulse Duration (Square Wave)

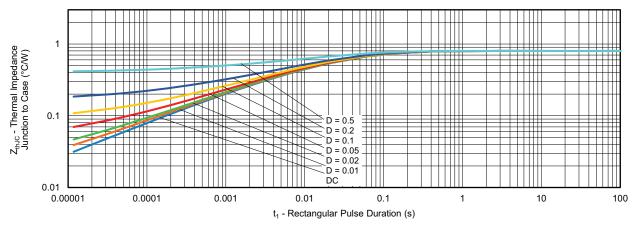


Fig. 5 - Typical Thermal Impedance Z_{thJC} Characteristics

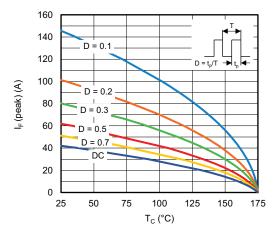


Fig. 6 - Peak Forward Current vs. Maximum Allowable Case Temperature

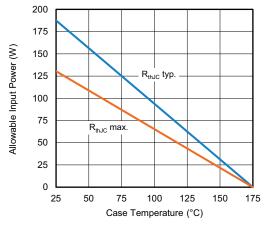


Fig. 7 - Forward Power Loss Characteristics

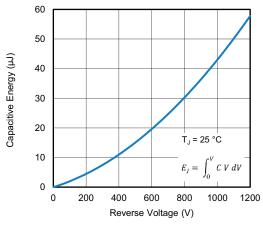


Fig. 8 - Typical Capacitive Energy vs. Reverse Voltage

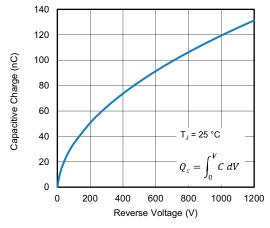
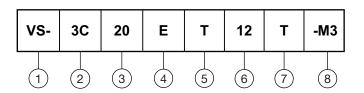


Fig. 9 - Typical Capacitive Charge vs. Reverse Voltage



ORDERING INFORMATION TABLE

Device code



1 - Vishay Semiconductors product

- 3C = SiC diode, Generation 3

Current rating (20 = 20 A)

- E = single diode

5 - Package TO-220

6 - Voltage rating: (12 = 1200 V)

7 - T = true 2 pin

8 - Environmental digit:

-M3 = halogen-free, RoHS-compliant, and termination lead (Pb)-free

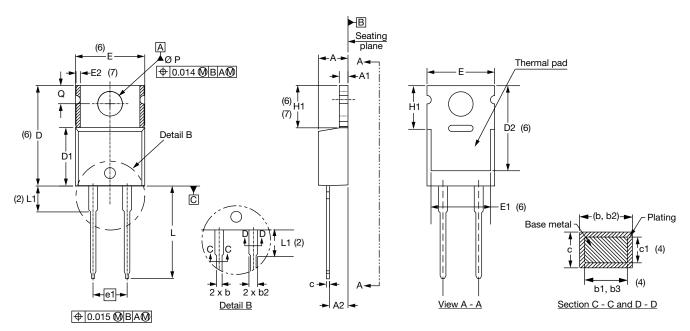
ORDERING INFORMATION		
PREFERRED P/N	BASE QUANTITY	PACKAGING DESCRIPTION
VS-3C20ET12T-M3	50/tube	Antistatic plastic tubes

LINKS TO RELATED DOCUMENTS				
Dimensions <u>www.vishay.com/doc?96069</u>				
Part marking information	www.vishay.com/doc?95391			



TO-220AC 2L

DIMENSIONS in millimeters and inches



SYMBOL	MILLIM	MILLIMETERS		INCHES		
STIMBOL	MIN.	MAX.	MIN.	MAX.	NOTES	
Α	4.25	4.65	0.167	0.183		
A1	1.14	1.40	0.045	0.055		
A2	2.56	2.92	0.101	0.115		
b	0.69	1.01	0.027	0.040		
b1	0.38	0.97	0.015	0.038	4	
b2	1.20	1.73	0.047	0.068		
b3	1.14	1.73	0.045	0.068	4	
С	0.36	0.61	0.014	0.024		
c1	0.36	0.56	0.014	0.022	4	
D	14.85	15.25	0.585	0.600	3	
D1	8.38	9.02	0.330	0.355		
D2	11.68	12.88	0.460	0.507	6	
E	10.11	10.51	0.398	0.414	3, 6	

SYMBOL	MILLIMETERS		INC	NOTES	
STWIDOL	MIN.	MAX.	MIN.	MAX.	NOTES
E1	6.86	8.89	0.270	0.350	6
E2	ı	0.76	-	0.030	7
e1	4.88	5.28	0.192	0.208	
H1	5.84	6.86	0.230	0.270	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
ØΡ	3.54	3.73	0.139	0.147	
Ø	2.60	3.00	0.102	0.118	

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimension: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- $^{(7)}$ Dimension E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC® TO-220, except D2, where JEDEC® minimum is 0.480"



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