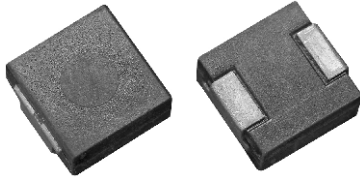


10 % DCR Tolerance, Low Profile, Power Inductors



Manufactured under one or more of the following:
US Patents; 6,198,375/6,204,744/6,449,829/6,460,244.
 Several foreign patents, and other patents pending.

STANDARD ELECTRICAL SPECIFICATIONS			
L₀ INDUCTANCE ± 20 % AT 100 kHz, 0.25 V, 0 A (μH)	DCR ± 10 % AT 25 °C (mΩ)	HEAT RATING CURRENT DC TYP. (A) ⁽³⁾	SATURATION CURRENT DC TYP. (A) ⁽⁴⁾
0.10	1.37	32.5	60
0.20	2.34	24	41
0.33	3.20	20	30
0.47	3.86	17.5	26
0.68	5.20	15.5	25
0.82	7.41	13	24
1.0	8.44	11	22
1.5	14.50	9	18
2.2	17.73	8	14
3.3	28.21	6	13.5
4.7	37.11	5.5	10
8.2	61.47	4	7.5
10	97.71	3	7.0

Notes

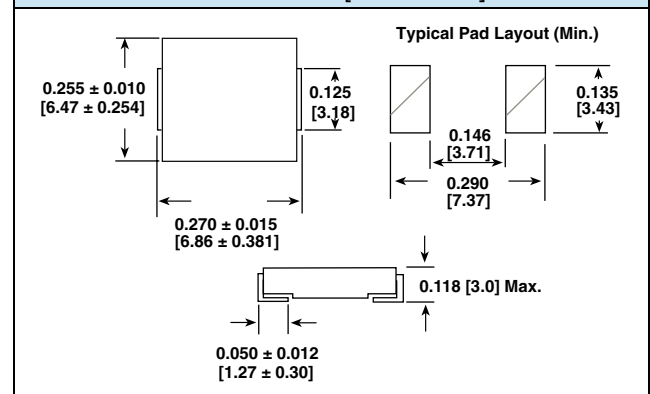
- (1) All test data is referenced to 25 °C ambient
- (2) Operating temperature range - 55 °C to + 125 °C
- (3) DC current (A) that will cause an approximate ΔT of 40 °C
- (4) DC current (A) that will cause L₀ to drop approximately 20 %
- (5) The part temperature (ambient + temp rise) should not exceed 125 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application.

FEATURES

- Lowest molded height (3.0 mm) in this package footprint
- Shielded construction
- Frequency range up to 5.0 MHz
- Lowest DCR/μH, in this package size
- Handles high transient current spikes without saturation
- Ultra low buzz noise, due to composite construction
- Encapsulated body offers improved environmental protection and moisture resistance
- Higher dielectric withstanding voltage vs. IHLP
- Flame retardant encapsulant (UL 94 V-0)
- Corrosion resistant package
- Compliant to RoHS directive 2002/95/EC


**RoHS
COMPLIANT**
APPLICATIONS

- Tolerance DCR for current sense applications
- Improved current balance in phased power supplies
- Improved thermal management
- PDA/notebook/desktop/server and battery powered devices
- High current, low profile POL converters
- DC/DC converters in distributed power systems
- DC/DC converter for Field Programmable Gate Array (FPGA)

DIMENSIONS in inches [millimeters]

DESCRIPTION

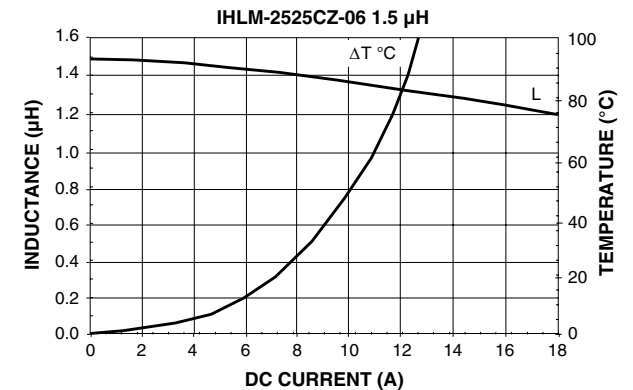
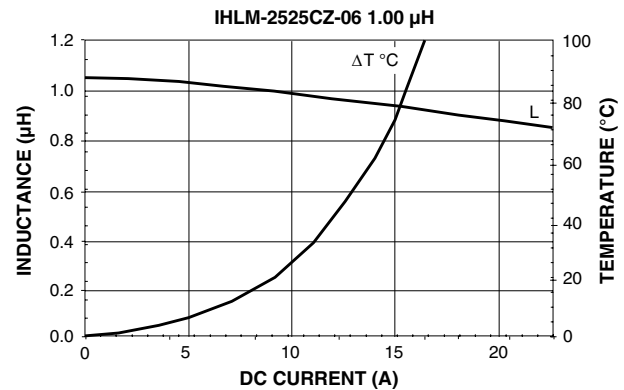
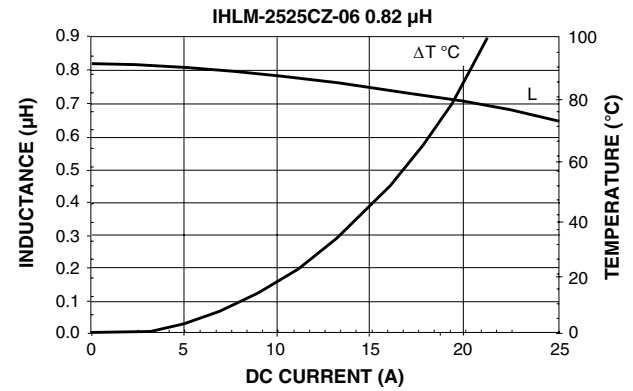
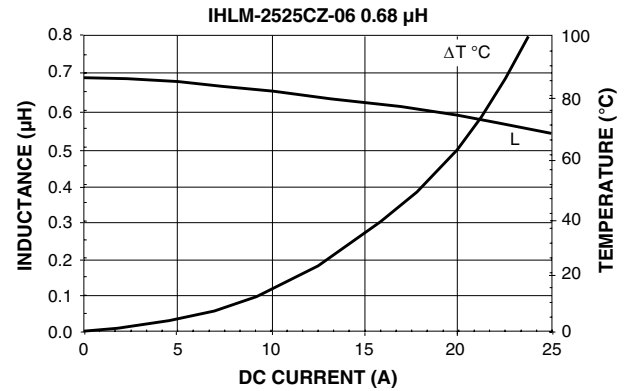
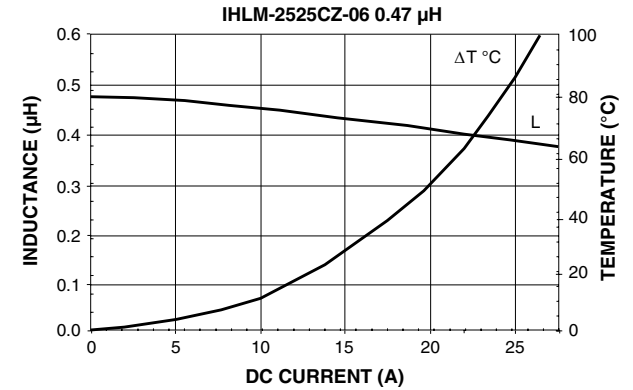
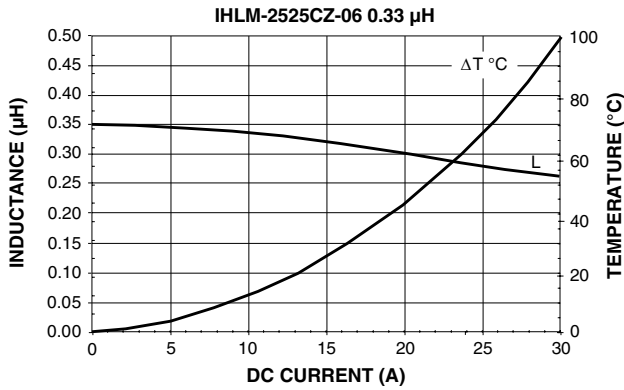
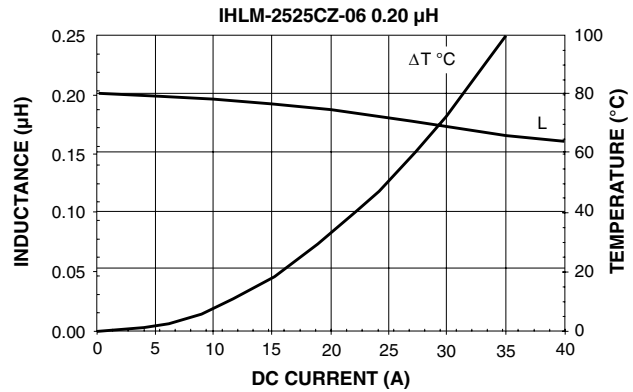
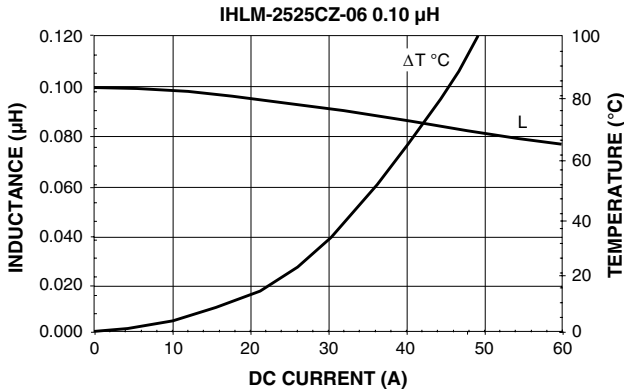
IHLM-2525CZ-06	1.0 μH	± 20 %	ER	e3
MODEL	INDUCTANCE VALUE	INDUCTANCE TOLERANCE	PACKAGE CODE	JEDEC LEAD (Pb)-FREE STANDARD

GLOBAL PART NUMBER

I	H	L	M	2	5	2	5	C	Z	E	R	1	R	0	M	0	6
PRODUCT FAMILY				SIZE				PACKAGE CODE		INDUCTANCE VALUE			TOL	SERIES			

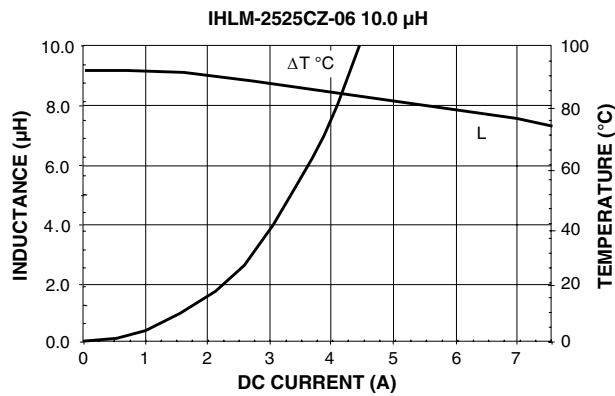
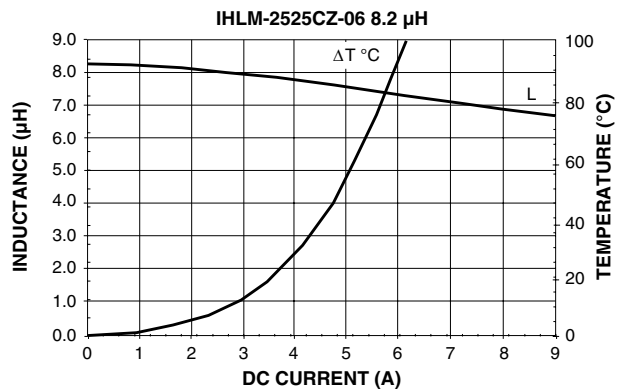
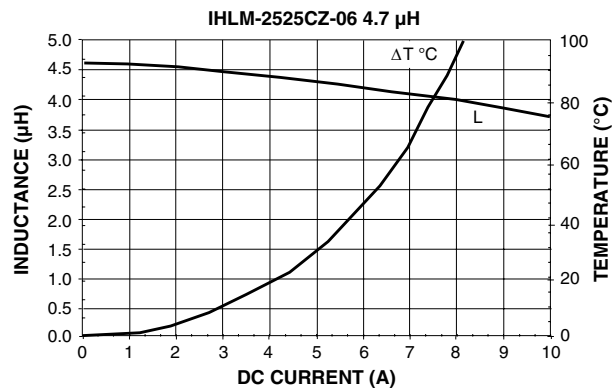
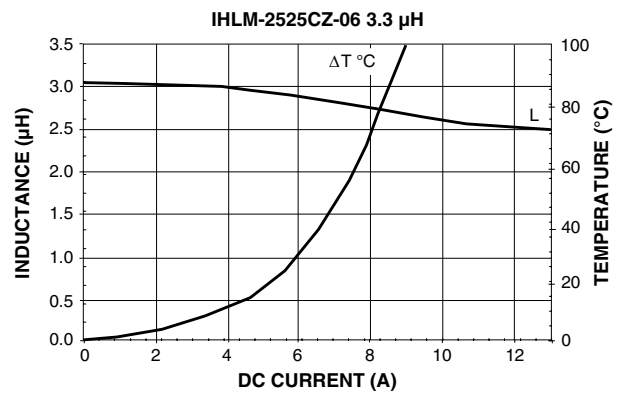
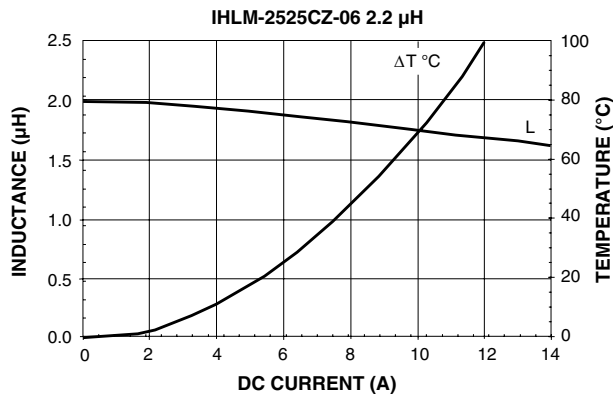


PERFORMANCE GRAPHS





PERFORMANCE GRAPHS





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