Overcoming PCMCIA Power Limits in Modem Designs

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High-value tantalum capacitors supply the high current pulses demanded during GSM/GPRS transmission bursts, while providing stability over time and temperature.

Demand for wireless network access to support mobile computing requirements is growing at a rapid pace. As a result, the Global System for Mobile Communication (GSM) telecommunications network and, by extension, the General Packet Radio Service (GPRS), have become ubiquitous. With this 2.5G infrastructure being deployed at an accelerated pace to support growth in network-enabled PDAs and mobile phones comes a demand for peripheral devices to enable network access for laptop computers. Engineers have been turning to the Personal Computer Memory Card International Association (PCMCIA) bus as an obvious solution in the implementation of GSM modem designs.

GSM transmission is comprised of relatively short bursts that require high current. Transmitters employed in this application operate at ~ 3 V with up to 2 A of peak current. However, the PCMCIA bus specification limits the available current to1 A max - a specification that is clearly insufficient to meet this demand. This then forces the designer to consider the use of bulk capacitance (1000 µF to 5500 µF) to maintain voltage and supply the requisite current during transmission.

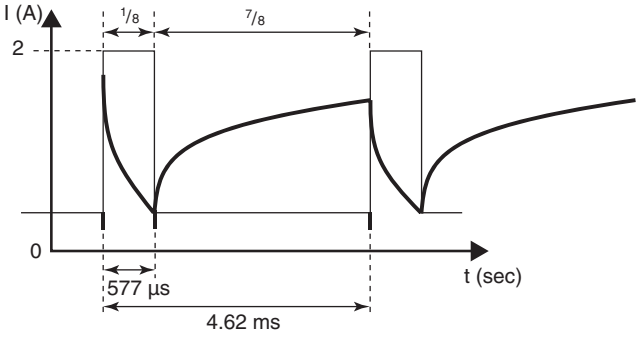

Fig. 1. During GSM transmissions, the power amplifier transmits a pulse lasting 577 µs. The capacitor supplying this current must charge during the remaining portion of the cycle.

The capacitor solutions available to designers of PCMCIA modem cards have been limited to electrochemical doublelayer capacitor (EDLC) technology, which offers very high capacitance. But, EDLCs have certain drawbacks such as high effective series resistance (ESR) along with instability over time and temperature, which hampers their use in pulsed applications.

However, tantalum capacitors can now offer an alternative to EDLCs. Tantalums feature a high capacitance × voltage (CV) product, are volumetrically efficient and have low ESR. Until recently, these devices could not be considered in the wireless modem application because they were limited in capacitance to 680 µF or less - clearly an unsuitable choice. But the development of ultrahigh-capacitance tantalum capacitors with values up to 3300 µF in a surface-mount package now offers modem designers an attractive alternative to EDLCs.

In this article, the discussion is limited to GSM modems implemented using the PCMCIA bus. Nevertheless, the concepts presented are also relevant to pulsed power applications using other power-limited bus structures such as the USB bus.

PROBLEM SUMMARY

As shown in **Fig. 1**, the GSM signal is transmitted over the carrier at a rate of 216 Hz (4.62 ms PRI [pulse repetition interval]), on one-time division comprising one-eighth of the cycle yielding a pulse width of 577 µs. This requires that the capacitor use the remaining seven-eighths of the cycle to recharge. For the purposes of this example, let's assume that the current required by the power amplifier is 2 A. In a worst-case analysis, we must assume that the power required during the transmission is completely supplied by a capacitor, thus ignoring the current available from the PCMCIA bus.

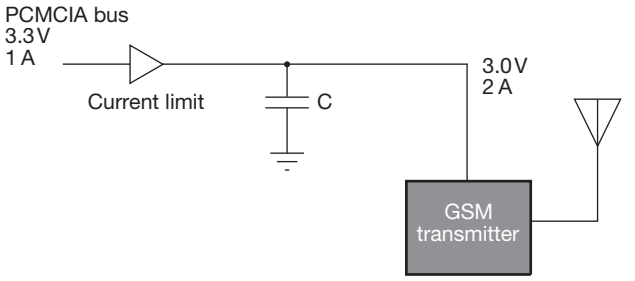

Fig. 2. The capacitor in this simplified circuit diagram must deliver the required current to the GSM transmitter while limiting the voltage drop to 0.3 V or less.

With a working voltage of 3.3 V available from the PCMCIA bus, and with a minimum input voltage of 3 V required by many power amplifiers, a maximum voltage drop of 0.3 V can be allowed. A review of **Table 1** summarizes the design constraints, while **Fig. 2** depicts the simplified circuit diagram.

The voltage drop in the circuit comprises two components - the IR drop associated with the capacitor's internal resistance (as approximated by ESR) and the drop in capacitor voltage at the end of the pulse. Thus the total voltage drop is given by:

$$V = IR \times I\left(\frac{t}{C}\right),$$

where V is the voltage drop (V), I is the current (A), R is the internal resistance of the capacitor – ESR (Ω), t is the pulse width (sec) and C is the capacitance (F).

DESIGN PARAMETER	VALUE
PCMCIA Voltage	3.3 V max
PCMCIA Current	1.0 A max
PA input voltage	3.0 V min
PA peak input current	2.0 A max
GSM pulse width	577 µs min

Table 1. Design problem summary

To consider the design options available, examine the data provided in **Table 2**. We shall discuss four potential solutions to this design problem. Two options will be used to demonstrate the impact of tantalum solutions on this design, while the other two will focus on the results of using EDLC technology.

The first option allows the use of three tantalum capacitors providing a total of 6.6 mF capacitance, while the second option uses two tantalum capacitors for a combined 4.4 mF total capacitance. In addition to total capacitance, these two options differ in ESR.

Option 3 is an EDLC providing 22 mF of rated capacitance. Option 4 offers increased capacitance and lower ESR than Option 3.

The internal composition of an EDLC is such that the device responds relatively slowly to an electric field compared to capacitors that use traditional dielectrics. Thus, the usable (or effective) capacitance is a strong function of pulse width as shown in **Fig. 3**. Given the pulse width used in GSM transmissions (577 µs), the effective capacitance of EDLCs on the market today is between 3 % and 48 % of the rated capacitance value. For this example, we will use the most optimistic projection of effective capacitance for EDLC technology.

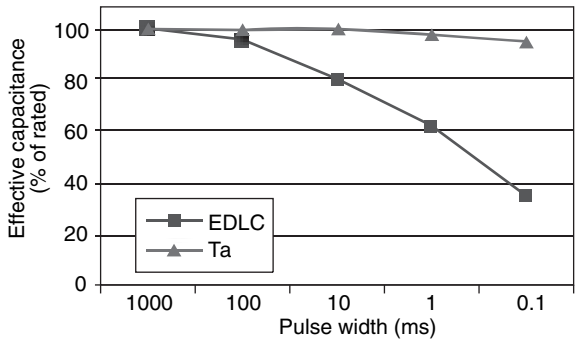

Fig. 3. The effective capacitance of different capacitors technologies varies as a function of pulse width.

CAPACITOR OPTIONS / DESIGN PARAMETERS (FIG.2)	OPTION 1 3 × 2200 µF, 6.3 V TANTALUMS	OPTION 2 2 × 2200 µF, 6.3 V TANTALUMS	OPTION 3 1 × 22 000 µF, 4.5 V EDLC	OPTION 4 1 × 35 000 µF, 5.5 V EDLC
Rated Capacitance (mF)	6.6	4.4	22	35
Effective Capacitance (mF)	6.6	4.4	11	17
Effective ESR (mΩ) at 20 °C	12	18	200	150
Overall size L × W × H (mm)	14.5 × 22.5 × 2	14.5 × 15 × 2	26 × 15 × 2.1	26 × 15 × 4.8
PC board mounting	SMD	SMD	Hand soldered	Hand soldered
Voltage drop (V), GSM pulse	0.19	0.30	0.50	0.37

Table 2. Four potential solutions to the design problem

FOUR OPTIONS

Option 1. Designing three tantalum capacitors in parallel will provide a total capacitance of 6.6 mF. **Fig. 4** illustrates the equivalent circuit showing both capacitance as well as the devices' internal resistance. Since the devices are in parallel, the total capacitance is given by:

$$C_T = C1 + C2 + C3 = 6.6 \text{ mF}$$

The total effective internal ESR is given by:

$$R_T = \frac{1}{\left(\frac{1}{R1} \times \frac{1}{R2} \times \frac{1}{R3}\right)}$$

when R1 = R2 = R3, the equation simplifies to:

$$R_T = \frac{R}{3}$$

Thus, the $ESR = \frac{35\ m\Omega}{3} = \sim 12\ m\Omega$

And we have:

$$V = (2\ A \times 0.012\ \Omega) + \left(2\ A \times \left(\frac{0.000557\ s}{0.0066\ F}\right)\right)$$

$$V = 0.02\ V + 0.17\ V = 0.19\ V$$

As can be seen in these calculations, the low internal resistance of tantalum capacitors results in minimal internal IR losses. The resulting 0.19 V total voltage drop is within the design constraint of 0.3 V maximum allowed.

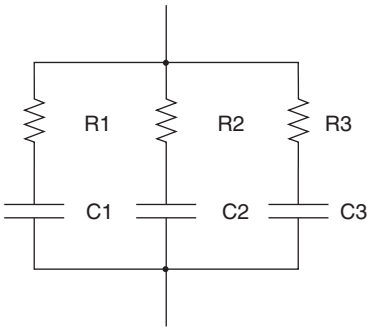

Fig. 4. Paralleling three tantalum capacitors provides 6.6 mF of capacitance with an effective ESR of 12 mΩ.

Option 2. As demonstrated in Option 1, effective ESR for Option 2 is calculated as follows:

$$ESR = \frac{35\ m\Omega}{2} = \sim 18\ m\Omega$$

And we have:

$$V = 0.04\ V + 0.26\ V = 0.3\ V$$

Although within the design constraint, the voltage drop of 0.3 V will provide no margin in the design.

Option 3. Next we examine the EDLC case and find that:

$$V = 0.4\ V + 0.1\ V = 0.5\ V$$

The high ESR becomes the dominant contribution to the total voltage drop, and the resultant total voltage drop of 0.50 V is in excess of what the circuit can allow.

Option 4. Lastly, examining the higher capacitance/lower ESR EDLC solution:

$$V = 0.3\ V + 0.07\ V = 0.37\ V$$

As one might expect, the lower ESR has a positive impact on the calculated voltage drop. However, increases in capacitance have shown little effect on overall performance. Although lower than in Option 3, the total voltage drop in Option 4 is still in excess of the design constraints. An additional drawback of this solution is the size of the device. At 4.8 mm in height, it is not a desirable solution for use within the form-factor of the PCMCIA card standard.

To overcome the excessive voltage drop associated with ESR, designers incorporating EDLC technology must consider the use of additional circuitry such as a dc-dc boost converter. This design option will add additional cost to the circuitry while unnecessarily using up valuable board space.

As mentioned previously, the circuit's dependence on ESR is an important design consideration. Calculations examined in the various options were based on initial ESR specified at 25 °C. A more thorough examination of ESR's impact to the circuit must take into consideration the following:

- ESR stability over temperature
- ESR variability due to aging over the life of the end product

A survey of technology available today shows that ESR in EDLCs can vary by up to 400 % over their specified operating temperatures, as compared to tantalum, whose ESR remains within specification over the same temperature range. The design engineer must also take into consideration that EDLC ESR increases with age over the life of the component.

ESR COMPARISON	TANTALUM 2.2 mF, 6.3 V	EDLC 2.2 mF, 4.5 V
ESR, 100 kHz; 25 °C	35 mΩ	200 mΩ
Operating temp range	- 55 °C to + 85 °C	- 20 °C to + 70 °C
Temp range for comarison	- 20 °C to + 70 °C	
Variation over temp range	0 %	400 %
Variation over time	0 %	300 %

Table 3. ESR performance

Table 3 compares ESR performance for tantalum and EDLC technologies. For tantalum, ESR is stable over both temperature and time, with no change in specification over the full operating temperature or life test. Given the operating environment for PCMCIA cards within laptop computers, ESR stability to 85 °C is highly desirable.

By contrast, ESR variation in EDLC technology is problematic in pulsed applications. As shown in our circuit analysis, the IR drop associated with ESR in the EDLC case is already the dominant contributor to the overall voltage drop. Given the high variability of ESR, designing the circuit with sufficient margin under all conditions would prove difficult.

In addressing the need for bulk capacitance in pulsed power applications, designers must realize that ESR is a key factor. Ultrahigh capacitance, or even excess capacitance, cannot overcome the losses in efficiency that are associated with high ESR solutions. Overcoming these losses with additional circuitry - as in the use of a boost converter - is not only costly, but uses valuable board space, adding to the bulk of the design. Alternatively, selecting a solution with *sufficient* capacitance coupled with low ESR will yield a more efficient, cost-effective solution.

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