Axial and Radial Leaded Multilayer Ceramic Capacitors for General Purpose
Class 1, Class 2, and Class 3, 50 V<sub>DC</sub>, 100 V<sub>DC</sub>, 200 V<sub>DC</sub>, 500 V<sub>DC</sub>

CONSTRUCTION AND ORDERING INFORMATION

INTERNAL CONSTRUCTION
Multilayer ceramic capacitors consist of electrodes, the RoHS interleaved ceramic dielectric and the external terminal connectors. The capacitance is given by the description:

\[
C = \frac{A \cdot n \cdot \varepsilon_r \cdot \varepsilon_0}{d}
\]

- \(A\) = Electrode area
- \(n\) = Number of active layers
- \(d\) = Distance between electrodes
- \(\varepsilon_r\) = Dielectric relative
- \(\varepsilon_0\) = Dielectric constant

Whilst the values “\(A \cdot n\)” and “\(d\)” are respectively determined by the production process, the dielectric constant is a function of the ceramic material used.

LEAD CONFIGURATION

**Axial Size 15 and 20**
Lead wire base material: FeCu
Plating: Electrolytic, tinned

**Radial Size 10, 15 and 20**
Lead wire base material: FeCu
Plating: Matte electrolytic, tinned

<table>
<thead>
<tr>
<th>ORDERING CODE INFORMATION</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Product Type</strong></td>
</tr>
<tr>
<td>-----------------------</td>
</tr>
<tr>
<td>K = Radial led MLCC</td>
</tr>
<tr>
<td>A = Axial led MLCC</td>
</tr>
</tbody>
</table>

For technical questions, contact: cmll@vishay.com

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000
**ELECTRICAL DATA AND DIELECTRIC CHARACTERISTICS**

### DIELECTRIC CHARACTERISTICS

<table>
<thead>
<tr>
<th>Capacitance Range:</th>
<th>Dielectric according to EIA</th>
<th>C0G (NP0)</th>
<th>X7R</th>
<th>Y5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>at 1 MHz, 1 V</td>
<td>According to CECC</td>
<td>CG</td>
<td>C1 (2C1)</td>
<td>2F4</td>
</tr>
<tr>
<td>at 1 kHz, 1 V</td>
<td>10 pF to 1 nF</td>
<td>1.2 nF to 10 nF</td>
<td>100 pF to 1 μF</td>
<td>10 nF to 1 μF</td>
</tr>
<tr>
<td>Tolerance on the Capacitance:</td>
<td>where C ≥ 10 pF</td>
<td>± 5 % (J); ± 10 % (K)</td>
<td>± 10 % (K); ± 20 % (M)</td>
<td>+ 80 %/- 20 % (Z)</td>
</tr>
<tr>
<td>Rated DC Voltage</td>
<td>50 V; 100 V, 200 V; 500 V</td>
<td>250 % of rated voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielectric Strength</td>
<td>When rated voltage is 50 V and 100 V, 250 % of rated voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Insulation Resistance (IR)</td>
<td>When rated voltage is 200 V, 150 % rated voltage + 100 VDC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Coefficient of the Capacitance</td>
<td>0 ppm/K</td>
<td>Refer to diagram</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tolerance of the Temperature Coefficient</td>
<td>± 30 ppm/K</td>
<td>Refer to diagram</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Capacitance Change with Respect to Capacitance at 25 °C</td>
<td>Refer to diagram</td>
<td>± 15 %</td>
<td>+ 22 %/- 82 %</td>
<td></td>
</tr>
<tr>
<td>Dissipation Factor (DF)</td>
<td>0.1 % max. when C ≥ 30 pF at 1 MHz, 1 V; where C ≤ 1000 pF at 1 kHz, 1 V; where C &gt; 1000 pF</td>
<td>≤ 2.5 % at 1 kHz, 1 V</td>
<td>≤ 5 % at 1 kHz, 1 V</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-55 °C to +125 °C</td>
<td>-30 °C to +85 °C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>25 °C ± 15 °C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Aging</td>
<td>None</td>
<td>typical 1 % per time decade</td>
<td>typical 7 % per time decade</td>
<td></td>
</tr>
</tbody>
</table>

**Note**
- The capacitors meet the essential requirements of “EIA 198”.
- Unless stated otherwise all electrical values apply at an ambient temperature of 25 °C ± 3 °C, at barometric pressures 650 mm to 800 mm of mercury, and relative humidity not to exceed 75 %.

### MAIN FEATURES

<table>
<thead>
<tr>
<th>CLASS 1</th>
<th>CLASS 2</th>
<th>CLASS 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>APPLICATION</strong></td>
<td>For temperature compensation of frequency discriminating circuits and filters, coupling and decoupling in high frequency circuits where low losses and narrow capacitance tolerances are demanded.</td>
<td>As coupling and decoupling capacitors for such application where higher losses and a reduced capacitance stability are tolerated.</td>
</tr>
<tr>
<td><strong>CLASSIFICATION</strong></td>
<td>Classification EIA: C0G (NP0)</td>
<td>X7R</td>
</tr>
<tr>
<td></td>
<td>Classification CECC: CG</td>
<td>2C1</td>
</tr>
</tbody>
</table>
**TEMPERATURE CHARACTERISTICS OF CAPACITANCE FOR CLASS 2/3 CERAMIC DIELECTRICS ACCORDING TO CECC 32100**

<table>
<thead>
<tr>
<th>CODE LETTER FOR SUB CATEGORY</th>
<th>MAXIMUM CAPACITANCE CHANGE IN % AT THE SPECIFIED TEMPERATURE RANGE</th>
<th>DESIGNATION OF THE SPECIFIED TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>2C</td>
<td>± 20 %</td>
<td>1</td>
</tr>
<tr>
<td>2F</td>
<td>+ 30 %/- 80 %</td>
<td>4</td>
</tr>
</tbody>
</table>

**TEMPERATURE COEFFICIENT OF CAPACITANCE** (Typical)

---

**C0G (NP0)/(CG)**

**X7R/(2C1)**

**YSV/(2F4)**

For technical questions, contact: cmll@vishay.com

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000
VOLTAGE COEFFICIENT OF CAPACITANCE (Typical)

When rated voltage is 50 V and 100 V

![Graph for C0G (NP0)/(CG) X7R/(2C1) Y5V/(2F4)](image1)

When rated voltage is 200 V and 500 V

![Graph for C0G (NP0)/(CG) X7R/(2C1) Y5V/(2F4)](image2)
DISSIPATION FACTOR VS. TEMPERATURE (Typical)

MINIMUM INSULATION RESISTANCE VS. TEMPERATURE (Typical)
AGING RATE (Typical)

C0G (NP0)/(CG)  

X7R/(2C1)

Y5V/(2F4)
OTHER INFORMATION

STORAGE
The capacitors must not be stored in a corrosive atmosphere where sulfide or chloride gas, acid, alkali, or salt are present. Moisture exposure should also be avoided.

The solderability of the leads is not affected by storage of up to 24 months. Temperature + 10 °C to + 35 °C, relative humidity up to 60 %.

With reference to class 2 ceramic dielectric capacitors, see section Capacitance “Aging” of Ceramic Capacitors this page.

SOLDERING

SOLDERING SPECIFICATIONS

<table>
<thead>
<tr>
<th>Soldering test for capacitors with wire leads: (According to IEC 60068-2-20, solder bath method)</th>
<th>SOLDERABILITY</th>
<th>RESISTANCE TO SOLDERING HEAT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soldering temperature</td>
<td>235 °C ± 5 °C</td>
<td>260 °C ± 5 °C</td>
</tr>
<tr>
<td>Soldering duration</td>
<td>2 s ± 0.5 s</td>
<td>10 s ± 1 s</td>
</tr>
<tr>
<td>Distance from component body</td>
<td>≥ 2 mm</td>
<td>≥ 5 mm</td>
</tr>
</tbody>
</table>

SOLDERING RECOMMENDATIONS

Soldering of the component should be achieved using a Sn96.5/Ag3.0/Cu0.5, a Sn60/40 type or a silver-bearing type solder.

As ceramic capacitors are very sensitive to rapid changes in temperature (thermal shock), the solder heat resistance specification (see above Soldering Specifications table) should not be exceeded.

Subjecting the capacitor to excessive heat may result in thermal shocks that can crack the ceramic body and melt the internal solder junction.

CLEANING

The components should be cleaned with vapor degreasers immediately following the soldering operation.

SOLVENT RESISTANCE

The coating and marking of the capacitors are resistant to the following test method: IEC 60068-2-45 (Method XA). The epoxy material is approved according to UL 94 V-0.

MOUNTING

We do not recommend modifying the lead terminals, e.g. bending or cropping as this action could break the coating or crack the ceramic insert. However, if the lead must be modified in such a way, we recommend supporting the lead with a clamping fixture next to the coating.

CAPACITANCE “AGING” OF CERAMIC CAPACITORS

Following the final heat treatment, all class 2 ceramic capacitors reduce their capacitance value. According to logarithmic law, this is due to their special crystalline construction. This change is called “aging”. If the capacitors are heat treated (for example when soldering), the capacitance increases again to a higher value deaging, and the aging process begins again.

\[
K = \frac{100 \times (C_{11} - C_{12})}{C_{11} \times \log_{10}(t_2/t_1)} \\
C_{12} = C_{11} \times [1 - K/100 \times \log_{10}(t_2/t_1)]
\]

REFERENCE MEASUREMENT

Due to aging, it is necessary to quote an age for reference measurements which can be related to the capacitance with fixed tolerance. According to EN 130700, this time period is 1000 h.

If the shelf-life of the capacitor is known, the capacitance for t = 1000 h can be calculated with the aging constant.

In order to avoid the influence of aging, it is important to deage the capacitors before stress-testing. The following procedure is adopted (see also EN 130700):

- Deaging at 125 °C
- One hour storage for 24 h at normal climate temperature
- Initial measurement
- Stress
- Deaging at 125 °C, 1 h
- Storage for 24 h at normal climate temperature
- Final measurement
**CAUTION**

1. OPERATING VOLTAGE AND FREQUENCY CHARACTERISTIC

When sinusoidal or ripple voltage applied to DC ceramic disc capacitors, be sure to maintain the peak-to-peak value or the peak value of the sum of both AC and DC within the rated voltage.

When start or stop applying the voltage, resonance may generate irregular voltage.

When rectangular or pulse wave voltage is applied to DC ceramic disc capacitors, the self-heating generated by the capacitor is higher than the sinusoidal application with the same frequency. The allowable voltage rating for the rectangular or pulse wave corresponds approximately with the allowable voltage of a sinusoidal wave with the double fundamental frequency.

The allowable voltage varies, depending on the voltage and the waveform.

Diagrams of the limiting values are available for each capacitor series on request.

<table>
<thead>
<tr>
<th>VOLTAGE</th>
<th>DC</th>
<th>DC AND AC</th>
<th>AC</th>
</tr>
</thead>
<tbody>
<tr>
<td>WAVEFORM FIGURE</td>
<td><img src="image1" alt="DC Waveform" /></td>
<td><img src="image2" alt="DC and AC Waveform" /></td>
<td><img src="image3" alt="AC Waveform" /></td>
</tr>
</tbody>
</table>

2. OPERATING TEMPERATURE AND SELF-GENERATED HEAT

The surface temperature of the capacitors must not exceed the upper limit of its rated operating temperature.

During operation in a high-frequency circuit or a pulse signal circuit, the capacitor itself generates heat due to dielectric losses. Applied voltage should be the load such as self-generated heat is within 20 °C on the condition of environmental temperature 25 °C.

Note, that excessive heat may lead to deterioration of the capacitor's characteristics.