

## Multilayer Ceramic Dipped Axial Capacitors 50 V<sub>DC</sub>, 100 V<sub>DC</sub>, 200 V<sub>DC</sub> and 500 V<sub>DC</sub>

### STORAGE

The capacitors must not be stored in a corrosive atmosphere where sulfide or chloride gas, acid, alkali, or salt are present. Moisture exposure should also be avoided.

The solderability of the leads is not affected by storage of up to 24 months. Temperature + 10 °C to + 35 °C, relative humidity up to 60 %.

With reference to class 2 ceramic dielectric capacitors, see the last page of this general information.

### SOLDERING

SOLDERING SPECIFICATIONS		
Soldering test for capacitors with wire leads: (According to IEC 60068-2-20, solder bath method)		
	SOLDERABILITY	RESISTANCE TO SOLDERING HEAT
Soldering temperature	235 °C ± 5 °C	260 °C ± 5 °C
Soldering duration	2 s ± 0.5 s	10 s ± 1 s
Distance from component body	≥ 2 mm	≥ 5 mm

### SOLDERING RECOMMENDATIONS

Soldering of the component should be achieved using a Sn96.5/Ag3.0/Cu0.5, a Sn60/40 type or a silver-bearing type solder.

As ceramic capacitors are very sensitive to rapid changes in temperature (thermal shock), the solder heat resistance specification (see above table) should not be exceeded.

Subjecting the capacitor to excessive heat may result in thermal shocks that can crack the ceramic body and melt the internal solder junction.

### CLEANING

The components should be cleaned with vapor degreasers immediately following the soldering operation.

### SOLVENT RESISTANCE AND FLAME ABILITY

The coating and marking of the capacitors are resistant to the following test method: IEC 60068-2-45 (Method XA). The epoxy material is approved according to UL 94 V-0.

### MOUNTING

We do not recommend modifying the lead terminals, e.g. bending or cropping as this action could break the coating or crack the ceramic insert. However, if the lead must be modified in such a way, we recommend supporting the lead with a clamping fixture next to the coating.



### CAPACITANCE “AGING” OF CERAMIC CAPACITORS

Following the final heat treatment, all class 2 ceramic capacitors reduce their capacitance value. According to logarithmic law, this is due to their special crystalline construction. This change is called “aging”. If the capacitors are heat treated (for example when soldering), the capacitance increases again to a higher value deaging, and the aging process begins again.

#### Note

- The level of this deaging is dependent on the temperature and the duration of the heat; an almost complete deaging is achieved at 150 °C in one hour. These conditions also form the basis for reference measurements when testing. The capacitance change per time decade (aging constant) differs for the various types of ceramic, but typical values can be taken from the equations below.

$$k = \frac{100 \times (C_{11} - C_{12})}{C_{11} \times \log_{10}(t_2/t_1)}$$

$t_1, t_2$  = measuring time point (h)

$C_{11}, C_{12}$  = capacitance values for the times  $t_1, t_2$

$$C_{12} = C_{11} \times (1 - k/100 \times \log_{10}(t_2/t_1))$$

$k$  = aging constant (%)

### REFERENCE MEASUREMENT

Due to aging, it is necessary to quote an age for reference measurements which can be related to the capacitance with fixed tolerance. According to EN 130700, this time period is 1000 h.

If the shelf-life of the capacitor is known, the capacitance for  $t = 1000$  h can be calculated with the aging constant.

In order to avoid the influence of aging, it is important to deage the capacitors before stress-testing. The following procedure is adopted (see also EN 130700):

- Deaging at 125 °C, 1 h
- Storage for 24 h at normal climate temperature
- Initial measurement
- Stress
- Deaging at 125 °C, 1 h
- Storage for 24 h at normal climate temperature
- Final measurement

## CAUTION

### 1. OPERATING VOLTAGE AND FREQUENCY CHARACTERISTIC

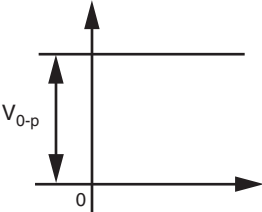
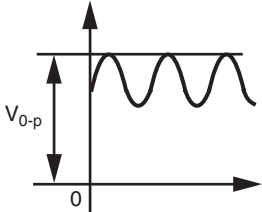
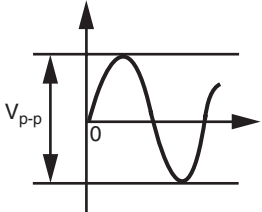
When sinusoidal or ripple voltage applied to DC Ceramic Disc Capacitors, be sure to maintain the peak-to-peak value or the peak value of the sum of both AC + DC within the rated voltage.

When start or stop applying the voltage, resonance may generate irregular voltage.

When rectangular or Pulse Wave Voltage is applied to DC Ceramic Disc Capacitors, the self-heating generated by the capacitor is higher than the sinusoidal application with the same frequency. The allowable voltage rating for the rectangular or pulse wave corresponds approximately with the allowable voltage of a sinusoidal wave with the double fundamental frequency.

The allowable voltage varies, depending on the voltage and the waveform.

Diagrams of the limiting values are available for each capacitor series on request.

VOLTAGE	DC	DC + AC	AC
Waveform Figure			

### 2. OPERATING TEMPERATURE AND SELF-GENERATED HEAT

The surface temperature of the capacitors must not exceed the upper limit of its Rated Operating Temperature.

During operation in a high-frequency circuit or a pulse signal circuit, the capacitor itself generates heat due to dielectric losses. Applied voltage should be the load such as self-generated heat is within 20 °C on the condition of environmental temperature 25 °C.

Note, that excessive heat may lead to deterioration of the capacitor's characteristics.