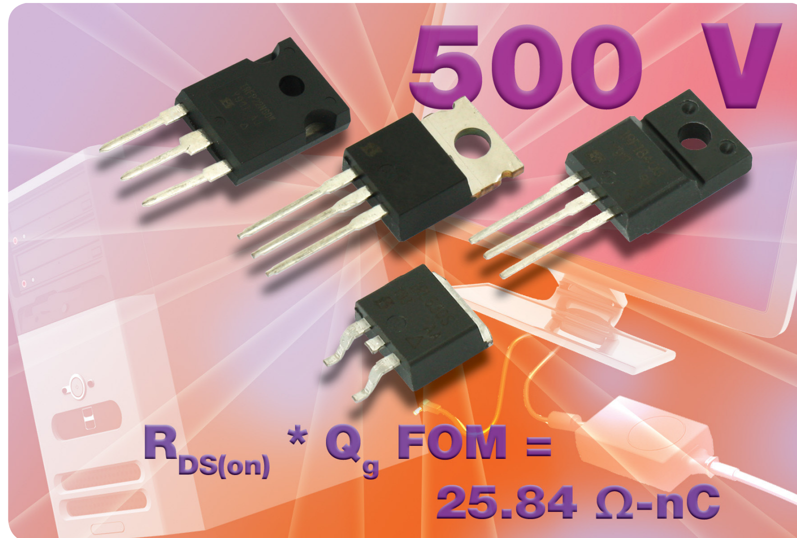
POWER MOSFETS

SiHP16N50C-E3, SiHF16N50C-E3, SiHB16N50C-E3, SiHG16N50C-E3

High-Voltage MOSFETs - 500 V N-Channel with Gen. 6.4 Cell Technology



KEY BENEFITS

- Vishay's Gen. 6.4 cell technology minimizes on-resistance and withstand high energy pulses
- 16 A, 500 V, $R_{DS(on)}$ max. = 380 mΩ at V_{GS} = 10 V
- Low gate charge: Q_g max. = 68 nC
- 100 % avalanche tested

APPLICATIONS

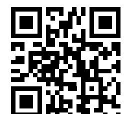
- PFC boost circuit topology
- PWM half bridge topology
- LLC topology

RESOURCES

- Datasheets: SiHP16N50C-E3, SiHF16N50C-E3, SiHB16N50C-E3 - http://www.vishay.com/doc?91401
  SiHG16N50C-E3 - http://www.vishay.com/doc?91418
- More featured products: http://www.vishay.com/ref/featuredmosfets
- For technical questions, contact: hvm@vishay.com
- Material categorization: For definitions of compliance please see http://www.vishay.com/doc?99912

RoHS
COMPLIANT

One of the World's Largest Manufacturers of
Discrete Semiconductors and Passive Components



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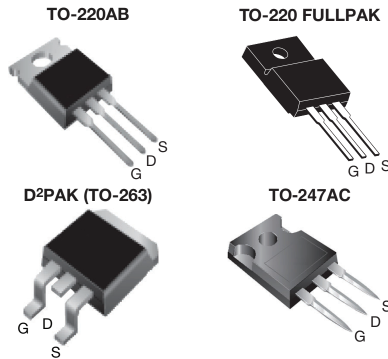

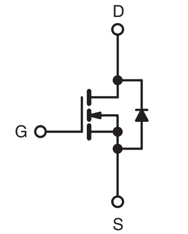

N-Channel MOSFET

ORDERING INFORMATION				
Package	TO-220AB	TO-247AC	D^2PAK (TO-263)	TO-220 FULLPAK
Lead (Pb)-free	SiHP16N50C-E3	SiHG16N50C-E3	SiHB16N50C-E3 SiHB16N50CTR-E3 SiHB16N50CTL-E3	SiHF16N50C-E3

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TO220AB, D^2PAK(TO-263)	TO-247AC	TO-220 FULL PAK	UNIT
Maximum Junction-to-Ambient	R_{thJA}	62	40	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	0.5	0.5	3.3	
Junction-to-Ambient (PCB mount)[a]	R_{thJA}	40			

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.6	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V		-	-	50	μA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 8 A	-	0.31	0.38	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = 50 V, I_D = 3 A		-	3	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz		-	1900	-	pF
Output Capacitance	C_{oss}			-	230	-	
Reverse Transfer Capacitance	C_{rss}			-	24	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 16 A, V_{DS} = 400 V	-	45	68	nC
Gate-Source Charge	Q_{gs}			-	18	-	
Gate-Drain Charge	Q_{gd}			-	22	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 16 A, R_g = 9.1 Ω, V_{GS} = 10 V		-	27	-	ns
Rise Time	t_r			-	156	-	
Turn-Off Delay Time	$t_{d(off)}$			-	29	-	
Fall Time	t_f			-	31	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain		-	1.6	-	Ω

Revision: 13-Jun-11

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