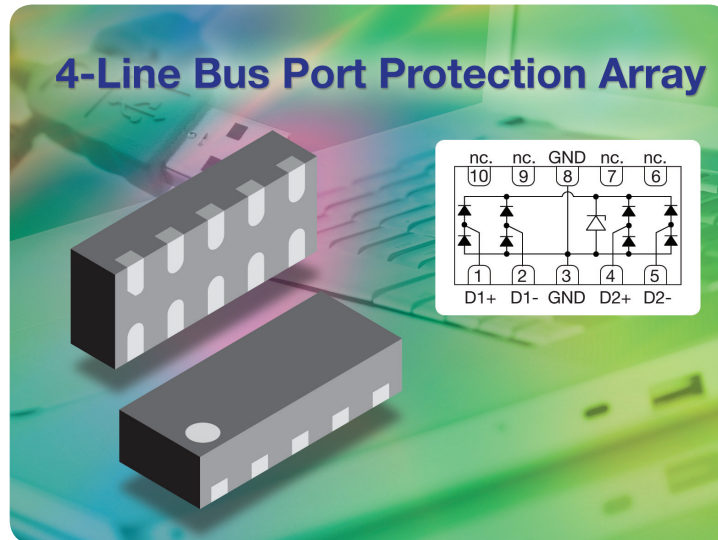


ESD-Protection Bus Port Array



KEY BENEFITS

- Low load capacitance of 0.6 pF
- Low maximum leakage current of $< 0.1 \mu\text{A}$ (at the working voltage of 5.5 V)
- Ultra-compact LLP2510 package
- Features a “flow through” design
 - Supports surge resistance requirements for high-speed data lines

APPLICATIONS

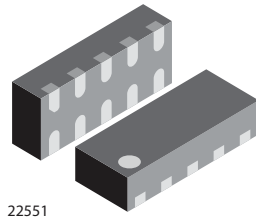
- ESD protection for high-speed data lines in applications such as:
 - USB 3.0
 - HDMI
 - DisplayPort
 - eSATA
 - 1394/Firewire in mobile electronics

RESOURCES

- Datasheet: <http://www.vishay.com/doc?82414>
- For technical questions, please contact: ESDprotection@vishay.com
- Material categorization: For definitions of compliance please see <http://www.vishay.com/doc?99912>



4-Line BUS-Port ESD Protection - Flow Through Design



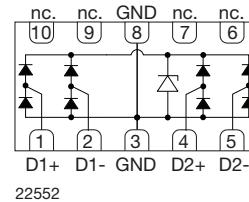
22551

FEATURES

- Compact LLP2510-10L package
- Low package height < 0.6 mm
- 4-line ESD-protection
- Low leakage current $I_R < 0.1 \mu\text{A}$
- Low load capacitance $C_D = 0.6 \text{ pF}$
- Ideal for high speed data line like
 - HDMI, DisplayPort, eSATA
 - USB, 1394/firewire
- ESD-protection acc. IEC 61000-4-2
 - $\pm 15 \text{ kV}$ contact discharge
 - $\pm 15 \text{ kV}$ air discharge
- Soldering can be checked by standard vision inspection. No X-ray necessary
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC

Note

** Please see document "Vishay Material Category Policy":
www.vishay.com/doc?99902



MARKING (example only)



Dot = pin 1 marking
 YY = type code (see table below)
 XX = date code

ORDERING INFORMATION

DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VBUS54ED-FBL	VBUS54ED-FBL-G4-08	3000	15 000

PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VBUS54ED-FBL	LLP2510-10L	L5	3.9 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

ABSOLUTE MAXIMUM RATINGS

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5; $t_p = 8/20 \mu\text{s}$; single shot	I_{PPM}	2	A
Peak pulse power	Acc. IEC 61000-4-5; $t_p = 8/20 \mu\text{s}$; single shot	P_{PP}	25	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 15	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 15	kV
Operating temperature	Junction temperature	T_J	- 40 to + 125	°C
Storage temperature		T_{STG}	- 55 to + 150	°C

ELECTRICAL CHARACTERISTICS VBUS54ED-FBL (pin 1, 2, 4 or 5 to pin 3)

PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	4	lines
Reverse stand-off voltage		V_{RWM}	-	-	5.5	V
Reverse voltage	at $I_R = 0.1 \mu\text{A}$	V_R	5.5	6.3	7.5	V
Reverse current	at $V_R = V_{RWM} = 5.5 \text{ V}$	I_R	-	0.02	0.1	μA
Reverse breakdown voltage	at $I_R = 1 \text{ mA}$	V_{BR}	6.9	7.5	8.7	V
Clamping voltage	at $I_{PP} = 1 \text{ A}$; acc. IEC 61000-4-5	V_C	-	9.1	11	V
	at $I_{PP} = 2 \text{ A}$; acc. IEC 61000-4-5	V_C	-	10.3	12.5	V
Forward clamping voltage	at $I_F = 1 \text{ A}$; acc. IEC 61000-4-5	V_F	-	1.9	2.2	V
	at $I_F = 2 \text{ A}$; acc. IEC 61000-4-5	V_F	-	2.5	3.1	V
Line capacitance	at $V_R = 0 \text{ V}$; $f = 1 \text{ MHz}$	C_D	-	0.7	0.8	pF
	at $V_R = 3.3 \text{ V}$; $f = 1 \text{ MHz}$		-	0.6	0.8	

Note

- Ratings at 25 °C, ambient temperature unless otherwise specified

FLOW THROUGH DESIGN

Modern digital transmission lines can be clocked up to 480 Mbit/s (USB2.0) or 1.65 Gbit/s (HDMI).

At such high data rates the transmission lines like cables or the line traces on the PCBs have to be very homogeneous regarding their surge impedance. This requires well defined trace dimensions as trace width and distance which have to be calculated depending on the requested surge impedance (e.g. 50 Ω) and the PCB material and layer dimensions. Any device connected to the data lines - like ESD-protection devices - have to be connected with minimal changes in these trace dimensions and distances.

With the package in the so called "Flow Through Design" this is possible. The lines are running straight along the PCB while the VBUS54ED-FBL is placed on top without any vias or loops.