



# 2015 Super 12 Products

SiC620R

60 A VRPower® Integrated Power Stage



A **WORLD OF**  
**SOLUTIONS**

## SiC620R

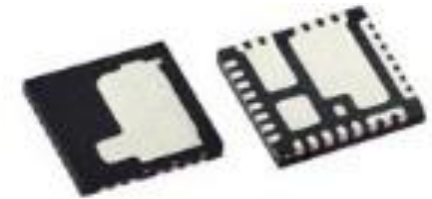
Next Generation DrMOS, 20 % Lower Power Losses and 50 °C Cooler Operation Than Previous Generation

- Features:
  - 20 % lower power losses
  - Dual-cooled package enables 70 A power stage
  - 95 % peak efficiency, over 3 % better efficiency than previous generation
  - Optimized package design for up to 1.5 MHz operation
  - 50 °C lower operating temperatures for improved reliability
  - Zero current detect control for light load efficiency improvement
  - Thermally enhanced PowerPAK® MLP55-31L double-cooling package
  - Low PWM propagation delay (< 20 ns)
  - Thermal and undervoltage monitoring



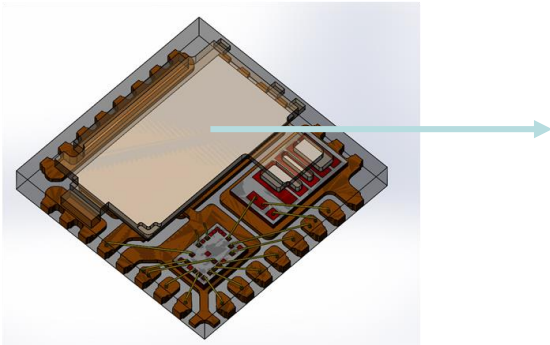
## SiC620R

- Applications / Market Segments:
  - Servers and workstations
  - Telecom ASIC power
  - Game consoles
  - POL modules
  - Graphic cards
  - Bitcoin mining hardware
  
- Datasheet document number: 63589
- Product page: [www.vishay.com/ppg?63589](http://www.vishay.com/ppg?63589)
- Product sheet: [www.vishay.com/doc?49597](http://www.vishay.com/doc?49597)



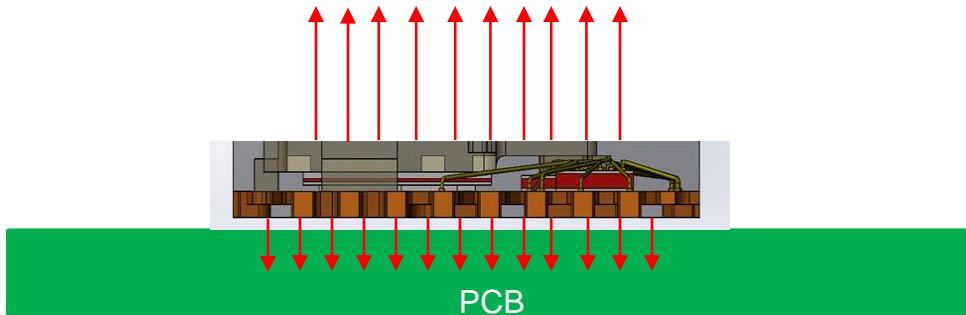
## SiC620R

- Package construction:



Clip forms the switch node (SW), which is exposed on top to allow for dual-sided cooling

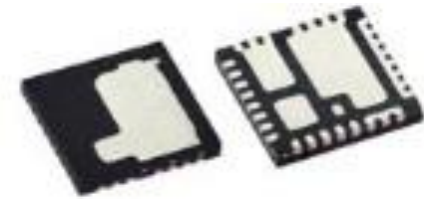
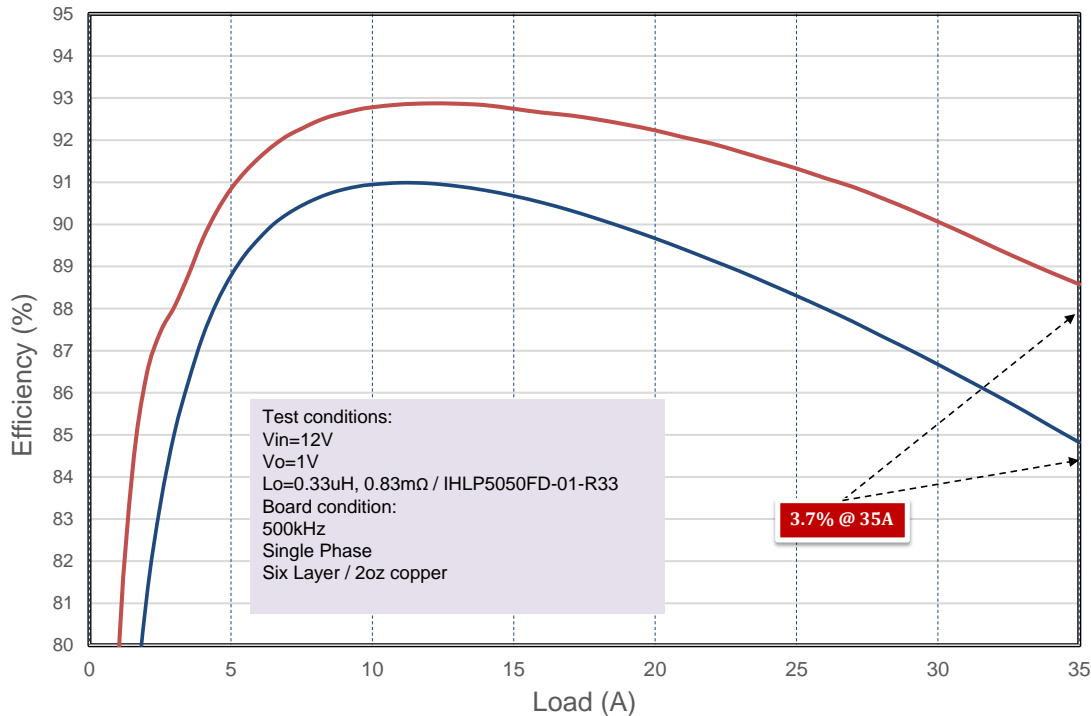
Heat is removed from the top via the SW clip



Large PGND pad allows for heat removal through PCB

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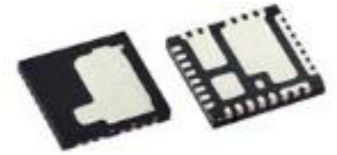
- Competition:



- The graph shows the efficiency improvement over competitor's part in standard 6 mm x 6 mm DrMOS footprint at 12  $V_{in}$  to 1  $V_{out}$

## SiC620R

- Why use SiC620R?
  - Vishay's flagship VRPower® module, the SiC620R offers an integrated MOSFET and driver power stage with unsurpassed performance
  - The device is capable of 70 A and achieves more than 95 % efficiency in a typical multi-phase buck converter design
  - The device has several package enhancements that enable it to offer superior MOSFET dynamic performance
  - Combined with Vishay's state-of-the-art Gen IV MOSFET technology, these enhancements enable 3 % better efficiency and over 50 °C lower operating temperatures compared to previous-generation DrMOS devices, while shrinking the footprint by 33 %





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