High-Voltage Silicon MOSFETs, GaN, and SiC: All have a place

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Questions have arisen about how silicon will compete against wide bandgap (WBG) materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN). There are many different technologies used in high voltage silicon devices today and though Si MOSFETs and WBG technologies will be the focus of this article, IGBTs are reviewed as they are a competing technology within the high voltage market. The MOSFET, IGBT, and JFET (WBG) technologies breakdown as follows:

MOSFETs (Si)

- Conventional planar technology
- Superjunction technology

IGBTs (Si)

- Non-punch through (NPT) technology
- Punch through (PT) technology
- Field stop (FS) technology

MOSFETs (SiC)

- Conventional planar structure

JFETS (GaN)

- Normally “ON”
- Normally ”OFF”

There is a lot of interest in the WBG technologies such as SiC and GaN and the purpose here is to show that both Si and WBG materials (SiC and GaN) all have their place within the power industry and neither will completely displace each other.

The power MOSFET market in 2010 was $5.85B with an expected growth of 10.3% to $9.56B in 2015. Silicon conventional planar devices range from voltages under 100V to greater than 1000V, with superjunction ranging from 500V thru 900V and IGBTs from 600V and up to and including 1200V (for this discussion).

This paper defines that equal to and greater than 400V are classified as high voltage devices. The 400V and greater voltage MOSFETs are the fastest growing segment out of all MOSFETs. In 2011 this segment represented $2.05B growing at a CAGR of 12.4% over the next five years[1]. Out of this $2.05B, superjunction devices account for around $500M growing close to $1B by 2016[2].

Today, much of the demand in superjunction devices is in the 500V to 650V range with a smaller portion in 800V and 900V. That being said just over $1.5B is represented by conventional planar devices with the largest market segments being computer, office equipment, and consumer.

Though IGBTs represent just under a billion dollars (less than 600V to greater than 900V) of the high-voltage device market they have been the fastest growing since the beginning of 2010. A couple reasons for this growth were the demand for solar inverters and a redesign in white goods where China has enacted a five year plan to reduce energy consumption.

If one compares the two Si MOSFET technologies (superjunction and conventional planar) and Si IGBTs based on a similar die size this is what you would see:

Superjunction (performance driven)

- Lower conduction losses: ability to reduce on-resistance four times over a similar voltage conventional planar.
- Lower switching losses: based on the same on-resistance, the ability to reduce switching characteristics such as Q_{GD} and reverse transfer capacitance (C_{rss})

Conventional Planar (value driven)

- Based on the same on-resistance of a superjunction device:
  - Greater robustness: due to the larger die size, therefore better for unclamped inductive switching (UIS).
  - Better thermals: larger die to dissipate the heat across
- Higher value: lower manufacturing costs, one step Epi growth
- Easier to design in with lower switching speeds

IGBTs (value and performance driven)

- Lowest cost – for the same current rating, IGBTs have higher current density than both Si MOSFET technologies
- Superior for low frequency high power applications

These advantages listed above will ultimately allow silicon technologies to continue to compete into the future as SiC and GaN come online.

Conventional silicon planar technology vs superjunction
Conventional Silicon Planar Technology vs. Silicon Superjunction Technology
In order to understand the differences between the two Si MOSFET technologies we need to start with the basics. Conventional planar MOSFET technology typically have a high Rds per unit area, and thus require large die sizes to achieve a low $R_{DS(on)}$. However, a larger die size has lower current density, and better heat sinking capabilities. As a result, the conventional planar MOSFETs are

inherently more rugged compared to superjunction technology for a given on resistance.

The superjunction structure (also called “charge balanced”) has a linear relationship between on-resistance and breakdown voltage. So, as the Epi gets thicker the on-resistance increases proportionally to the increase in breakdown voltage. In reality for the same breakdown voltage and die size the on resistance of a superjunction will be less than a conventional planar device.

The way charge balancing works is as the n region becomes more heavily doped it’s on-resistance decreases. This charge that is present in the n region is offset by the charge in the p-type pillars allowing a linear relationship between on-resistance and breakdown voltage. Superjunction today is operating with a specific on-resistance of around a quarter of conventional planar technology depending on voltage rating. With this reduction in resistance has obvious conduction loss benefits; the reduction in chip area for this technology lowered capacitance (C_{rss}) and dynamic losses as well.

To pictorially show how blocking voltage and on resistance is defined between conventional planar technology and superjunction, please refer to figure 1 below.

- **Superjunction MOSFETs use thinner Epi for a given blocking voltage**
  - Conventional planar MOSFET = A1 + A3
  - Superjunction MOSFET = A1 + A2
- **Blocking voltage is defines as:**
  - Conventional Planar MOSFET
    - The Epi thickness and the doping (ND+) (slope of the line)
    - If additional blocking voltage is required not only does the Epi have to be made thicker, but also the Epi doping (ND+) line has to change
  - Superjunction MOSFET
    - Only the thickness of the Epi defines the blocking voltage
      - The doping of the N column (ND+) is balanced out by the doping of the P column (NA-) so that is why the top of A1 + A2 is flat (no slope), NetQ = 0.
- **On Resistance is also different between the two technologies (based on a given voltage and die size)** – remember in a HVM most of the on resistance is in the drift region
  - Conventional planar MOSFET
    - Thicker drift region Epi higher on resistance
  - Superjunction
    - Thinner drift region Epi lower on resistance

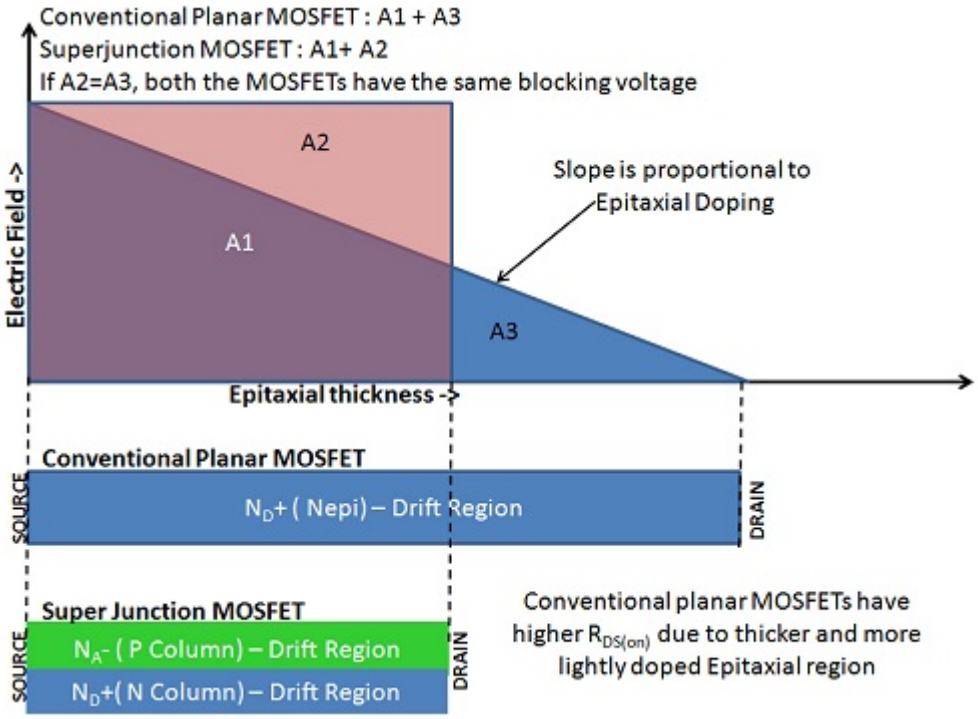

Figure 1: Conventional planar MOSFET versus superjunction MOSFET

Note: Along with an increase in on resistance, capacitance increases as well. Though, thicker Epi should reduce the capacitance it actually increases due to the larger die size (higher Rds-A) in the conventional planar technology. As the Epi gets thicker the on-resistance increases so the die has to be made larger thereby increasing the capacitance.

Applications such as electric bikes and welding in the industrial market space require highly robust devices so this is where conventional planar vertical technology has an advantage. With conventional planar MOSFETs being manufactured with a single layer of epi grown all at once, the manufacturing cost is lower than superjunction making them a value play.

Newer design concepts like dual trenches and charge balancing make it possible to break what was considered silicon barrier two or three years ago. Today as stated above we are able to offer leading edge specific on resistance value for our 600V and 650V MOSFETs using “charge balancing technology.”

However the ever increasing demands of better efficiency call for highly focused tradeoff between raw $R_{DS(on)}$ and other switching parameters. We have to move away from simple figures of merit that paired $R_{DS(on)}$ with C_{iss}, Q_g, Q_{gd}, Q_{gs}, Q_{sw} and more recently Q_{oss}. For example PFCs, Critical Conduction Mode (CrCM)flybacks, LLC half bridges, solar inverters and welding equipment all use 600V MOSFETs but there is no one Figure of Merit (FOM) or one device technology that optimizes performance for all these applications.

Today’s designers are not asking for generic figures of merit but for solutions that produce the lowest loss in their system. This requires close communication with designers and deep understanding of their topologies and loss mechanisms and using that knowledge to define products optimized specifically to each application.

Silicon IGBTs
Silicon IGBTs
Silicon IGBTs are more suitable for high power density applications. These devices have a very

lightly doped drift region, suitable for blocking high voltages. However, during forward conduction, these devices undergo conductivity modulation from minority carrier injection which are approximately two orders of magnitude higher than background doping.

This makes the IGBTs achieve low forward voltage drop during conduction, and high current density of operation. However, this also results in a current tail when the device switches from conduction to blocking, because the minority carriers in the drift region need to be swept out before the device can block voltage. This results in a trade off in operating frequency.

Depending on the power level of the application this process reduces the maximum operating frequency to in many cases no higher than 125 kHz (Switch Mode Power Supplies (SMPS)) and in some cases below 30 kHz for motor drives. This gives IGBTs a disadvantage against voltage controlled devices such as MOSFETs that have the ability operate at high frequencies (up to and over 1MHz).

Another disadvantage of conductivity modulated device such as IGBT is the 0.7V voltage knee during forward conduction. This makes them unsuitable for applications that required the high voltage switch to operation with a forward voltage drop lower than 0.7V

So, ultimately all the above silicon technologies have a place in systems depending on their operation, application and what the customer constitutes as being most important. Figure 2 summarizes Vishay's MOSFET technology comparisons:

MOSFETs	Standard (conventional planar)	D Series (conventional planar)	S Series (superjunction)	E Series (superjunction)
Standard (conventional planar)		Better Thermals Same Package StandardTechnology offers FREDFETs Standard MOSFETs More Robust		
D Series (conventional planar)	Lower $R_{DS(ON)}$ Lower Q_G Lower Cost Better FOM		Better Thermals Same Package More Robust	
S Series (superjunction)	Lower $R_{DS(ON)}$ Lower Q_G Lower Cost Better FOM	Lower $R_{DS(ON)}$ Lower Q_G Lower Cost Better FOM		Higher $R_{DS(ON)}$ Better Thermals Higher Qg
E Series (superjunction)	Lower $R_{DS(ON)}$ Lower Q_G Lower Cost Better FOM	Lower $R_{DS(ON)}$ Lower Q_G Lower Cost Better FOM	Lower $R_{DS(ON)}$ Lower Q_G Lower Cost Better FOM	

Figure 2: Vishay Siliconix: comparing silicon technologies

Silicon vs. SiC and GaN (Wide bandgap material)
Now that we have discussed how the silicon technologies differ, the main question is, "How does silicon technology compare with SiC and GaN?"There are three areas here:

- Material: Wide Bandgap[1] material versus Si (Table 1)
- Differences in Manufacturing
- Device performance and price

For switching power applications SiC devices are mainly in the form of Schottky barrier diodes (600V to 1200V up to 40A, with a couple 1700V), some normally OFF-JFETs, and a couple 1200V MOSFETs where as for GaN there are some companies offering up to 200V normally OFFAlGaN-GaN HFETs .

The table below compares material properties for Silicon (Si), Silicon Carbide (4H-SiC[2]) and Gallium Nitride (GaN). These material properties have a major influence on the fundamental performance characteristics of the devices.

Material	Bandgap (E_G) (eV)	Electron Mobility (cm^2/V-sec)	Intrinsic Carrier Concentration (n_i) @ 300°C (cm^{-3})	Critical Field 10^5 (E_C) (V/cm)	Saturated Electron Drift Velocity (cm/s) (V_D)
Silicon (Si)	1.1	1450	$>1.0 \times 10^{15}$	0.25	1.0×10^7
Silicon Carbide (4H-SiC)	3.26	900	1.0×10^4	2.2	2.0×10^7
Gallium Nitride (GaN)	3.2	2000	2.0×10^2	3.0	2.5×10^7

Table 1: Semiconductor material overview

From Table 1 the performance tradeoffs are as follows:

Si, SiC, and GaN Materials

High Temperature of Operation

The intrinsic carrier concentration for Si, SiC, and GaN are shown in Table 1 as a function of temperature this being at 300ºC. The control of the free-carrier concentration is vital for the performance of all semiconductor devices. The intrinsic carrier concentration (n_i) is exponentially dependant on temperature. At temperatures above 300°C, SiC and GaN have much lower intrinsic carrier concentrations than Si. This implies that devices designed for higher temperatures should be fabricated from WBG semiconductors. In order to use this advantage, high temperature packaging must also be available.

Electric Field Characteristics

The high critical field of both GaN and SiC compared to Si is a property which allows these devices to operate at higher voltages and lower leakage currents (able to handle an electric field 10 times greater than Si). This allows the use of a thinner (0.1 times that of silicon devices), more highly doped (ten times the doping concentration) drift layer, resulting in a lower on-resistance ($R_{DS(on)}$) – typically a minimum of 10 times lower than for Si devices of the same blocking voltage.

Manufacturing

Substantial improvements have been made in material quality for both SiC and GaN over the last several years. The devices of interest for switching applications require an epitaxial layer of either SiC or GaN to be grown or deposited on a substrate composed of either the same (homoepitaxy) or a different (heteroepitaxy) material.

Homoepitaxial SiC devices are fabricated in a way that is analogous to silicon in that a SiC epi layer is formed on a SiC substrate (Figure 3). The result is a good crystallographic match between the epi

and substrate and an electrically and thermally conductive path from the top to the bottom of the wafer. This has implications on the device structures which can be fabricated as well as cost. There are a number of companies producing SiC substrate and epi wafers.

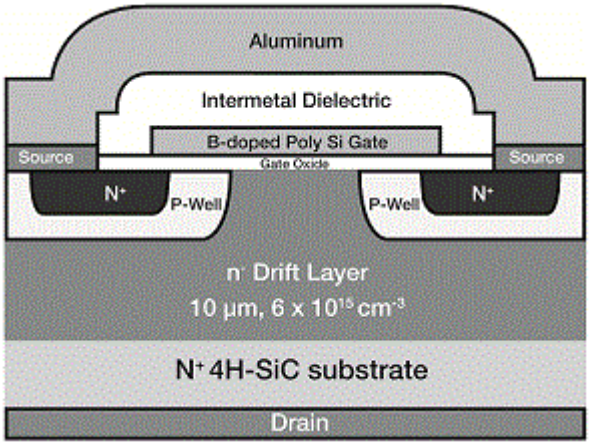

Figure 3: Simplified cross-section of a 1200V 4H-SiC DMOSFET[3]

GaN substrates are available today and primarily used to manufacture blue laser diodes on 2” wafers which is the current state of the art for this material[4]. A homoepitaxial GaN wafer offers advantages over heteroepitaxy approaches for GaN-based devices; however, production processes for epi ready GaN substrates of high quality (low defect) are still in the early stages and much less mature than SiC.

Just as with SiC, there are many inherent challenges that must be addressed when it comes to the growth of bulk single crystal GaN to achieve an epi-ready substrate. Therefore, the common approach today is the heteroepitaxy approach. There are several variations being implemented but for the purposes of switching power applications, the primary choice today for a heteroepitaxial GaN wafer is GaN epi on a “non-native” SiC substrate. Another combination being used is GaN epi on Si. In both cases there are crystal lattice differences which need to be accounted for, which add additional materials and processing costs.

Performance and Price

The common approach to accommodating the crystallographic differences is through the use of a buffer layer (Figure 4). Aluminum Nitride (AlN) is one material being used which provides a good material match but is electrically insulating which impacts the types of device structures which can be fabricated.

Creation of the buffer layer also adds cost and process complexity. Also these buffer layers combined with the use of non-native substrates result in defects and inherent stress which need to be overcome in order to not adversely affect device performance, yields and reliability

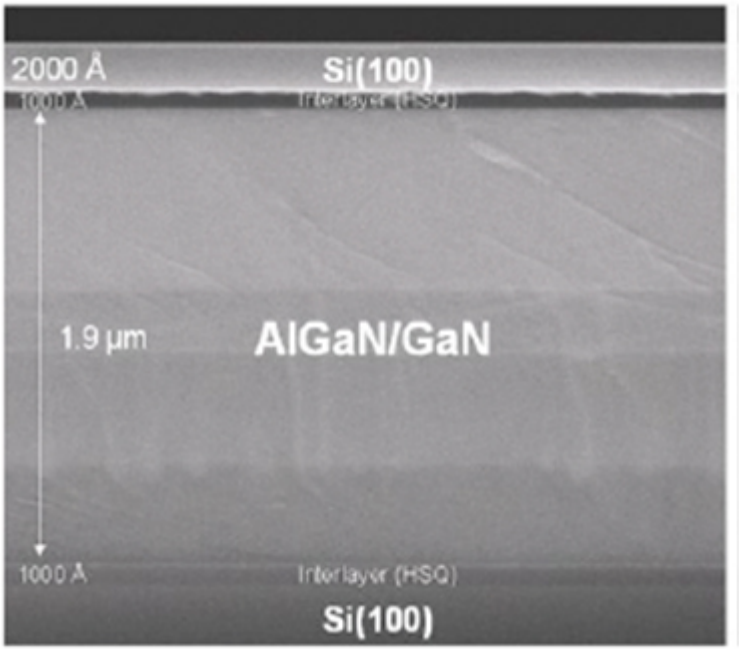

Figure 4: Scanning electron micrograph of a Si-GaN-Si virtual wafer[1]

State-of-the-art wafer diameters are 4” going to 6” for homoepitaxial SiC and 3” for heteroepitaxy GaN on SiC or Si wafers (moving to 6”). In terms of cost, GaN on SiC wafers cost about 20% more than their SiC on SiC counterparts. From a device manufacturing point of view, defectivity for GaN on SiC or GaN on Si wafers is higher than their SiC on SiC and Si on Si counterparts. This is an important consideration because unlike simple diodes or LEDs, power devices are very sensitive to defects.

In addition, GaN on Si has a 2 to 1 difference (Table 2) in the coefficient of thermal expansion (CTE) at the epi interface, which can be an issue during power cycling (another reason why additional layers of material are required to make the device mechanically sound). GaN on silicon wafers promise to be substantially lower cost than either the SiC on SiC or GaN on SiC wafers leading to a great deal of current interest in this combination. A primary question is…. Can the device structures, yields, electrical and thermal performance, reliability and overall benefit to the system cost overthrow the current silicon devices used today?

Substrate	GaN	Si <111>	Sapphire (Crystal of Al2O3)	SiC 6H	Ge<111>
Lattice Constant (A)	3.19	3.84	2.75	3.08	4.0
Coefficient of Thermal Expansion (CTE)	5.6	2.6	7.5	4.2	5.9

Table 2: Lattice constant and CTE of semiconductor starting material

Performance and Price

Fast Body Diode

In order to speed up the body diode in Si based MOSFETs, two additional steps are used. Being that the SiC SBD has low reverse recovery charge (Q_{rr})and low reverse recovery time (T_{rr}), the SiC

MOSFETs body diode exhibits the same type of performance so additional processing is not required and therefore can be used in soft switching applications.GaN lateral JFETs on the other hand do not have body diodes so in order to create a fast recovery body diode device an external Schottky barrier diode (SiC or GaN) or Fast Recovery Epitaxial Diode (FRED) would have to be used.

Lateral Device versus Vertical Device

Being that one can only manufacture a lateral device in GaN as the voltage and current level increases so will the size of the device more so than a SiC vertical device. There are companies developing and have products on the market that use GaN on Si. Making the product on the Si reduces the overall cost of the product, and allows them to move quicker to larger diameter wafers.

Being that only lateral devices can be developed, these are in essence normally ON-JFETs that have been designed for normally OFF operation. Normally OFF JFETs are not driven the same as Si/SiC MOSFETs and that can be seen as a drawback. Right now up to 200V normally OFF J-FET devices are available in GaN. Table three below shows an overview of what devices can be developed in the different WBG material.

Device	Vertical Topology	Lateral Topology
SBD	SiC-4H,Si	GaN
JFET / SIT	SiC-4H, Si	NA
MESFET	NA	SiC-4H, GaN, Si
BJT	SiC-4H, Si	NA
MOSFET	SiC-4H, Si	NA

Table 3: Summary of which devices can be built with the different materials

Transconductance, Electron Mobility and Saturated Electron Drift Velocity

The SiC low transconductance due to low inversion mobility needs to be carefully considered in the design of the gate drive circuit. The gate driver has to be capable of a 22V (or higher) swing. For the CREE CMF10120D, the recommended on state VGS is +20V and the recommended off state VGS is between -2V to -5V. For higher power applications having a higher saturated electron drift velocity is advantageous where carrier velocity increases versus transferring the energy to the lattice of the structure.

Capacitances and Switching Speeds

As the specific on-resistance of Si, SiC, and GaN technologies decrease with time so does the capacitances. Having smaller capacitances and charges are nice as less power is needed to turn the devices on, but the turn off performance also increases. What is meant here is that the dv/dt becomes quicker where over shoot and electromagnetic interference (EMI) can become an issue.

Designers have had to slow down superjunction Si devices today in order to achieve the required performance over a range of voltages. SiC and GaN having smaller specific-on resistances means that specifically the die size and hence capacitance will be smaller for the same on-resistance. This is seen as a further challenge to using SiC and GaN in switching applications.

Price

One major disadvantage is cost. Now, overtime WBG device cost will reduce, but as superjunction technology continues to increase its performance by reducing its specific on-resistance, be manufactured on larger diameter wafers, it will always have a cost advantage. SiC products (manly Schottky Diodes) today are using 4" material and will require to be manufactured on 6" if the MOSFET is to be successful in commercial and automotive type applications. Though SiC and GaN is more expensive, it does come with some advantages over Si.

Figure 5 below shows the voltage levels at where switching technology and their respective applications fit.

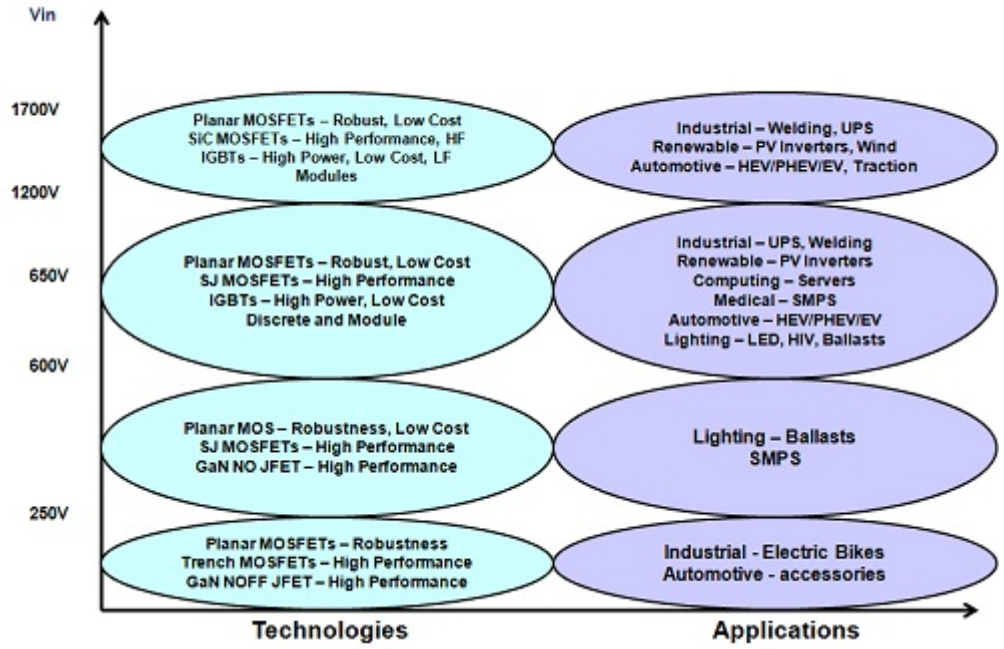

Figure 5: Device technologies and applications for the stated voltage ranges

Conclusion

The overall material and processing cost of both conventional planar and superjunction will always be lower than SiC and GaN. Conventional planar technology encompasses more than 50% of the current total available market (TAM) for high voltage MOSFETs (HVM) and offers a value added technology with robust operation. Superjunction is growing faster than conventional planar technology at a 23% CAGR over the next five years and is poised to hit $1.3B by 2015, well on its way towards being more competitive with the specific-on-resistance against IGBTs, which is at a minimum 2x that of the competitive technology. Even though conventional planar technology has hit its silicon limit, based on price, its complexity in manufacturing, performance and applications, we do not see SiC and GaN replacing Si technology, plus superjunction still has a ways to go. With this increase in performance specifically in on-resistance which is classified as conduction losses comes switching performance and ruggedness that will continue to be a challenge facing all technologies.

Author's Biography:

Philip Zuk currently serves as the Director of Market Development, High-Voltage MOSFET Group at Vishay Siliconix. He holds a BEE from the University of Manitoba and an MBA from the I.H. Asper School of Business.

Notes:

1. IMS Research

2. Yole Development

3. Wide bandgap pertains to the energy required for an electron to jump from the top of the valence band to the bottom of the conduction band within the semiconductor. Materials which require energies typically larger than one or two electron-volts (eV) are referred to as wide bandgap materials.

4. The “4H” in SiC-4H refers to the crystal structure of the SiC material

5. B. Hull et al., presented at ECSCRM 2008, Barcelona, Spain, Sept. 7-11, 2008

6. Orientation Control of Bulk GaN Substrates Grown via Hydride Vapor Phase Epitaxy, Kyma Technologies, Inc.

7. On-Wafer Integration of nitrides and Si Devices: Bringing the Power of Polarization to Si, 2009 IEEE