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Optimum Dead Time Selection in ZVS Topologies

Insufficient dead time during turn off can result in the loss of ZVS, poor efficiency, and in the worst case, failure of the device due to shoot-through. Minimum dead time required can be calculated from the published device parameters. Dead time optimization based on the following analysis can help to exploit the advances in device technology and achieve better performance even from legacy designs.

Medium and high voltage power MOSFETs are used in a variety of isolated converter topologies, such as half or full bridges and single ended boost or synchronous buck regulators. The bridges may be hard or soft switched; however, most of today's converters employ zero voltage switching (ZVS) to eliminate turn-on switching losses. The power train remains the same, only the sequence in which devices are turned on and off needs to be modified. Synchronous buck converters, typically used for front end pre-regulation in wide input DC-DC brick converters, also switch the low side MOSFET in ZVS mode. While the hard switched bridges and boost converters do not have critical dead time requirements, all soft switched ZVS bridges and synchronous buck converters must operate within such limits. In low voltage synchronous buck converters, the dead time during the transitions between low and high side MOSFETs is optimized by the controller or the driver. Shoot-through protection is also implemented, either by sensing the falling edge of the gate drive or the switch node voltage. There are more sophisticated techniques that attempt to optimally adjust the delay on a continuous basis.

However, such fine tuning is not practical with higher voltage drivers and the designers must fall back on fixed dead times during transitions. Since long dead times lead to longer body diode conduction and a consequent loss of efficiency, it is always desirable to provide an optimally minimized dead time without running into shoot-through conditions. This requires a detailed understanding of the transition process and calculation of different intervals based on MOSFET and circuit parameters. While optimum delays can be, and quite often are, determined empirically, analysis is necessary to account for variations and to choose the right device for the highest efficiency. For an illustration of this analysis, we will use a soft switched full bridge, which operates with a full duty ratio of 50% per arm. Such a topology is also known as a DC transformer, and is popular for generating unregulated intermediate bus converter (IBC) output from a 48 V DC input. The concepts and parametric tradeoffs discussed here can be extended to many other ZVS topologies as well.

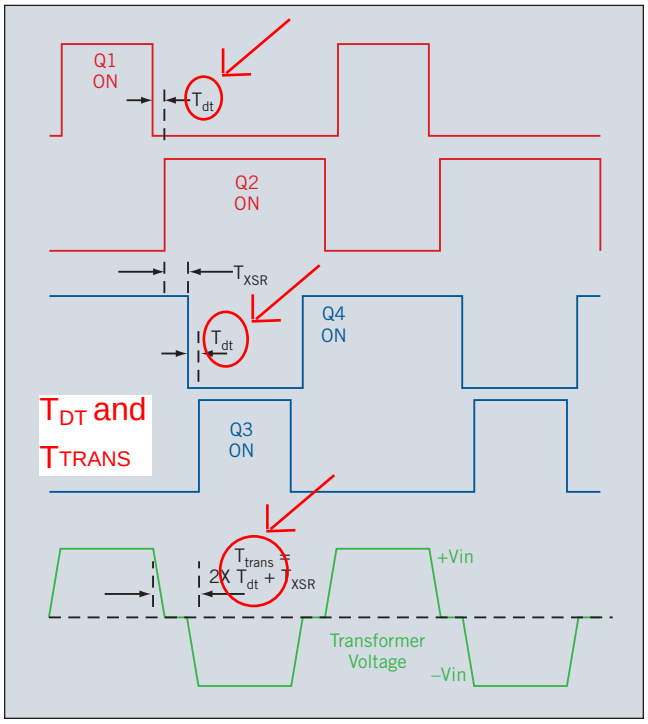


Fig. 1: Gate drive and transformer voltages in a full-duty ratio bridge.

THE TRANSITION PROCESS

To start with, there are different ways to sequence a soft-switched full bridge, and each has its own benefits and traps. One particular sequence, where each transition is initiated by turning off the high side MOSFET, is shown in *Fig. 1*. The flow of current through different devices during the transition is shown in

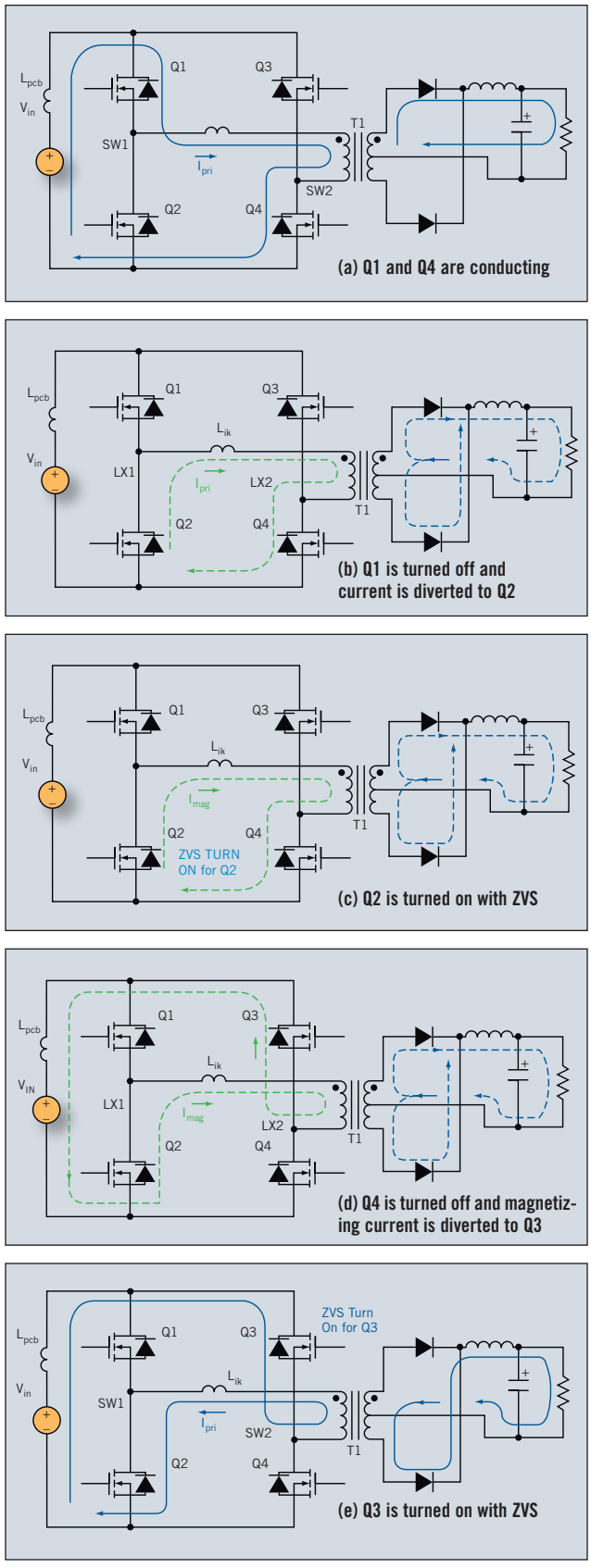


Fig. 2. Soft-switched full-bridge current through MOSFETs:

Figs. 2a through 2e. Initially Q1 and Q4 are conducting and power is delivered to load (*Fig. 2a*). The transition is initiated by turning off Q1 and its current is diverted to the body diode of Q2 (*Fig. 2b*). This interval lasts for T_{DT}.

When Q1 is completely off, Q2 is turned on with ZVS. This is followed by a short duration (T_{XSR}), during which transformer primary is shorted out and magnetizing current circulates between the low side MOSFETs (*Fig. 2c*). In phase shifted bridge converters, output regulation is achieved by varying T_{XSR}, but in DC transformers it is kept to a minimum. After the T_{XSR} delay, Q4 is turned off and the magnetizing current is diverted to Q3 (*Fig. 2d*). The transition is complete when Q3 is turned on with ZVS after another interval of T_{DT} (*Fig. 2e*).

The total transition time is given by the equation $T_{TRANS} = 2 \times T_{DT} + T_{XSR}$.

The interval T_{XSR} is not critical to the primary transition; it can be zero in theory. However, a minimum value is demanded by the secondary synchronous rectifier. If output rectifiers are replaced by synchronous MOSFETs, their drive signals must toggle during the T_{XSR} dead band. This is true whether SSRs are self-driven or control driven; the secondary drive pulses are matched to the primary in both cases. The only difference is that in a self-driven scheme, T_{XSR} needs to be higher since the transformer secondary rise and fall times are much slower. Another factor to consider is that High to Low and Low to High transitions are not symmetric with IC based gate drivers, which may add a delay during the level shifting of the input signals. This is different from, and in addition to, the normal propagation delay through the drive stages. The level shift delay reduces available dead time even further during H to L transitions, but is actually beneficial during L to H transitions and increases available dead time. Most drivers try to match the total delays within a few ns, but the difference, denoted as T_{LSH}, needs to be taken into account.

It is clear that ZVS turn-on is achieved only if, ~~it is~~ within the available dead time T_{DT}, ~~and:~~

- Gate capacitance of the outgoing MOSFET is discharged to below $V_{TH,}$
- Output capacitor of the incoming MOSFET is fully discharged close to zero.

Fig. 3 shows the simplified gate turn-off circuit used in the analysis. Since all capacitances are functions of V_{DS}, the equivalent charge specifications will be used in the calculations. There are three distinct stages for the gate discharge, as shown in *Fig. 4*.

T0 – T1: C_{ISS} is discharged from the gate supply voltage V_{GSS} to plateau V_{GP}, assuming constant turn-off current. During this interval the I_{GOFF} current is limited by the drive capability rather than gate resistors.

T1 – T2: Conventional plateau time where V_{DS} rises to V_{IN} and beyond due to ringing. The gate current is now

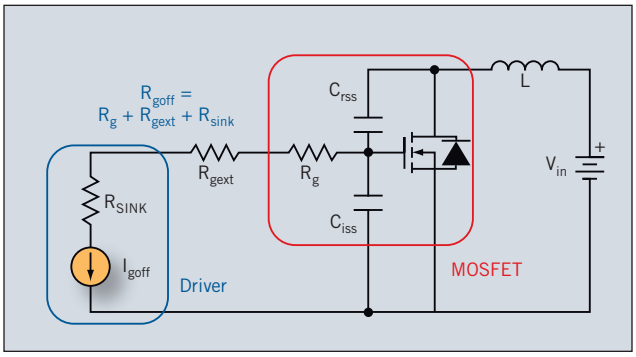
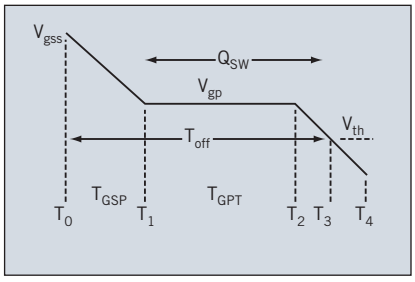


Fig. 3: Simplified gate drive circuit.

Fig. 4. Gate turn-off voltage and time intervals.



limited by the total resistance in the gate loop.

T2 – T3: Current fall time in the outgoing MOSFET.

The three intervals can be calculated using the equations:

$$T_{GSP} = C_{ISS0} \times \left(\frac{\cancel{V_{GSS}}}{I_{GOFF}} \right) \quad V_{GSS} - V_{GP} \qquad (1)$$

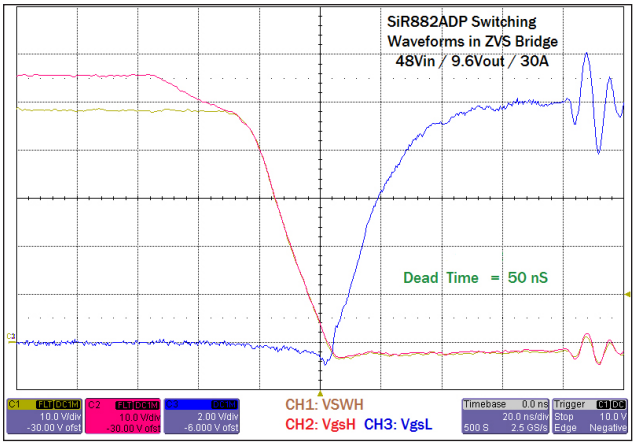
$$T_{GPT} = R_{IGOFF} \times \frac{Q_{SW}}{V_{GP}} \qquad (2)$$

C_{ISS0}

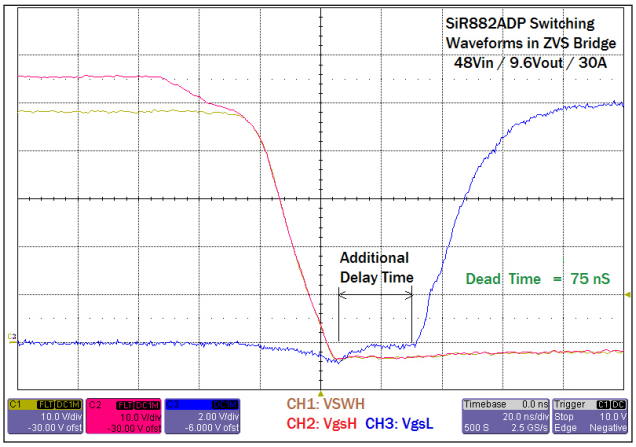
$$R_{GOFF} = R_G + R_{EXT} + R_{SINK} \qquad (3)$$

The value C_{iss0} used for T_{GSP} is not from the datasheet tables, but at V_{DS} = 0V, when the MOSFET is fully on. For ultra-low $R_{DS(ON)}$ MOSFETs with extremely high cell densities, trench gates, and charge balancing structures, C_{iss0} can be 4 ~ 5 times higher than the C_{ISS} specified at mid voltage. There is no power loss, but this interval can eat up a major part of the available dead time. The formula for T_{GPT} defines the sum of voltage rise time and current fall time during turn-off based on the drive conditions. This is an inadequate approximation, since the current fall time depends on a number of external parameters such as PCB trace inductance, source inductance of the package, and input voltage. These factors dominate di/dt of the primary loop current over gate drive. However, the focus here is on achieving zero voltage status for the incoming MOSFET, which may be determined using another approach. As the current in the high side MOSFET goes to zero, the same is taken up by its complement in the low side. This enables a simple estimate of the time required to discharge the output capacitance as one quarter of one resonant cycle of L_{PCB} and C_{OSS}.

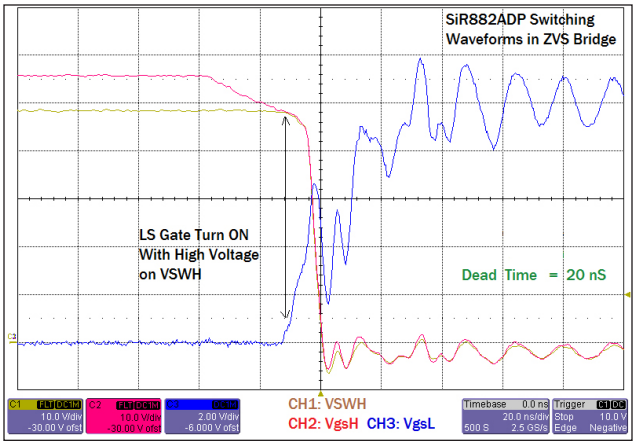
Fig. 5. Switching node waveforms:



(a) Dead time = 50 nS



(b) Dead time = 75 nS



(c) Dead time = 20 nS

$$T_{DSD} = \frac{\pi}{2} \times \sqrt{\frac{L_{PCB} \times Q_{OSS}}{V_{IN}}} \qquad (4)$$

It is assumed that the PCB trace inductance is much smaller than the leakage inductance L_{LK}, and during T_{DSD} the transformer loop current does not change. With this we are in a position to state the complete timing requirement

Blue curve is 75 ns
Green curve 50 ns

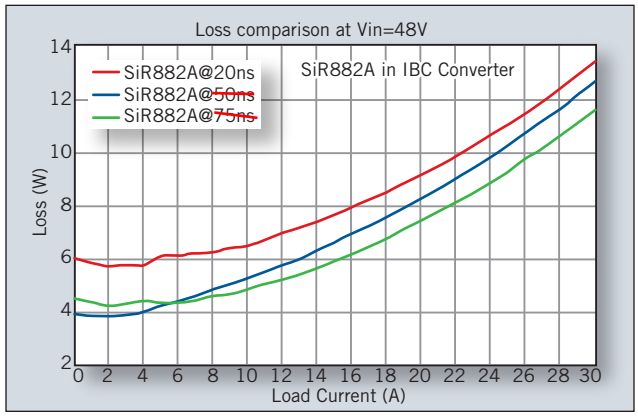


Fig. 6. Total loss as a function of dead time.

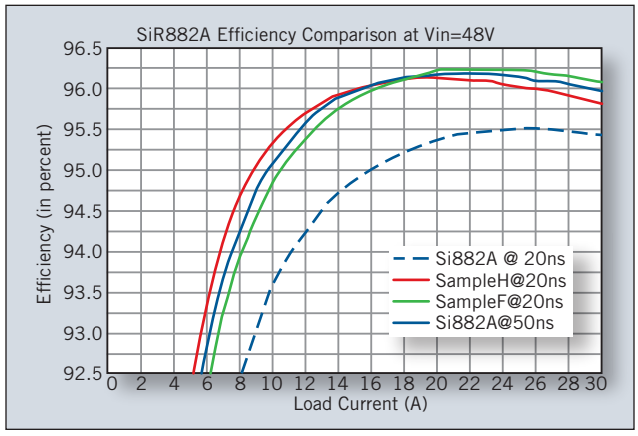


Fig. 7. System efficiency comparison.

TABLE 1: DEAD TIME CALCULATIONS FOR SIR882ADP

SIR882ADP			CIRCUIT PARAMETERS		
$R_{DS(ON)}$	7.40	mΩ	V_{IN}	48	V
C_{ISS}	1975	pF	V_{GSS}	10	V
C_{ISS0}	4500	pF	I_{GOFF}	2	A
Q_{SW}	9.8	nC	L_{PCB}	20.0	nH
Q_{OSS}	64.0	nC	R_{SINK}	2.0	Ω
V_{GP}	3.0	V	R_{GEXT}	2.0	Ω
R_G	1.0	Ω	R_{GOFF}	5.0	Ω
TGSP	15.75	nS	TLSH	10.00	nS
TGPT	16.20	nS	TDSD	8.11	nS

TABLE 2: COMPARISON OF COMPETITIVE DEVICES

MOSFET	UNITS	SAMPLE H	SAMPLE F	SIR882ADP
Typical $R_{DS(ON)}$	(mΩ)	12	6.3	7.2
Calculated Optimum Dead Time	(nS)	38.3	38.9	50.1

for the dead time T_{DT},

$T_{dt} \geq T_{LSH} + T_{GSP} + T_{GPT} + T_{DSD}$

This final result is somewhat conservative for devices with high V_{TH} values. The higher rise time needed before gate voltage can reach V_{TH} adds to the dead time.

TEST RESULTS ON IBC CONVERTER

The above analysis was verified with the SiR882ADP high performance MOSFET targeted for high frequency DC-DC converters. The relevant specifications of the device are shown in *Table 1*. The test platform was a 48V to 9.6V IBC converter operating at 200 kHz. The original design set the dead time at 20 ns. From the *Table 1* values, it is clear that this dead time is quite insufficient.

Figs. 5a to 5c show the switching node waveforms for three different dead times: 50 ns, 75 ns, and 20 ns. *Fig. 6* shows the power loss of the entire converter as a function of different dead times. Optimal switching with minimum loss occurs at a dead time of 50 ns, as calculated. At 20 ns, the low side MOSFET is turned on with the switch node voltage at $V_{IN,}$ resulting in shoot-through losses. While the waveforms at 75 ns look clean and offer an extra safety margin, the duration of diode conduction also increases. *Fig. 6* shows its impact: diode losses steadily adding up with increasing current.

DILIGENCE BEFORE DROP IN

are quite dependent on

It is quite common for designers to try out a promising new part in an existing design. It is also equally common to do this by just dropping in the new part in place of the existing one and run an automated efficiency test program. Unfortunately, the results are almost never reliable. The power losses depend quite on how well the dead time is matched to the device characteristics. Modern trench devices with dense cell structures offer the benefit of very low $R_{DS(ON)}$, but also come with larger C_{ISS0}, Q_{GD}, and Q_{OSS} values. While these devices offer better figure of merit (FOM) and improved efficiencies, designers need to fine tune their circuits to realize their full potential.

This can be further illustrated by comparing three different devices in the same circuit. *Table 2* shows the calculated optimum dead times for the SiR882ADP against two other samples. *Fig. 7* shows the measured efficiency of all devices at different dead times. Sample H was the original device used in the IBC converter with a dead time of 20 nS. It has the highest gate threshold voltage V_{TH} and is more immune to shoot-through even with reduced dead times. Both the lower $R_{DS(ON)}$ devices show worse efficiency, simply because they were dropped in a circuit that was not designed for them.