FPGA Power Supply Considerations

An examination of the power requirements for FPGAs, offers guidance on how and where to place them on the PCB, and takes the reader step-by-step through a design example involving an FPGA that needs to operate in a system supplied by a 12 V bus, which is the main output from a mains-supplied SMPS.

Owain Bryant, Product Applications Engineer, Vishay Siliconix | *Power Electronics* *Aug. 1, 2013*

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What is in this article?:

The key part of the FPGA design is to determine the voltage requirements needed and the current requirements of each voltage rail. The major FPGA vendors offer comprehensive

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calculators that take into account the frequency that the part operates at, the number of gates used, as well as the toggle rate of the gates to determine these requirements. For instance, Altera offers the PowerPlay Early Power Estimator and Xilinx offers the XPower Analyzer.

TABLE 1. 80 PLUS CERTIFICATION REQUIREMENTS

	Part number	Logic (Ks)	Core voltage (V)	Core tol. (mV)	Auxiliary Voltages (V)	IO voltages (V)	IO tol. (%)
Altera							
Stratix V	5SEBA	1087	0.85	30	2.5 (VCCA_PLL) 1.5 (VCCD_PLL)	1.2 - 3	5 5
Cyclone IV GX	EP4CGX150	150	1.2	40	2.5 (VCCA, VCCA_GXB, VCCH_GXB) 1.2 (VCCD_PLL, VCC_CLKIN)	1.2 - 3	5 5
Arria V	5AGXB7	503	1.1	30	2.5 (VCC_AUX, VCCA_FPLL, VCCPD)	1.2 - 3.3	5
Xilinx							
Virtex 6	XC6VLX760	760	1	50	2.5 (VCC_AUX)	1.2 - 2.5	5
Virtex 6	XC7V2000T	2000	1	30	1 (MGTAVCC, VCCBRAM) 1.2 (MGTAVTT) 1.8 (MGTVCCAUX, VCCAUX, VCCAUX_IO) 4.5 (VCCBRAM)	1.2 - 1.8	5
Spartan 6	XC6SLS150T	147	1.2	60	1.2 (MGTAVCC, MGTAVCCPLL, MGTAVTTRX, MGTAVTTTX) 2.5 (VCCAUX) 3.3 -	1.2 - 3.3	5
Artix 7	XC7A350T	360	1	30	1 (MGTAVCC, VCCBRAM, VCCINT) 1.2 (MGTAVTT) 1.8 (MGTVCCAUX, VCCAUX, VCCAUX_IO)	1.2 - 3.3	5

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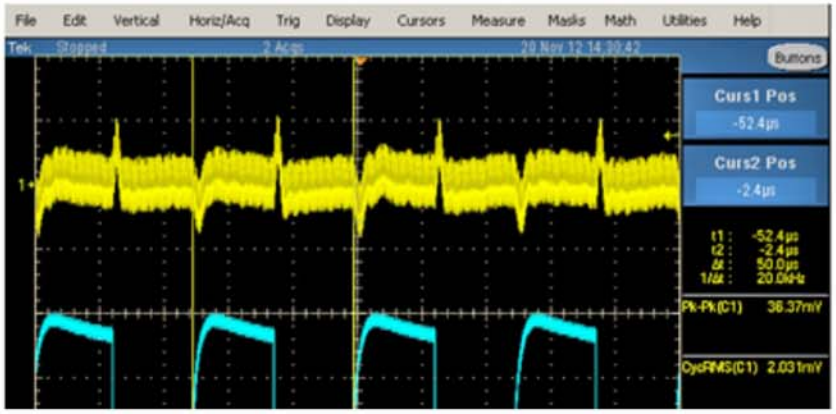
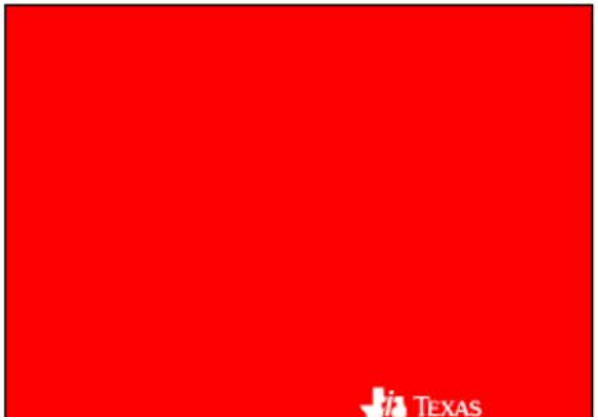
Table 1 lists some of the typical voltage rails required by Altera and Xilinx devices, broken down into the core voltage, the I/O voltages, the transceiver, and the auxiliary voltages.

FPGAs with lower core voltage needs require high currents, high accuracy, and minimum ripple. In order to achieve this, decoupling capacitors should be placed as close as possible to the FPGA, with minimal ESR and ESL in the decoupling path.

Another desirable practice is to place the POL regulators as near to the part as possible without affecting routing in and out of the FPGA. Higher operating frequencies and the integration of control, drivers and MOSFETs, enable a compact layout. The small solution footprint allows for close placement of the regulators to the FPGA, thus improving regulator transient response. ***Fig. 1*** provides an example of a 3 A regulator in Vishay's microBUCK® product offering.

The step response, with minimal input and output capacitance of 22 µF (0805), can be observed in ***Fig. 1*** as 37 mV Pk-Pk (the load has some capacitance also).





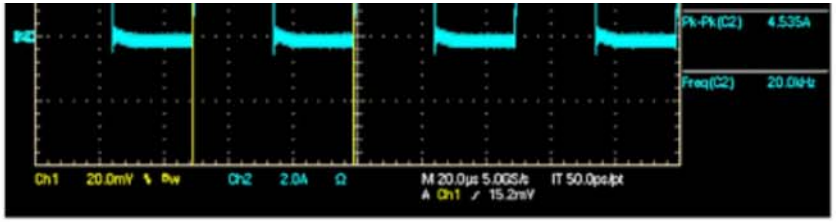


Fig.1. Step Response of SiP12107. VIN = 5 V, VOUT = 1.2, Fsw = 2 MHz; Load step at 20 kHz = 0 to 3 A; L = 330 nH, CIN = 22 µF, COUT = 22 µF; Yellow = VOUT, Blue = current.

The regulator uses a current mode constant-on-time (CM-COT) topology, and does not need external ripple injection for stability. This allows for reduced component count and an excellent transient response.

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