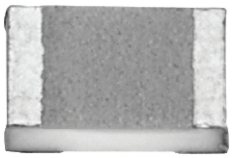
ESCC (·e) 4001/023 Qualified High Precision (5 ppm, 0.01 %), Thin Film Chip Resistors



LINKS TO ADDITIONAL RESOURCES

3D Models

Vishay Sfernice Thin Film division holds ESCC QML qualification (ESCC technology flow qualification).

These High-Rel. components are ideal for low noise and precision applications, superior stability, low temperature coefficient of resistance, and low voltage coefficient, Vishay Sfernice's precision thin film wraparound resistors exceed requirements of MIL-PRF-55342G characteristics Y (± 10 ppm/°C).

FEATURES

HALOGEN FREE

- Load life stability at ± 70 °C for 2000 h: 0.15 % under Pn
- Low temperature coefficient down to ± 5 ppm/°C
- Very low noise (< -35 dB) and voltage coefficient (< 0.01 ppm/V)
- Resistance range: 10 Ω to 3 MΩ (depending on size)
- Laser trimmed tolerances to ± 0.01 %
- TCR in lot tracking ≤ 5 ppm/°C
- Termination: Thin film technology
- SnPb terminations over nickel barrier
- ESCC 4001 (generic specifications)
- ESCC 4001/023 (detailed specifications)
- ESCC qualified
- SMD wraparound chip resistor
- Operating temperature range: -65 °C to +155 °C
- From 0402 to 2010
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

STANDARD ELECTRICAL SPECIFICATIONS

MODEL	SIZE	ESCC VARIANT NUMBER	RESISTANCE RANGE Ω	RATED POWER AT + 70 °C (Pn) W (1)	LIMITING ELEMENT VOLTAGE (UL) V (1)	INSULATION VOLTAGE (U_i) V	TOLERANCE ± %	TEMPERATURE COEFFICIENT ± ppm/°C
PHR 0402 ·e	0402	13 and 14	10 to 150K	0.05	30	50	0.01, 0.02, 0.05, 0.1	5, 10, 25
PHR 0603 ·e	0603	01 and 05	10 to 500K	0.1	35	100	0.01, 0.02, 0.05, 0.1	5, 10, 25
PHR 0805 ·e	0805	02 and 06	10 to 750K	0.125	75	200	0.01, 0.02, 0.05, 0.1	5, 10, 25
PHR 1206 ·e	1206	03 and 07	10 to 3.5M	0.25	100	300	0.01, 0.02, 0.05, 0.1	5, 10, 25
PHR 2010 ·e	2010	04 and 08	10 to 6M	0.50	150	300	0.01, 0.02, 0.05, 0.1	5, 10, 25

Note

(1) Limiting voltages and power rating are already derated (for maximum ratings admissible, refer to P chip: www.vishay.com/cod?53017)

CLIMATIC SPECIFICATIONS

Operating temperature range	-65 °C; +155 °C
Soldering temperature (T_{sol})	260 °C, immersion 10 s

MECHANICAL SPECIFICATIONS

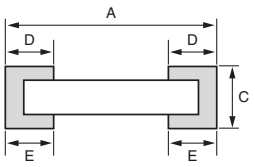
Substrate material	Alumina
Technology	Thin film
Film	**Nickel chromium** with mineral passivation
Protection	Epoxy and silicone
Terminations	**B type:** SnPb over nickel barrier for solder reflow (1) **G type:** gold over nickel barrier

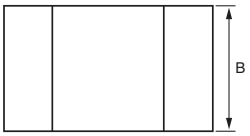
Note

(1) For B terminations use recommended reflow profile #1 as per Application Note "Guidelines for Vishay Sfernice Resistive and Inductive Components" (document number: 52029)

For technical questions, contact: sferthinfilm@vishay.com

DIMENSIONS in millimeters





VARIANT NUMBER	STYLE	DIMENSIONS									
		A		B		C		D		E	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
01, 05	0603	1.39	2.16	0.62	1.01	0.25	1.02	0.17	0.51	0.25	0.51
02, 06	0805	1.78	2.55	1.14	1.53	0.25	1.02	0.17	0.51	0.25	0.51
03, 07	1206	2.87	3.64	1.47	1.86	0.25	1.02	0.17	0.51	0.25	0.51
04, 08	2010	4.95	5.72	2.41	2.8	0.25	1.02	0.35	0.85	0.35	0.85
13, 14	0402	0.87	1.64	0.47	0.86	0.25	1.02	0.09	0.38	0.12	0.38

TRACEABILITY DEFINITIONS

The two major traceability elements are defined as:

- The primary process lot number named Front End lot (FE lot). One “FE lot” is composed of several wafers issued from the same thin film deposition sequence.
- The date code named Batch Number (BN). The “BN” is defined after completion of the end of production testing sequence.

The lot homogeneity is given by the “FE lot” and not by the “BN”.

According to the applied rules validated by the ESCC through the product qualification, the following situations are agreed:

- Parts coming from different “FE lost” might have the same “BN”.
- A maximum of two different “BN” might be applied to the same “FE lot” to enable the use of overruns from a previous PO.
- Unless requested / approved by the customer the “BN” will be 2 years old maximum.

SPECIFIC TRACEABILITY REQUIREMENTS

The following specific requirements have to be treated as:

- A customer who requires “Lot Homogeneity” has to mention it on the PO as “SINGLE PRODUCTION LOT”.
- A customer who requires “Lot Homogeneity” in addition to a “Single Batch Number” has to mention it on the PO as “SINGLE PRODUCTION LOT AND OPTION R0101”.

END OF PRODUCTION TESTING

Mandatory testing performed at the end of the production process:

- 100 % overload: Voltage $\sqrt{(6.25 \text{ Pn x Rn})}$ or 2 UL whichever is less - duration 2 s
- 100 % burn in: 168 h at Pn at 70 °C

OPTIONS

LOT VALIDATION TESTING

For procurement of qualified components, lot validation testing is not required and shall only be performed if specifically stipulated in the purchase order.

For procurement of unqualified components, lot validation testing shall be performed as stipulated in the purchase order. The need for lot validation testing shall be determined by the orderer.

When lot validation testing is required, it shall consist of the performance of one or more of the tests or subgroup test sequences of chart F4 indicated in the ESA Generic Specification ESCC 4001. The testing to be performed and the sample size shall be as stipulated in the purchase order. When procurement of more than one component type is involved from a family, range or series, the selection of representative samples shall also be stipulated in the purchase order.

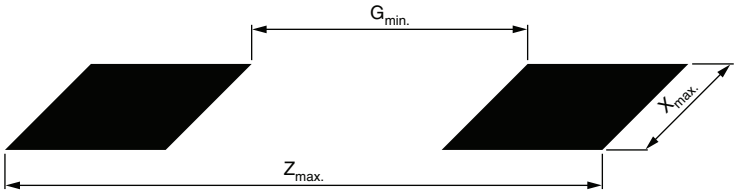
Lot validation testing will be composed of one LVT charges and LVT samples:

- Lot validation test charges has to be ordered separately on purchase order.
- Lot validation samples have to be ordered separately on purchase orderer.

FINAL INSPECTION

If requested by the orderer a final inspection can be performed on site.
Final inspection has to be stipulated separately on purchase order.

LAND PATTERN in millimeters



CHIP SIZE	$Z_{max.}$	$G_{min.}$	$X_{max.}$
0402	1.55	0.15	0.73
0603	2.37	0.35	0.98
0805	2.76	0.74	1.40
1206	3.91	1.85	1.73
2010	5.93	3.71	2.67

Note

- Suggested land pattern: According to IPC-7351A

QUALIFIED OHMIC RANGE (1)

MODEL	ESCC VARIANT	OHMIC RANGE (Ω)	TOLERANCE (%)
PHR	01 to 08 and 13 to 14	10 to < 50	0.1
		50 to < 100	0.05 and 0.1
		100 to < 250	0.02, 0.05 and 0.1
		≥ 250	0.01, 0.02, 0.05 and 0.1

QUALIFIED OHMIC RANGE (1)

MODEL	ESCC VARIANT	OHMIC RANGE (Ω)	TEMPERATURE COEFFICIENT (ppm/°C)	ESCC CODE
PHR	01 to 08 and 13 to 14	10 to < 20	E: 25 (-55 °C; +155 °C)	2
		20 to < 50	E : 25 (-55 °C ; +155 °C) Y : 10 (-55 °C ; +155 °C) Z : 5 (+22 °C ; +70 °C)	2 1 0
		≥ 50	E : 25 (-55 °C ; +155 °C) Y : 10 (-55 °C ; +155 °C) Z : 5 (+22 °C ; +70 °C) C : 5 (-55 °C ; +155 °C)	2 1 0 9

QUALIFIED OHMIC RANGE: MAX. VALUE (1)

PHR 0402	PHR 0603	PHR 0805	PHR 1206	PHR 2010
100 kΩ (67 kΩ for TCR C)	200 kΩ (160 kΩ for TCR C)	250 kΩ	1 MΩ	3 MΩ

Note

(1) For values, TCR, tolerance outside of qualified range: Please consult

POPULAR OPTIONS

OPTION 0041

Production according to ESCC 4001/023 for: Cases, ohmic values, tolerance or TCR outside of qualified range. Please consult Vishay Sfernice for feasibility.

PACKAGING

Two types of packaging are available: Waffle-pack and tape and reel.

SIZE	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH
	WAFFLE PACK 2" × 2"	TAPE AND REEL (2)		
		MIN.	MAX.	
0402	100	50	5000	8 mm
0603				
0805			4000	
1206	140			
2010	60		2000	12 mm

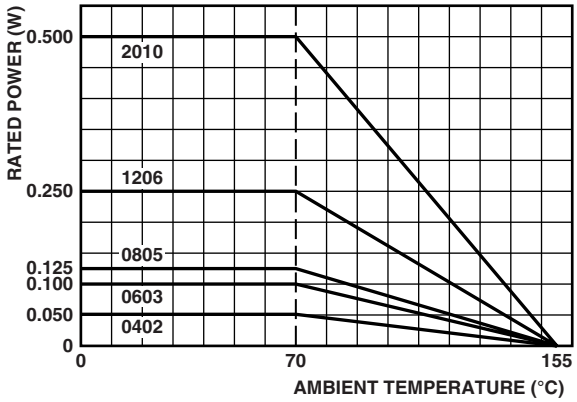
Note

(1) MoQ: 50 pieces

EXTENDED FEATURES

You may consult Vishay Sfernice for chip sizes, ohmic values and tolerances outside of the qualified range.

POWER DERATING CURVE



PERFORMANCE				
TEST	CONDITIONS	REQUIREMENTS		TYPICAL
		ESA/SCC 4001/023	MIL-PRF-55342G	
Short time overload	$U = \sqrt{(6.25 \text{ Pn x Rn})}$ $U_{max.} < 2$ UL - 2 s	± 0.05 % + (0.05 Ω x 100/Rn)	0.10 %	± 0.01 %
Rapid temperature change	-55 °C / +155 °C 5 cycles CEI 66-2-14 Test Na	± 0.05 % + (0.05 Ω x 100/Rn)	0.1 % (for 100 cycles)	± 0.01 % ± 0.015 % (for 500 cycles)
Soldering (thermal shock)	260 °C / 10 s CEI 68-2-20 A Test T6 (met. 1A)	± 0.05 % + (0.05 Ω x 100/Rn)	-	± 0.005 %
Terminal strength: adhesion bend strength of end plated facing	CEI 115-1 Clause 4.32 CEI 115-1 Clause 4.33	± 0.05 % + (0.05 Ω x 100/Rn)	-	± 0.01 %
Climatic sequence	CEI 67-2-1 / CEI 68-2-2 CEI 67-2-13 / CEI 68-2-30	± 0.10 % + (0.05 Ω x 100/Rn)	-	± 0.02 % Insulation resistance > 1 GΩ
Load life	2000 h Pn at +70 °C 90' / 30' cycle	± 0.15 % + (0.05 Ω x 100/Rn)	0.5 %	± 0.02 % Insulation resistance > 1 GΩ
High temperature exposure	2000 h Pn at +155 °C CEI 68-2-20A Test B	± 0.15 % + (0.05 Ω x 100/Rn)	± 0.10 % (duration 1000 h)	± 0.05 % Insulation resistance > 1 GΩ

ESCC/PHR CODIFICATION CORRESPONDENCE TABLES			
VARIANT	MODEL	CASE SIZE	TERMINATION
13	PHR	0402	B (tin/lead)
01		0603	
02		0805	
03		1206	
04		2010	
14		0402	G (gold)
05		0603	
06		0805	
07		1206	
08		2010	

ESCC/PHR CODIFICATION CORRESPONDENCE TABLES		
TEMPERATURE COEFFICIENT	ESCC CODE	PHR CODE
5 ppm/°C (+22 °C; +70 °C)	0	Z
10 ppm/°C (-55 °C; +155 °C)	1	Y
25 ppm/°C (-55 °C; +155 °C)	2	E
5 ppm/°C (-55 °C; +155 °C)	9	C

ESCC/PHR CODIFICATION CORRESPONDENCE TABLES		
TOLERANCE	ESCC CODE	PHR CODE
0.1 %	B	B
0.05 %	W	W
0.02 %	P	P
0.01 %	L	L

GLOBAL PART NUMBER INFORMATION

LIMITED TO 18 DIGITS: If more digits are necessary a codification of some digits might be necessary

P	H	R	0	6	0	3	Y	1	0	0	3	B	B	T		1	4

TYPE	TCR	OHMIC VALUE	TOLERANCE	TERMINATION	PACKAGING	OPTION
PHR0402 **PHR0603** **PHR0805** **PHR1206** **PHR2010**	**Y** = ± 10 ppm/°C **E** = ± 25 ppm/°C **Z** = 5 ppm/°C (+22 °C; +70 °C) **C** = 5 ppm/°C (-55 °C; +155 °C)	The first three digits are significant figures and the last digit specifies the number of zero to follow. R designates decimal point. Example: **10R0** = 10 Ω **3901** = 3900 Ω **1004** = 1 MΩ	**L** = ± 0.01 % **P** = ± 0.02 % **W** = ± 0.05 % **B** = ± 0.10 %	**B**: SnPb over nickel barrier **G**: gold	For more information see Codification of Packaging table	Leave blank if no option

Note

- **Terminations B:** Variants 01 / 02 / 03 / 04 and 13
  Terminations G: Variants 05 / 06 / 07 / 08 and 14

GLOBAL PART NUMBER INFORMATION

ESCC Code

4	0	0	1	0	2	3	0	1	1	0	0	3	B	1

ESCC SPEC	VARIANT	OHMIC VALUE	TOLERANCE	TCR
4001023	**13** or **14** = 0402 **01** or **05** = 0603 **02** or **06** = 0805 **03** or **07** = 1206 **04** or **08** = 2010	The first three digits are significant figures and the last digit specifies the number of zero to follow. R designates decimal point. Example: **10R0** = 10 Ω **3901** = 3900 Ω **1004** = 1 MΩ	**L** = ± 0.01 % **P** = ± 0.02 % **W** = ± 0.05 % **B** = ± 0.10 %	**1** = ± 10 ppm/°C **0** = ± 5 ppm/°C (+22 °C; +70 °C) **2** = ± 25 ppm/°C **9** = ± 5 ppm/°C (-55 °C; +155 °C)

CODIFICATION PACKAGING - Waffle Pack

CODE 18	PACKAGING
W	25 min. (100 min. for size 0402), 1 mult
WA	100 min., 100 mult (1)

CODIFICATION PACKAGING - Plastic Tape (2)

CODE 18	PACKAGING
T	50 min. (100 min. for size 0402), 1 mult
TA	100 min., 100 mult
TB	250 min., 250 mult
TC	500 min., 500 mult
TD	1000 min., 1000 mult
TE	2500 min., 2500 mult
TF	Full tape (3)

CODIFICATION PACKAGING - Paper Tape (2)

CODE 18	PACKAGING
PT	100 min., 1 mult
PA	100 min., 100 mult
PB	250 min., 250 mult
PC	500 min., 500 mult
PD (3)	1000 min., 1000 mult
PE (3)	2500 min., 2500 mult
PF (3)(4)	Full tape

Notes

(1) Available only in size 1206
(2) Plastic tape in standard for all sizes. Paper tape in option for 0402, 0603, 0805 and 1206. Please consult Vishay Sfernice for 2010 size
(3) Not available for size 0402
(4) Qantity depending on size of chips

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